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Transmission Lines

6.1 OVERVIEW ON TRANSMISSION LINES

With today's high-technology products and faster logic devices, PCB transmission line effects become a limiting factor for proper circuit operation. A trace routed adjacent to a reference plane forms a simple transmission line. Consider the case of a multilayer PCB. When a trace is routed on an outer PCB layer, we have the microstrip topology, though it may be asymmetrical in construction. When a trace is routed on an internal PCB layer, the result is called stripline topology. Details on the effects of microstrip and stripline are provided in both Chapter 4 and this chapter.

A transmission line is a system of conductors, such as wires, waveguides, coaxial cables, or PCB traces suitable for conducting electric power or signals and electric power efficiently between two or more terminals.

To meet the challenges of high-speed digital processing, today's multilayer PCB must

- Reduce propagation delay between devices.
- Manage transmission line reflections and crosstalk (signal integrity).
- Reduce signal losses.
- Allow for higher density interconnections.

What are the electrical propagation modes that exist within a transmission line structure? A transmission line allows a signal to propagate from one device to another at or near the speed of light within a medium, as modified (slowed down) by the capacitance of the traces and by the active devices in the circuit. This signal contains some form of energy. Is this energy transmitted by electrons, line voltages and currents, or by something

else? In a transmission line, electrons do not travel in the conventional sense. An *electromagnetic field* is the component that is present within and around a transmission line. The energy is carried along the transmission line by an electromagnetic field.

We usually place units of measurements for intelligence that exist within transmission lines. These units are voltage and current. *Voltage* is a unit of measurement whose spatial derivative describes the electrostatic force exerted on the electrons. *Current* is a unit of measurement that describes how many electrons flow in a transmission line structure during a specific time period. Neither unit describes the electromagnetic field or the electromagnetic wave present in the structure.

Typical electromagnetic fields consist of the following partial list.

- AM/FM radio waves
- Television waves
- Light waves
- Cellular telephone/pager waves
- Microwave and radar transmissions
- EMI/RFI created as a byproduct (unwanted energy) of digital components

All of these waves travel near the speed of light in a medium. EMI/RFI is included in this list to show that electromagnetic energy is a waveform that may cause harmful interference to other electronic equipment susceptible to electromagnetic disruption.

If a transmission line is not properly terminated, circuit functionality and EMI concerns can exist. These concerns include voltage droop, ringing, overshoot, and undershoot. All concerns will severely compromise switching operations and system signal integrity. Transmission line effects must be considered when the round-trip propagation delay exceeds the switching-current transition time. Faster logic devices and their corresponding increase in edge rates are becoming more common in the sub-nanosecond range. A very long trace in a PCB can become an antenna for radiating RF currents or cause functionality problems if proper circuit design techniques are not used early in the design cycle.

When dealing with transmission line effects, the impedance of the trace becomes an important factor in designing a product for optimal performance. A signal that travels down a PCB trace will be absorbed at the far end if, and only if, the trace is terminated in its characteristic impedance. If a proper termination is *not* provided, most of the transmitted signal will be reflected back in the opposite direction. If an *improper* termination exists, multiple reflections will occur, resulting in a longer signal-settling time because of multiple overshoots and undershoots. This condition is known as *ringing*, and is discussed later in this chapter.

When a high-speed electrical signal travels through a transmission line, a propagating electromagnetic wave will move down the line (e.g., a wire, coaxial cable, or PCB trace). A PCB trace looks very different to the signal source at high signal speeds than it does at DC or at low signal speeds. The characteristic impedance of the transmission line is identified by the letter Z_o. For a lossless line, the characteristic impedance is equal to the square root of L/C, where L is the inductance per unit length divided by C, the capacitance per unit length. Impedance is also the ratio of the line voltage to the line current, in analogy to Ohm's law. When we examine Eq. (6.1), we see subscripts for the line voltage

and the line current. The ratio of line voltage to line current is constant with respect to the line distance x only for a matched termination. The (x) subscript indicates that variations in V and I will exist along the line, except for special cases.

$$Z_o = \sqrt{\frac{L_o}{C_o}} = \frac{V_{(x)}}{I_{(x)}} \tag{6.1}$$

We now examine *characteristic impedance*. As a logic signal transitions from a low to a high state, or vice versa, and propagates down a PCB trace, the impedance it encounters (the voltage to current ratio) is equal to a specific characteristic impedance. Once the signal has propagated up and down, trace reflections, if any, have died or become a nonissue related to signal integrity when the quiescent state is achieved. The characteristic impedance of the trace now has no effect on the signal. The signal becomes DC, and the line behaves as a typical wire.

To illustrate transmission line effects, let's assume a PCB trace has a propagation constant of 150 ps per inch, one way. Round-trip delay is this 300 ps per inch. If a clock driver has an edge rate of 2 ns, the transmission line characteristics of a short PCB trace is not a concern. This is because the signal will reflect back to the source long before the next edge-triggered event occurs. If properly terminated, the transmitted signal will have all possible reflections absorbed and dissipated within the network. Thus, a clean clock signal is available for the load device, which is the requirement for optimal functionality. If the clock trace is 10 inches in length, a serious problem could occur within the transmission line (the round-trip length of the trace is now 20 inches) since the reflected signal will return after the next edge-triggered event, causing possible functionality concerns if the trace is improperly terminated.

When a clock or strobe line drives multiple integrated circuits using a single trace, additional distributed capacitance and inductive elements are encountered because of additional components on the net. Each IC provides several pF of input shunt capacitance. This loading increases the capacitance value of the trace, thus increasing propagation delay of the signal. The increase in propagation delay occurs because distributed capacitance is proportional to the square root of the capacitance per unit length (Eq. 6.1). With a 2-ns and faster edge rate signal, transmission line effects become important for lead lengths of no more than a few inches.

Figure 6.1 shows conceptually what a typical transmission line looks like within a PCB structure. The resistance, R, is omitted for simplicity.

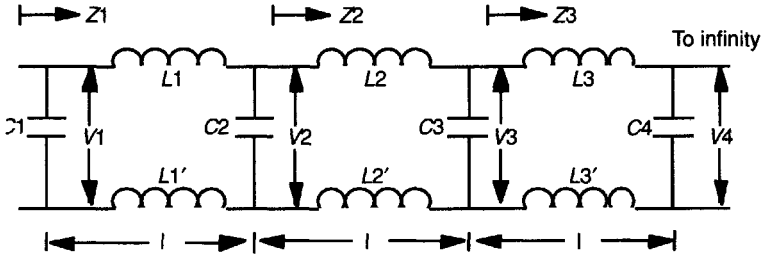


Figure 6.1 Transmission line equivalent circuit within a PCB.

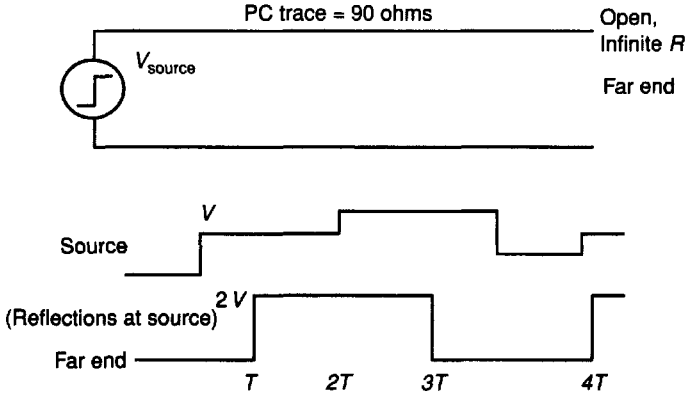
6.2 TRANSMISSION LINE BASICS

How can a transmission line cause problems? Problems occur when a signal on a PCB trace encounters an impedance discontinuity or a change in geometry. We can consider transmission line effects as Ohm's law for high-speed, edge rate signals. When the output driver changes logic state, the voltage to current ratio in the structure will equal the characteristic impedance, Z_o, of the trace. As long as the impedance within the transmission line does not change, the signal smoothly propagates without changing the shape of the signal. If the end of the transmission line is open (infinite impedance), the current must go to zero. At the end of the trace, the voltage to current ratio inverts, and to satisfy Ohm's law, a reflected wave that is equal, but opposite in polarity (phase relationship), is created to cancel the current that exists within the trace. The reflected wave returns to the source driver. If the driver impedance does not match the transmission line impedance, another reflected wave will be created and be re-reflected when the signal reaches the source driver. This process keeps happening until all the energy in the signal is absorbed within the network. A descriptive example of this reflection is shown in Fig. 6.2.

The voltage that is reflected at the end of the transmission line will be greater than the initial voltage if the termination impedance is greater than the line impedance. The voltage level will be less than the initial voltage if the termination impedance is less than the line impedance. The amplitude of the reflected voltage at the end of the transmission line is calculated by Eq. (6.2).

$$V_r = V_i\left(\frac{R_t - Z_o}{R_t + Z_o}\right) = \rho V_i \tag{6.2}$$

where V_r is the reflected voltage at the far end, V_i is the initial voltage, R_t is the termination impedance, Z_o is the characteristic line impedance of the trace, and ρ is the reflection



The top trace is the signal from the source driver.
The bottom trace illustrates the reflected waveform observed at the source if a mismatch exists within the transmission line structure.

Figure 6.2 Reflections in a transmission line.

coefficient. This equation identifies how much voltage gets reflected by the impedance mismatch. Notice that if $R = Z_o$, the reflection coefficient $\rho = 0$. There is no reflection and the voltage level does not change. If $R_t = \infty$, $\rho = +1$. This means that 100% of the voltage is reflected. This voltage will be double in value since the actual measured voltage is the sum of the initial voltage plus the reflected voltage. If $R_t = 0$, a short circuit exists, $\rho = -1$, and the voltage goes to zero. *The greater the mismatch, the greater the reflected voltage.* If both sides of the transmission line have mismatches, ringing will be created.

A circuit can be treated as a collection of lumped elements with capacitive and inductive components. This condition occurs when a signal path segment is small compared to the wavelength of a signal's highest frequency spectral component propagating down the trace. As the signal frequency increases, the circuit must be treated as a distributed transmission line. For this situation, controlled impedance, matched termination, and radiated emission effects must be considered.

6.3 TRANSMISSION LINE EFFECTS

For a high-speed transmission line, a fundamental concept exists called the *electrically long trace*. This means that as the length of the trace becomes greater than $\lambda/20$ (wavelength/20) of the signal (frequency domain), or the propagation delay becomes greater than rise time/4 (time domain), functionality concerns exist. The edge rate refers to a signal that changes logic in the period of dV/dt. We use the symbol t_r to identify edge rate. When using $\lambda/20$ and $t_r/4$ in the following discussions, we get roughly, but not exactly, the same line length. Depending on application, use of $\lambda/20$ *or* $t_r/4$ may provide a more accurate answer.

If the one-way "propagation time" distance from transmitter to receiver exceeds $\lambda/20$ (frequency domain) or the propagation delay is equal to or shorter than the propagation time of the trace with round-trip reflection, the PCB trace should be treated as a transmission line. These parameters are conservative. These traces may not fall within the electrically long trace requirement if the trace approximately equals these dimensions.

For a 1-ns edge rate signal, impedance matching may be required when the transmission line exceeds 9 cm (3.5 in.). Assuming a velocity of propagation, V_p that is 60% the speed of light ($c = 3 * 10^8$ m/s *or* $V_p = 1.8 * 10^8$ m/s), a line length greater than 9 cm must be treated as a transmission line which must include some type of termination. To determine this maximum line length, Eq. (6.3) is provided using the time domain analysis presented earlier.

$$\begin{aligned} l &= (t_r/2) * V_p \ (\textit{one way propagation travel}) \\ l &= (1 * 10^{-9} \text{ sec}/2) * 1.8 * 10^8 \text{ m/sec} \\ l &= 0.09 \text{ m (9 cm or 3.5 in.)} \end{aligned} \tag{6.3}$$

where l = trace length (of the transmission line)
V_p = velocity of propagation (60% the speed of light)
t_r = edge transition rate of the signal

With l = 19 cm (3.5 in.), any trace longer than 19 cm for a 1-ns edge rate transition is considered to be electrically long. This value is for a signal that propagates in free space and not for a microstrip or stripline structure. A PCB will cause the propagated signal to travel at a much slower speed due to the dielectric constant of the core or prepreg material.

The length of a signal path compared to the shortest wavelength of the signal trace determines whether the circuit should be treated as a lumped or distributed configuration. If the one-way path length of the trace is less than $\lambda/20$, a low-frequency lumped circuit can be assumed. If the path length is greater than $\lambda/20$, we can assume that a high-frequency distributed circuit is present. With a distributed circuit, the characteristic impedance of the trace must be controlled and a matched termination is required for good signal integrity.

A frequently asked question is, When does impedance matching require $Z_L = Z_o$ or $Z_s = Z_o$? For Fig. 6.3, is it necessary to match both the source driver *and* load of a transmission line. If the signal flow is bidirectional, as found on bus structures, both ends must be terminated. For a single-ended circuit (e.g., a clock signal from an oscillator to a load), only one end of the trace requires termination. A decision must be made as to whether to terminate at the source or load end of the circuit. Termination methods and their applications are discussed in Chapter 8. Which end to terminate depends on several factors (again, discussed in Chapter 8).

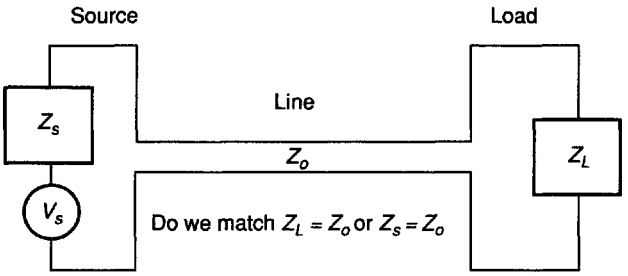


Figure 6.3 Impedance matching requirements of a circuit.

If the load value of Z_L is fixed, the transmission line is usually designed to match the load impedance, $Z_o = Z_L$. This transmission line connection occurs when preexisting equipment and the transmission line must be matched. If the load impedance is not known (which is often the case) or not predetermined, the optimal value for Z_o must be chosen so that the load is matched to the line ($Z_o = Z_L$). If Z_L is not known, termination pads to experimentally determine the correct component values for impedance matching should be provided on the PCB during layout.

To examine trace impedance in more detail, Fig. 6.4 illustrates a simple configuration. For a voltage pulse of amplitude V, driving a transmission line, Z_o, we have a drive current of $I = V/Z_o$. Assuming V = 5V, and Z_o = 5 Ω (an unrealistic value), we observe

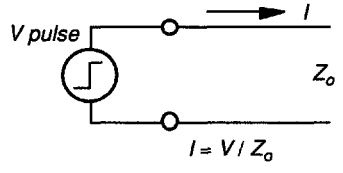


Figure 6.4 Simplified network for drive currents.

that the drive current would be 1A. If Z_o is now 50 Ω, a drive current of 100 mA is required. It is *not* advisable (for both functional purposes; power supply loading and EMI) to use source drivers with 100-mA drive capabilities for an application that generally requires only a few milliamps of drive current. For this reason, most components are designed to drive a minimal trace impedance of 30–65 Ω.

The propagation speed of a signal within a medium is finite. The propagation delay per unit length, δ, is equal to the square root of the inductance per unit length, L_o, times the capacitance per unit length, C_o. A typical PCB trace (with a dielectric constant of 4.6) has a propagation delay of 1.72 ns/ft (0.36 ns/cm or 0.143 ns/in.).

$$\delta = \sqrt{L_o C_o} \tag{6.4}$$

6.4 CREATING TRANSMISSION LINES IN A MULTILAYER PCB

Different logic families have different characteristic source impedance. Emitter-coupled logic (ECL) has a source and load impedance of 50 Ω. Transistor-transistor logic (TTL) has a source impedance range of 70 to 100 Ω. If a transmission line is to be created within a PCB, the engineer must seek to match the source impedance of the logic family being used.

Most high-speed traces must be impedance controlled. Calculations to determine proper trace width and separation to the nearest reference plane must occur. Board manufacturers and CAD programs can easily perform these calculations. If necessary, board fabricators can be consulted for assistance in designing the PCB, or a computer application program can be used to determine the most effective approach relative to trace width and distance spacing between planes for optimal performance. These approximate formulas may not be fully accurate because of manufacturing tolerances during the fabrication process. These formulas were simplified from exact models! Stock material may have a different thickness value and a different dielectric constant. The finished etched trace width may be different from a desired design requirement, or any number of manufacturing issues may exist. The board vendors know what the real variables are during construction and assembly. These vendors should be asked to provide the real or actual dielectric constant value, as well as the finished etched trace width for both base and crest dimensions, as shown in Fig. 6.5.

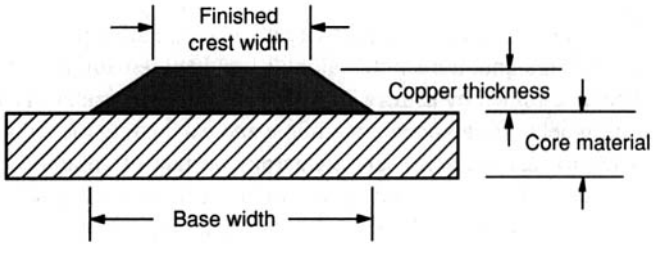


Figure 6.5 Finished trace width dimensions after etching.

6.5 RELATIVE PERMITTIVITY (DIELECTRIC CONSTANT)

Before giving a detailed description of how transmission lines are created within the PCB, we must examine the importance of the electrical parameter ε_r, also identified as *relative permittivity* or *dielectric constant.*

The relative dielectric constant ε_r is a measure of the amount of energy stored in the dielectric insulators per unit electric field, and hence a measure of the capacitance between a pair of conductors (trace-air, trace-trace, wire-wire, trace-wire, etc.) in the vicinity of the dielectric insulator compared to the capacitance of the same conductor pair in a vacuum. The relative dielectric constant of vacuum is 1.0. All materials have a dielectric constant greater than one. The larger the number, the more energy stored per unit insulator volume. The higher the capacitance, the slower the wave travels down the transmission line. The relationship between the capacitance and propagation speed was presented in Eq. (6.4).

Electromagnetic waves propagate at a speed that is dependent on the electrical properties of the surrounding medium. Propagation delay is typically measured in units of picoseconds/inch. Propagation delay is the inverse of velocity of propagation (the speed at which data is transmitted through conductors in a PCB), as presented in Chapter 2. The dielectric constant varies with several material parameters. Factors that influence the relative permittivity of a given material include the electrical frequency, temperature, extent of water absorption (also forming a dissipative loss), and the electrical characterization technique. In addition, if the PCB material is a composite of two or more laminates, the value of ε_r may vary significantly as the relative amount of resin and glass of the composite is varied [8].

In air, or vacuum, the velocity of propagation is the speed of light. In a dielectric material, the velocity of propagation is slower (approximately 0.6 times the speed of light for common PCB laminates). Both velocity of propagation and the effective dielectric constant are given by Eq. (6.5).

$$V_p = \frac{C}{\sqrt{\varepsilon_r}} \quad \text{(velocity of propagation)}$$
$$\varepsilon'_r = \left(\frac{C}{V_p}\right)^2 \quad \text{(dielectric constant)} \tag{6.5}$$

where C = $3 * 10^8$ meters per second, or about 30 cm/ns (12 in./ns)
ε'_r = effective dielectric constant
V_p = velocity of propagation

The effective relative permittivity ε'_r, is the relative permittivity that is experienced by an electrical signal transmitted along a conductive path. Effective relativity permittivity can be determined by using a Time Domain Reflectometer (TDR) or by measuring the propagation delay for a known length line and calculating the value.

The propagation delay and dielectric constant of common PCB base materials are presented in Table 6.1. Coaxial cables often use a dielectric insulator to reduce the effective dielectric insulator inside the cable to improve performance. This dielectric insulator lowers the propagation delay while simultaneously lowering the dielectric losses.

TABLE 6.1 Propagation Delay in Various Transmission Media

Medium	Propagation Delay (ps/in)	Relative Dielectric Constant
Air	85	1.0
FR-4 (PCB), microstrip	141–167	2.8–4.5
FR-4 (PCB), stripline	180	4.5
Alumina (PCB), stripline	240–270	8–10
Coax (65% velocity)	129	2.3
Coax (75% velocity)	113	1.8

FR-4, currently the most common material used in the fabrication of a PCB, has a dielectric constant that varies with the frequency of the signal within the material. Most engineers generally assume that ε_r is in the range of 4.5 to 4.7. These values, referenced by designers, have been published in various technical reference manuals for many years and are based on measurements taken with a 1-MHz reference signal. Measurements were not made on FR-4 material under actual operating conditions, especially with today's high-speed designs. What worked over 20 years ago is insufficient for twenty-first-century products. Knowledge of the correct value of ε_r for FR-4 must now be introduced. A more accurate value of ε_r is determined by measuring the actual propagation delay of a signal in a trace using a TDR. The values in Table 6.2 are based on a typical, high-speed edge rate signal.

Figure 6.6 shows the "real" value of ε_r for FR-4 material based on research by the Institute for Interconnecting and Packaging Electronics Circuits Organization (IPC). This chart has been published in document IPC-2141, *Controlled Impedance Circuit Boards and High Speed Logic Design.*

TABLE 6.2 Dielectric Constants and Wave Velocities of PCB Materials

Material	ε_r (at 30 MHz)	Velocity (inches/ns)	Velocity (ps/inch)
Air	1.0	11.76	85.0
PTFE/glass (Teflon)™	2.2	7.95	125.8
RO 2800	2.9	6.95	143.9
CE/custom ply (Cyanide ester)	3.0	6.86	145.8
BT/custom ply (Beta-Triazine)	3.3	6.50	153.8
CE/glass	3.7	6.12	163.4
Silicon dioxide	3.9	5.97	167.5
BT/glass	4.0	5.88	170.0
Polyimide/glass	4.1	5.82	171.8
FR-4 glass	4.5	5.87	170.4
Glass cloth	6.0	4.70	212.0
Alumina	9.0	3.90	256.4

Note: Values measured at TDR frequencies using velocity techniques. Values were not measured at 1 MHz, which provides faster velocity values. Units for velocity are different due to scaling and are presented in this format for ease of presentation.

Source: IPC-2141, *Controlled Impedance Circuit Boards and High Speed Logic Design,* Institute for Interconnecting and Packaging Electronics Design. © 1996. Reprinted with permission.

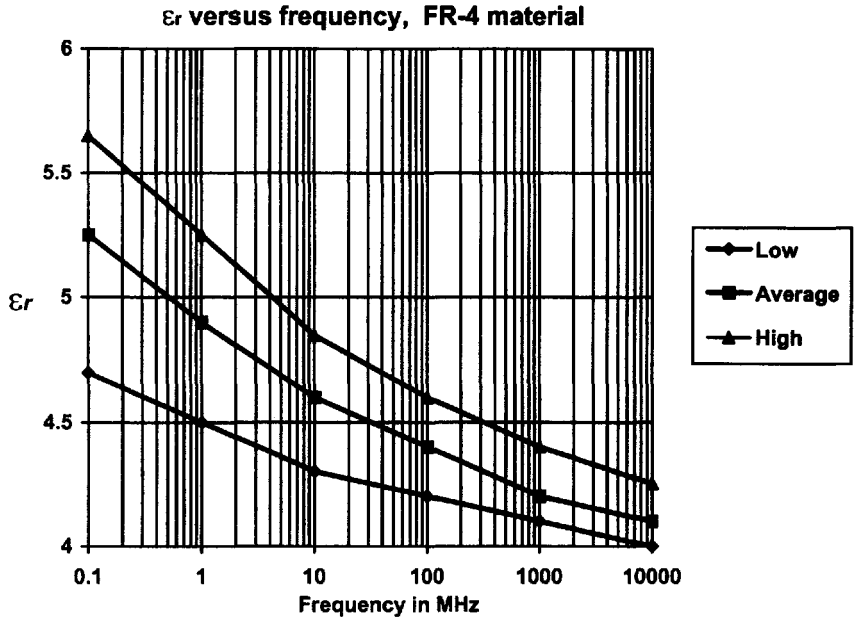


Figure 6.6 Actual dielectric constant values for FR-4 materials. (*Source:* IPC-2141, *Controlled Impedance Circuit Boards and High Speed Logic Design,* Institute for Interconnecting and Packaging Electronics Circuits. © 1996. Reprinted with permission.)

Figure 6.6 shows the frequency range from 100 kHz to 10 GHz for FR-4 laminate with a glass-to-resin ratio of approximately 40:60 by weight. The value of ε_r for this laminate ratio varies from about 4.7 to 4.0 over this frequency range. This change in the magnitude of ε_r is due principally to the frequency response of the resin and is reduced if the proportion of the glass ratio in the composite is increased. In addition, the frequency response will also be changed if an alternative resin system is selected. Material suppliers typically quote values of dielectric properties determined at 1 MHz, not at actual system frequencies that now easily exceed 100 MHz [9].

If a TDR is used for measuring the velocity of propagation, it is appropriate to use a frequency corresponding to the actual operating conditions of the PCB for comparing dielectric parameters. The TDR is a wideband measurement technique using time domain analysis. The location of the TDR on the trace being measured may affect measurement values. IPC-2141 provides an excellent discussion of how to use a TDR for propagational delay measurements [9].

The dielectric constant of various materials used to manufacture a PCB is provided in Table 6.2. These values are based on measurements using a TDR, and are not based on published, limited-basis reference information.

For microstrip topology, the dielectric constant is usually lower than the number provided by the manufacturer of the material. The reason is that part of the energy flow is in air or soldermask, and part of the energy flows within the dielectric medium. As a result, the signal will propagate faster down the trace than for the stripline configuration.

When a stripline conductor is surrounded by a single dielectric that extends to the reference planes, the value of ε'_r may be equated to that of ε_r for the dielectric measured

under appropriate operating conditions. If more than one dielectric exists between the conductor and reference plane, the value of ε'_r is determined from a weighted sum of values of ε_r for all contributing dielectrics. Use of an electromagnetic field solver is required for a more accurate ε'_r value [16, 17, 18]. For purposes of evaluating the electrical characteristics of PCB, a composite such as a reinforced laminate, with a specific ratio of compounds, is usually regarded as a homogeneous dielectric with an associated relative permittivity.

For microstrip with a compound dielectric medium consisting of board material and air, Kaupp [14] derived an empirical relationship that gives the effective relative permittivity as a function of board material. Use of electromagnetic field solver is required for a more accurate answer [16].

$$\varepsilon'_r = 0.475\varepsilon_r + 0.67 \quad \text{for } 2 < \varepsilon_r < 6 \tag{6.6}$$

In this expression, ε_r relates to values determined at 25 MHz.

Trace geometries also affect the electromagnetic field within a PCB structure. These geometries determine if the electromagnetic field is radiated into free space or if it will stay internal to the assembly. If the electric field stays local to, or in the board, the effective dielectric constant becomes greater and signals propagate more slowly. The dielectric constant value will change internal to the board based on where the electric field shares its electrons. For microstrip (see Section 6.6.1) the electric field shares its electrons with free space, whereas stripline configurations capture free electrons. Microstrip permits faster transitions of electromagnetic waves. These electric fields are associated with capacitive coupling (Chapter 2) owing to the field structure within the PCB. The greater the capacitive coupling between a trace and its reference plane, the slower the propagation of the electromagnetic wave.

6.5.1 How Losses Occur Within a Dielectric

When we speak about losses within a dielectric structure, the term *lossy dielectric* implies an energy loss or joule heating in the dielectric material. How does this energy loss or joule heating occur? An examination of the atomic mechanism of dielectric behavior reveals the causes of heating.

A dielectric material is any substance that resists the penetration of an electric field into its interior. Consider one plate of a dielectric within which we attempt to establish an electric field by piling negative charges along one side and positive charges along the other. The dielectric will resist the electric field by producing opposite charges at its surfaces wherever the charges appear. The more charge provided, the more the dielectric will counter with opposing charges. The effect of this action is to cancel out some of the electric fields that would otherwise have been produced inside the dielectric. The dielectric constant of a material is defined by the magnitude of this reduction. This magnitude is the ratio of the field which would have been produced without these opposing charges to the field which is actually produced. For example, if only one-third of the expected field occurs within the dielectric, its dielectric constant is 3. The dielectric constant of a vacuum is 1.

A dielectric behaves similar to a capacitor. As we pile charges onto one end and take them out of the other, the dielectric inside the capacitor is busy piling up canceling charges right next to the ones we put in. This process is performed at both ends of the capacitor and prevents a voltage potential from being established across the capacitor. To the outside observer it appears that the capacitor is "gobbling up" the charges (storing them).

From an atomic viewpoint, how does a dielectric do this? All substances consist of atoms, which in turn contain a positively charged nucleus and an equally (but negatively) charged circle of electrons. In a *conductor*, electrons are free to swim about (almost like a fluid) within the crystal lattice. In a *dielectric*, however, the electrons are bound to the nuclei. In the presence of an electric field, the electrons may shift slightly to one side (this is an extreme simplification of quantum mechanics). This tiny amount of shifting, though very small in comparison to the size of the atom, takes place for every atom within the dielectric. This shifting creates the effect of a bulk displacement of all positive charges toward the negative pole of the applied field and vice versa for the negative charge. The total amount of charge in any common substance is astounding but we are unaware of it because the positive and negative charges are always in near perfect balance. Because of this balance, even an exceedingly slight shift can cause a significant total effect to be observed.

This shifting effect is similar to a team sport in which the ball is reversed on the field. Every player takes two or three steps to the side. The net effect is the same as if a single player were moved from one side of the field to the other. The same thing happens in a dielectric. The net effect of shifting electrons is the same as if some charges were transferred from one side of the material to the other (positive charges appears on one surface, negative on the other). This shifting is called *polarization.*

How does "loss" come into all this, and what does it have to do with the resonant frequency of polarization? It all has to do with time delay. When a field is applied, the aforementioned shifting cannot occur instantaneously; there must be some time delay. This time delay occurs at the resonant frequency of polarization. If we apply a rapidly reversing field to a dielectric, a phase lag will take place between the applied field and the resulting polarization field. As the frequency of the applied field is increased, the absolute lag is constant; therefore, the phase lag increases. When the phase lag reaches $\pi/2$ (90 degrees) we are at resonance.

There is a frequency-dependent phase lag between the applied electric field and polarization. This polarization is the mechanism by which a dielectric resists the application of the electric field. This cancellation gives the appearance that the dielectric is "gobbling up" charge (e.g., drawing excess current). Thus, a frequency-dependent phase lag will occur between the applied electric field and the resulting current flowing to establish those fields.

For a molecular explanation of what is going on, we can imagine a dielectric sample to which we apply one half cycle of a very high-frequency electric field (single short electric pulse). As soon as the pulse arrives, the electrons begin shifting over toward the positive side of the field. Since the pulse is so short, the electric field disappears by the time the electrons have started moving. We now have many electrons that have acquired kinetic energy. This energy has to go somewhere. As the electrons move around to return to their normal equilibrium state, some of the energy stored in the polarization field is transferred into the crystal lattice as vibrational energy (heat). This all happens because the

pulse was so short that the electrons couldn't track it fast enough (phase lag). If the electric field were continuously oscillating instead of a single pulse, this effect would occur continuously. The shifting of the electrons would be out of phase with the applied electric field. It basically comes down to energy being pumped into the time-varying electric field between the atoms. This energy must eventually be dissipated into the crystal lattice, causing heating.

6.6 ROUTING TOPOLOGIES

Several techniques are available for creating a transmission line structure in a multilayer PCB. Two basic topologies are used, each of which has two configurations: microstrip (single and embedded) and stripline (single and dual).

Note: None of the equations provided in the next section for microstrip and stripline is applicable to PCBs constructed of two or more dielectric materials, excluding air, for example, or fabricated with more than one type of laminate. All equations are extracted from IPC-D-317A, *Design Guidelines for Electronic Packaging Utilizing High-Speed Techniques* [8].[1]

6.6.1 Microstrip Topology

Microstrip topology is a popular method used to provide trace-controlled impedance on a PCB for digital circuits. Microstrip lines are exposed to both air and a dielectric material referenced to a planar structure. The approximate formula for surface microstrip impedance is provided in Eq. (6.7) for the configuration of Fig 6.7. The intrinsic line capacitance is shown in Eq. (6.8).

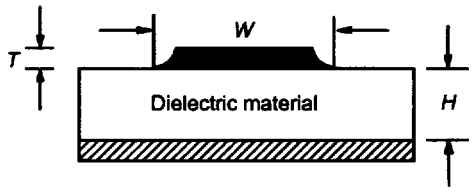


Figure 6.7 Surface microstrip topology.

[1]Within the IPC standards, typographical and mathematical errors exist in the section related to impedance. Before applying equations detailed within IPC-D-317, study and identify all errors before literal use. Equations presented herein have been verified for accuracy.

$$Z_o = \left(\frac{87}{\sqrt{\varepsilon_r + 1.41}}\right) ln\left(\frac{5.98\,H}{0.8\,W + T}\right)\Omega \quad \text{Valid for } 15 < w < 25 \text{ mils}$$
$$Z_o = \left(\frac{79}{\sqrt{\varepsilon_r + 1.41}}\right) ln\left(\frac{5.98\,H}{0.8\,W + T}\right)\Omega \quad \text{Valid for } 5 < w < 15 \text{ mils} \tag{6.7}$$

$$C_o = \frac{0.67(\varepsilon_r + 1.41)}{ln\left(\frac{5.98H}{0.8W + T}\right)} \quad \text{pf/inch} \tag{6.8}$$

where Z_o = characteristic impedance (ohms)
W = width of the trace (inches)
T = thickness of the trace (inches)
H = distance between signal trace and reference plane (inches)
C_o = intrinsic capacitance of the trace (pF/inch)
ε_r = dielectric constant of the planar material

Equation (6.7) is typically accurate to ± 5% when the ratio of W to H is 0.6 or less. When the ratio of W to H is between 0.6 and 2.0, accuracy typically drops ± 20%.

When measuring (or calculating trace impedance), the width of the line should technically be measured at the middle of the trace thickness. Depending on the manufacturing process, the finished line width after etching may be different from that specified (Fig. 6.5). The width of the copper on the top of the trace may be etched away, thus making the trace width smaller than desired. Using the average between top and bottom of the trace thickness, we find that a more typical, accurate impedance number is possible. With respect to the measurement of a trace's width, with an *ln* (natural logarithm) expression, how much significance should we give to accuracy of trace impedance for the majority of designs? Most manufacturing tolerances are well within 10% of desired impedance.

The propagation delay of a signal routed microstrip is described by Eq. (6.9) which has a variable of only ε_r. This equation states that the speed of a signal within a trace is related only to the effective permittivity of the dielectric material. Kaupp derived this equation for the propagation delay function under the square root radical [14].

$$t_{pd} = 1.017\sqrt{0.475\,\varepsilon_r + 0.67} \quad \text{(ns/ft)}$$
$$\text{or} \tag{6.9}$$
$$t_{pd} = 85\sqrt{0.475\,\varepsilon_r + 0.67} \quad \text{(ps/in.)}$$

6.6.2 Embedded Microstrip Topology

The embedded microstrip is a modified version of standard microstrip. The difference lies in providing a dielectric material on the top surface of the copper trace. This material may include another routing layer (core or prepreg material). If the embedded trace is surrounded by a material, such as soldermask, conformal coating, potting, or other material containing the same dielectric constant, with a thickness of 0.008 to 0.010 inch (8 to 10 mils) placed on top of the trace, air or the environment will have little effect on impedance calculations. Another way to view embedded microstrip is to compare it to a single, asymmetric stripline with one plane infinitely far away.

Coated microstrip uses the same conductor geometry as the uncoated except that the effective relative permittivity will be higher. Coated microstrip refers to placing a substrate on the outer microstrip layer. This substrate can be soldermask, conformal coating, or another material, including another microstrip layer. The dielectric on top of the trace may be asymmetrical to the host material. The difference between coated and uncoated microstrip is that the conductors on the top layer are fully enclosed by a dielectric substrate. The equations for embedded microstrip are the same as those for uncoated microstrip with a modified permittivity, ε'_r. If the dielectric thickness above the conductor is more than a few thousandths of an inch, ε'_r will need to be determined either by experimentation or by use of an electromagnetic field solver. For "very thin" coatings, such as soldermask or conformal coating, the effect is negligible. Masks and coatings may drop the impedance of the trace by several ohms.

The approximate formula for embedded microstrip impedance is provided by Eq. (6.10). For embedded microstrip, particularly those with asymmetrical dielectric heights, knowledge of the base and crown widths after etching will improve accuracy. These formulas are reasonable as long as the thickness of the upper dielectric material $[B - (T + H)]$ is greater than 0.004 inch (0.001 mm). If the coating is thin, or if the relative dielectric coefficient of the coating is different (e.g., conformal coating), the impedance will typically be between those calculated between microstrip and embedded microstrip.

Embedded microstrip is described in Eq. (6.10) for the configuration shown in Fig. 6.8. The intrinsic capacitance of the trace is defined in Eq. (6.11).

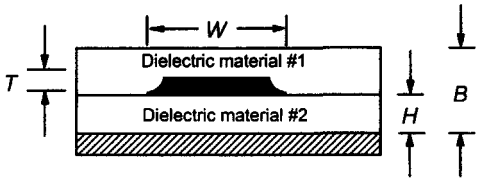


Figure 6.8 Embedded microstrip. NOTE: Thickness of the dielectric material may asymmetrical.

$$Z_o = \left(\frac{87}{\sqrt{\varepsilon'_r}}\right) ln\left(\frac{5.98\,H}{0.8\,W + T}\right) \Omega \qquad (6.10)$$

where: $\varepsilon'_r = \varepsilon_r \left\{1 - e^{\left(\frac{-1.55B}{H}\right)}\right\}$

$$C_o = \left(\frac{1}{H + T}\right) \times ln\left(1 - \frac{0.6897(\varepsilon_r + 1.41)}{\sqrt{\varepsilon_r}}\right) \text{ pF/inch} \qquad (6.11)$$

where Z_o = characteristic impedance (ohms)
C_o = intrinsic capacitance of the trace (pF/inch)
W = width of the trace (inches)
T = thickness of the trace (inches)
H = distance between signal trace and reference plane (inches)
B = overall distance of both dielectrics (inches)
ε_r = dielectric constant of the planar material

The propagation delay of a signal-routed embedded microstrip is given in Eq. (6.12). For a typical embedded microstrip, with FR-4 material and a dielectric constant that is 4.1, propagation delay is 0.35 ns/cm or 1.65 ns/ft (0.137 ns/in.). This propagation delay is the same as single stripline, discussed next, except with a modified ε'_r.

$$t_{pd} = 1.017\sqrt{\varepsilon'_r} \quad \text{(ns/ft)}$$

or

$$t_{pd} = 85\sqrt{\varepsilon'_r} \quad \text{(ps/in.)}$$

where

$$\varepsilon'_r = \varepsilon_r\left(1 - e^{\left(\frac{-1.55B}{H}\right)}\right) \tag{6.12}$$

$$0.1 < W/H < 3.0$$

$$1 < \varepsilon_r < 15$$

6.6.3 Single Stripline Topology

Stripline refers to a trace that is located between two planar conductive structures with a dielectric material completely surrounding the trace (Fig. 6.9). As a result, stripline traces, routed internal to the board, are not exposed to the external environment.

Routing stripline traces compared to microstrip has several advantages, namely, it captures fields and minimizes crosstalk, and it also provides an RF current reference return plane for magnetic field flux cancellation. Any radiated emissions that may occur from a routed trace will be captured by the reference plane and be prevented from radiating to the outside environment, provided the correct routing rules (e.g., the 3-W rule) are followed; see Chapter 7.7. Radiated emissions will still exist from components located on the outside layers of the board and their bond lead wires, not from the traces themselves buried within the PCB.

When measuring (or calculating) trace impedance, the microstrip section should be consulted for a discussion of why we should measure trace impedance of the line at the middle of the trace thickness after etching.

The approximate formula for single stripline impedance is provided in Eq. (6.13) for the illustration in Fig. 6.9. Intrinsic capacitance is presented in Eq. (6.14). Note that Eq. (6.14) is based on variables chosen for an optimal value. In actual board construction, the impedance may vary by as much as ± 5%.

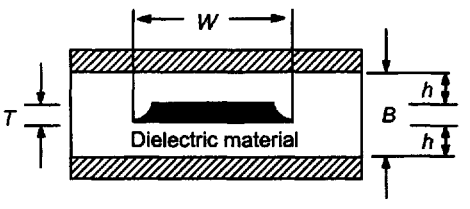


Figure 6.9 Single stripline topology.

$$Z_o = \left(\frac{60}{\sqrt{\varepsilon_r}}\right) ln\left(\frac{1.9B}{(0.8W + T)}\right) \Omega \tag{6.13}$$

$$C_o = \frac{1.41\varepsilon_r}{ln\left(\frac{3.81h}{0.8W + T}\right)} \quad \text{pF/inch} \tag{6.14}$$

where Z_o = characteristic impedance (ohms)
W = width of the trace (inches)
T = thickness of the trace (inches)
B = distance between both reference planes (inches)
h = distance between signal plane and reference plane (inches)
C_o = intrinsic capacitance of the trace (pF/inch)
ε_r = dielectric constant of the planar material
$W/(H - T) < 0.35$
$T/H < 0.25$

The propagation delay of signal stripline is described by Eq. (6.15), which has only ε_r as a variable.

$$t_{pd} = 1.017\sqrt{\varepsilon_r} \quad \text{(ns/ft)}$$
$$\text{or} \tag{6.15}$$
$$t_{pd} = 85\sqrt{\varepsilon_r} \quad \text{(ps/in.)}$$

6.6.4 Dual Stripline Topology

A variation on the single stripline is the dual stripline, which increases coupling between the circuit plane and the nearest reference plane. When the circuit is placed approximately in the middle one-third of the interplane region, the error caused by assuming the circuit to be centered will be quite small.

The approximate formula for dual stripline impedance provided in Eq. (6.16) is for the illustration of Fig. 6.10. This equation is a modified version of that used for a single stripline. Note that the same approximation reason as dual stripline is used to compute Z_o.

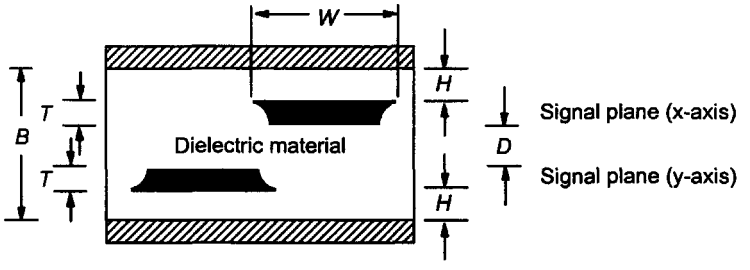


Figure 6.10 Dual stripline topology.

$$Z_o = \left(\frac{80}{\sqrt{\varepsilon_r}}\right) ln\left[\frac{1.9\,(2\,H + T)}{(0.8\,W + T)}\right]\left[1 - \frac{H}{4(H + D + T)}\right] \tag{6.16}$$

$$C_o = \frac{2.82\,\varepsilon_r}{ln\left[\frac{2(H - T)}{0.268W + 0.335T}\right]} \tag{6.17}$$

where Z_o = characteristic impedance (ohms)
W = width of the trace (inches)
T = thickness of the trace (inches)
D = distance between signal plane (inches)
H = dielectric thickness between signal plane and reference plane
C_o = intrinsic capacitance of the trace (pF/inch)
ε_r = dielectric constant of the planar material
$W/(H - T) < 0.35$
$T/H < 0.25$

Equation (6.16) can be applied to asymmetrical (single) stripline configuration when the trace is not centered equally between the two reference planes. In this situation, H is the distance from the center of the line to the nearest reference plane. The letter D would become the distance from the center of the line being evaluated to the other reference plane.

The propagation delay for the dual stripline configuration is the same as that for the single stripline, since both configurations are embedded in a homogeneous dielectric material.

$$t_{pd} = 1.017\sqrt{\varepsilon_r} \quad \text{(ns/ft)}$$

or (6.18)

$$t_{pd} = 85\sqrt{\varepsilon_r} \quad \text{(ps/in.)}$$

Note: When using the dual stripline, both routing layers must be routed orthogonal to each other. This means that one routing layer is provided for x-axis trace routing, while the other layer is used for y-axis traces. Routing these layers at 90 degree angles prevents crosstalk from occurring between the two routing planes with wide busses or with high-frequency traces causing data corruption to the alternate routing layer.

The actual operating impedance of a line can be significantly influenced (e.g., ≈ 30%) by multiple high-density crossovers of orthogonally routed traces, increasing the loading on the net and reducing the impedance of the transmission line. This impedance change occurs because these routed traces include a loaded impedance to the image plane, along with capacitance to the signal trace under observation. This is best illustrated by Fig. 6.11.

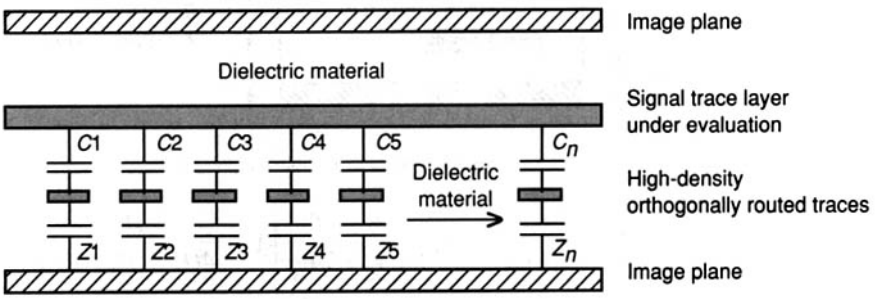


Figure 6.11 Impedance influences on dual stripline routing planes.

6.6.5 Differential Microstrip and Stripline

Differential traces have conductors routed adjacent to each other throughout the entire trace route. The impedance for differentially routed traces is not the same as a single-ended routed trace unless the position of the images obeys the *10-W* rule. The *10-W* rule refers to the distance separation between the two traces measured at 10 times the width (of an individual trace) from the centerline of one trace to the centerline of the other. For this configuration, sometimes only line-to-ground (or reference plane) impedance is considered as if the traces were routed single-ended. The concern should also be with the line-to-line impedance between the two traces operating in differential mode.

For Fig. 6.12, differential traces are shown. If the configuration is microstrip, the upper reference plane is not provided. For stripline, both reference planes are provided, with equal center spacing between the parallel traces and the two planes.

When calculating differential Z_o (Z_{diff}), trace width W should be adjusted to alter Z_{diff}. The user should not adjust D, which should be the minimal spacing specified by the PCB vendor [15].

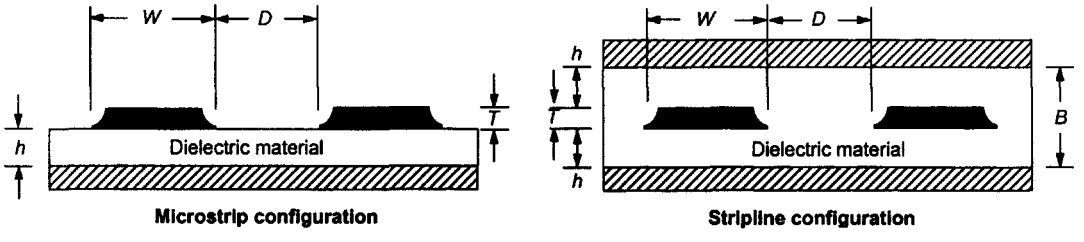


Figure 6.12 Differential trace routing topology.

$$Z_{diff} \approx 2 * Z_o\left(1 - 0.48e^{-0.96\frac{D}{h}}\right) \text{ ohms} \quad \text{(microstrip)}$$
$$Z_{diff} \approx 2 * Z_o\left(1 - 0.347e^{-2.9\frac{D}{B}}\right) \text{ohms} \quad \text{(stripline)} \tag{6.19}$$

$$Z_o = \frac{60}{\sqrt{0.475\,\varepsilon_r + 0.67}} ln\left(\frac{4h}{0.67(0.8W + T)}\right) \text{ ohms} \quad \text{(microstrip)}$$
$$Z_o = \frac{60}{\sqrt{\varepsilon_r}} ln\left(\frac{4h}{0.67\,\pi(0.8W + 1)}\right) \text{ ohms} \quad \text{(stripline)} \tag{6.20}$$

where B = plane separation
W = width of the trace
T = thickness of the trace
D = trace edge-to-edge spacing
h = distance spacing to nearest reference plane
Note: Use consistent dimensions for the above (inches or centimeters).

6.7 ROUTING CONCERNS

In regards to multiple loads daisychained on a net when a signal travels along a transmission line, the transition voltage will change at different propagation times. The difference in the reception time at the loads located at various propagational positions along the net is referred to as clock skew (see Chapter 3). Since the component closest to the driver will receive the signal before a load at the end of a long trace, synchronous clocking of multiple devices becomes difficult, especially if the edge rate is extremely fast and the trace length is electrically broken up into different propagational lengths.

If clock skew is an important consideration for multiple loads on a bus structure, microstrip is preferred. This is because signal propagation for microstrip is faster than stripline (1.65 ns/ft vs. 2.06 ns/ft with a dielectric constant of 4.1). Microstrip is faster than stripline by approximately 25%. This is because stripline has twice the capacitance per unit length owing to the routing layers sandwiched between two planar structures (compared to microstrip with one adjacent plane). The effective ε_r is lower, thus higher $v = c/\sqrt{\varepsilon_r}$. Propagation time, δ, per unit length is proportional to the square root of the product of inductance and capacitance per unit length; see Eq. (6.4).

When radiated emissions is a concern, routing a trace using stripline is preferred. Unfortunately, single (centered) stripline assemblies are more difficult to handle from a manufacturing viewpoint. The PCB would become extremely thick if a single stripline configuration and a large layer stackup were provided. With increased layers, dual stripline is an optimal choice. Emissions performance is enhanced since two routing layers exist between two planar "image" (shield layers). Crosstalk is also minimized at the same time because the routing layers are always placed orthogonally to each other, (one layer in the x-axis, the other layer in the y-axis) or separated by interplaced image planes.

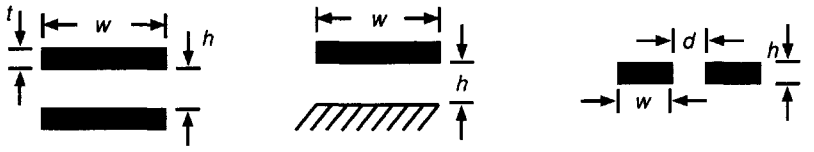
With different logic families and impedance concerns within a PCB, the characteristic impedance of a trace may also have to be different. An example of changing trace impedance in an impedance controlled assembly follows.

EXAMPLE

A motherboard is designed for a controlled 50-Ω impedance for all logic functions. Video circuitry must be routed at 75 Ω. How does one create two different impedance traces on the same PCB structure? This operation can be performed by changing physical dimensions within the PCB assembly. To change the impedance of a trace within a PCB, the following techniques are available from easiest (lower costs in board construction) to a more costly implementation method.

- Changing trace width referenced to a plane.
- Changing distance spacing between the routing layer and the reference plane.
- Removing a portion of the reference plane underneath the signal trace and allowing the trace to be referenced to another plane within the structure at a distance further away than the original reference plane (requires absence of copper over what would normally be a solid plane and a trace-void zone in adjacent layers).
- Changing thickness of the PCB layers (core material).
- Using a different dielectric constant (core or prepreg) between planar structures.

TABLE 6.3 Impedance of Different Conductor Pairs



w/h or d/w	Parallel Traces Z_{o1}	Trace over Ground plane Z_{o2}	Traces Side by Side Z_{o3}
0.5	377	377	NA
0.6	281	281	NA
0.7	241	241	NA
0.8	211	211	NA
0.9	187	187	NA
1.0	169	169	0
1.1	153	153	25
1.2	140	140	34
1.5	112	112	53
1.7	99	99	62
2.0	84	84	73
2.5	67	67	87
3.0	56	56	98
3.5	48	48	107
4.0	42	42	114
5.0	34	34	127
6.0	28	28	137
7.0	24	24	146
8.0	21	21	153
9.0	19	19	160
10.0	17	17	166
12.0	14	14	176
15.0	11.2	11.2	188
20.0	8.4	8.4	204
25.0	6.7	6.7	217
30.0	5.6	5.6	227
40.0	4.2	4.2	243
50.0	3.4	3.4	255
100	1.7	1.7	293

N/A = not applicable

$$Z_{o1} = \left(377/\sqrt{\varepsilon_r}\right)(h/w), \text{ for } W > 3h \text{ and } h > 3t$$

$$Z_{o2} = \left(377/\sqrt{\varepsilon_r}\right)(h/w), \text{ for } W > 3h$$

$$Z_{o3} = \left(120/\sqrt{\varepsilon_r}\right) ln_e\,(d/w + \sqrt{(d/w^2 - 1}, \text{ for } W >> 1$$

$d >>$ nearby ground plane

Changing the width of the trace is the easiest method if a different impedance is required. If different logic families are provided in an assembly, poor performance or signal integrity can exist if impedance-controlled traces are routed on the same layer. Table 6.3 illustrates different impedance values for three common trace configurations [13].

6.8 CAPACITIVE LOADING

Capacitive input loading affects trace impedance and will increase with gate loading (additional devices added to the routed net). The unloaded propagation delay for a transmission line is defined by $t_{pd} = \sqrt{L_o C_o}$. If a lumped load, C_d, is placed in the transmission line (includes all loads with their capacitance added together), the propagation delay of the signal trace will increase by a factor of

$$t'_{pd} = t_{pd}\sqrt{1 + \frac{C_d}{C_o}} \text{ ns/length} \tag{6.21}$$

where t_{pd} = unmodified propagation delay, nonloaded circuit
t'_{pd} = modified propagation delay when capacitance is added to the circuit
C_d = input gate capacitance from all loads
C_o = characteristic capacitance of the transmission line

For example, let's assume a load of five CMOS components are on a signal route, each with 10-pF input capacitance (total of C_d = 50 pF). With this capacitance value on a glass epoxy board, 25 mil traces, and a characteristic board impedance Z_o = 50 Ω (t_r = 1.65 ns/ft), there exists a value of C_o = 35 pF. The modified propagation delay is:

$$t'_{pd} = 1.65 \text{ ns/ft}\sqrt{1 + \frac{50}{35}} = 2.57 \text{ ns/ft} \tag{6.22}$$

This equation states that the signal arrives at its destination 2.57 ns/ft (0.54 ns/cm) later than expected. The characteristic impedance of this transmission line, altered by gate loading, Z'_o, is:

$$Z'_o = \frac{Z_o}{\sqrt{1 + \frac{C_d}{C_o}}} \tag{6.23}$$

where Z_o = original line impedance (ohms)
Z'_o = modified line impedance (ohms)
C_d = input gate capacitance—sum of all capacitive loads
C_o = characteristic capacitance of the transmission line

For the example above

$$Z'_o = \frac{50}{\sqrt{1 + \frac{50}{35}}} = 32\ \Omega$$

Typical values of C_d are 5 pF for each ECL input, 10 pF for each CMOS device, and 10–15 pF for TTL. Typical C_o values of a PCB trace are 2–2.5 pF/inch. These C_o values are subject to wide variations due to the physical geometry and the length of the trace. Sockets and vias also add to the distributed capacitance (sockets ≈ 2 pF and vias ≈ 0.3–0.8 pF each). Given that $t_{pd} = \sqrt{L_o * C_o}$ and $Z_o = \sqrt{L_o / C_o}$, C_o can be calculated as

$$C_o = 1000 \left(\frac{t_{pd}}{Z_o}\right) \text{pF / length} \tag{6.24}$$

This loaded propagation delay value is one method that may be used to decide if a trace should be treated as a transmission line ($2 * t'_{pd} *$ trace length $> t_r$ or t_f) where t_r is the rising edge of the signal and t_f is the falling edge.

C_d, the distributed capacitance per length of trace, depends on the capacitive load of all devices including vias and sockets, if provided. To mask transmission line effects, slower edge times are recommended. A heavily loaded trace slows the rise and fall times of the signal due to an increased time constant ($\tau = ZC$) associated with increased distributed capacitance and filtering of high-frequency components from the switching device. Notice that the impedance, Z, is used, and not R (pure resistance) for the time constant equation. This is because Z consists of real resistance and inductive reactance. Inductive reactance, $(j\omega L)$, is much greater than R in the trace structure at RF frequencies, which must be taken into consideration. Heavily loaded traces seem advantageous until the loaded trace condition is considered in detail.

A high C_d increases the loaded propagation delay and lowers the loaded characteristic impedance. The higher loaded propagation delay value increases the likelihood that transmission line effects will not be masked during rise and fall transition states. A lower loaded characteristic impedance often exaggerates impedance mismatches between the driving device and the PCB trace. Thus, the apparent benefits of a heavily loaded trace are not realized unless the driving gate is designed to drive large capacitive loads [2].

Loading alters the characteristic impedance of the trace. As with the loaded propagation delay, a high ratio between distributed capacitance and intrinsic capacitance exaggerates the effects of loading on the characteristic impedance. Because $Z_o = \sqrt{L_o / (C_o + C_d)}$, the additional load, C_d, adds capacitance. The loading factor $\sqrt{1 + C_d/C_o}$ divides in Z_o, and the characteristic impedance is lowered when the trace is loaded. Reflections on a loaded trace, which cause ringing, overshoots, undershoots, and switching delays, are more extreme when the loaded characteristic impedance differs substantially from the driving device's output impedance and the receiving device's input impedance. The units of measurements used for both capacitance and inductance are *per inch* or *cm* units. If the capacitance used in the L_o equation is pF/inch, the resulting inductance will be in pH/inch.

With knowledge of added capacitance lowering the trace impedance, it becomes apparent that if a device is driving more than one line, the active impedance of each line must be determined separately. This determination must be based on the number of loads

and the length of each line. Careful control of circuit impedance and reflections for trace routing and load distribution must be given serious consideration during the design and layout of the PCB.

If capacitive input loading is high, compensating a signal may not be practical. Compensation refers to modifying the transmitted signal to enhance the quality of the received signal pulse using a variety of design techniques. For example, use of a series resistor, or a different termination method to prevent reflections or ringing that may be present in the transmission line, is one method to compensate a distorted signal. Reflections in multiple lines from a single source must also be considered.

The low impedance often encountered in the PCB sometimes prevents proper Z_o (impedance) termination. If this condition exists, a series resistor as large as possible should be put in the trace (without corrupting signal integrity). Even a 10-Ω resistor is helpful; however, 33-Ω is commonly used.

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