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Image Planes

4.1 OVERVIEW

In any digital system, especially with high-speed components (fast edge rate), a low-impedance (low-inductance) RF return current path must be present for optimal performance. As examined in Chapter 2, a closed-loop network is required for reasons of functionality. This closed-loop network is required for both time and frequency domain aspects of the circuit. All components and all possible trace or wire interconnects that exist must operate in an environment in which the RF return currents find their way back to their source (low-impedance path).

Since RF currents must return to their source (closed-loop circuit), they will do so using any path possible. We must control all return currents using conductive paths. An alternate conductive return path is better than no path at all. If no conductive path exists, free space becomes the path. Free space is exactly what we do not want as a return path for RF currents, especially with regulatory compliance concerns.

Examining Fig. 4.1, we see that the RF return currents do not have an optimal return path home. Assume that the components are tied to a voltage reference source only by traces to the power supply structure. In the time domain, functionality concerns are met, and the circuit works. The RF return path occurs through the ground wires that provide the 0V reference to the circuit. Why should digital designers worry about EMC issues when the circuit operates per marketing specification and logic signals travel from source to load without functional degradation?

As discussed in Chapter 2, time and frequency domain aspects of a circuit must be considered simultaneously. Return currents (DC voltage reference) occur through the power and 0V reference (ground) structure of the PCB. These return currents exist in both the time and frequency domain for each and every trace. While a single-sided PCB may

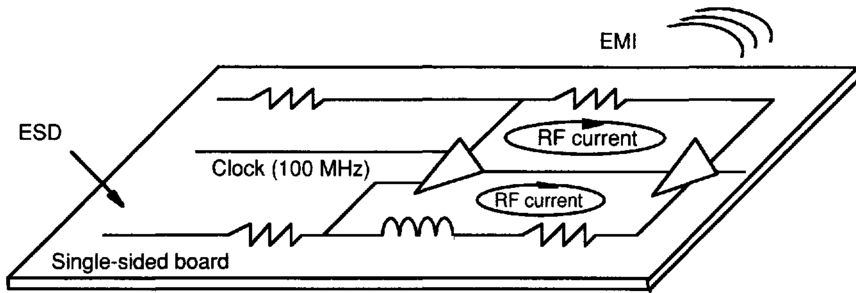


Figure 4.1 Typical PCB design without an RF return current system.

be a cost-effective implementation of a design (which will maximize profits), the probability is high that this simple configuration will not pass various EMC test requirements. Adding a ground plane (two-layer board), or making the assembly a four-layer design will enhance the overall performance of the assembly related to signal integrity and EMC compliance. While cost is being taken out of the PCB by using a single-sided design, alternative methods of EMC compliance may be required, which may include adding an expensive metal cover or metalized plastic enclosure.

In addition to maximizing radiated emissions between two components, the PCB becomes sensitive to ESD events. A high-current pulse, along with its effective radiated field, will see a lower impedance provided by the PCB than that observed by free space. This radiated field becomes impressed into the trace. Component failure may occur by damage to the die internal to the component package. In addition, a functional glitch may also occur, degrading the performance of the product.

High-technology CMOS products are sensitive to ESD events. This sensitivity requires special handling during the assembly cycle, yet protection against ESD on the PCB is frequently not considered, especially if cost has to be added to the board.

A good 0V reference (ground) system is the foundation of any digital PCB. If the 0V reference system is poor, it becomes difficult to fix an EMI problem when one develops. Indeed, a poor 0V reference implementation may be the actual cause of the problem. The only remedy is to redesign the board or start the design over from scratch. Adding in two more layers to a double-sided PCB, for example, a power and ground plane, requires only minimal work, yet will achieve improvement between 10 to 20 dB on radiated emissions as documented in numerous EMC publications, textbooks, and technical papers (not identified) herein. (For a sample list of publications, see References at end of this chapter and the Bibliography.)

EMI test failures can negate the cost-effectiveness of using less expensive double-sided boards. An extra round of EMC tests (emissions and immunity), redesign and relayout, and a prototype build for functionality testing, tying up engineering resources and adding many weeks of delay to the schedule, can easily result in costs exceeding tens of thousands of dollars. An incremental cost in adding two more layers may be cheaper than trying to maintain a double-sided structure. Depending on the number of boards to be produced, a cost saving may occur using multilayer boards. In one experience, $50,000 was spent in additional engineering resources to optimize a double-sided board—all in an effort to save $10,000 in production costs. Management must consider these financial values before making a decision to remain with an ill-considered design.

Taking this concern to the next level, we may find an indefinite number of parallel return paths. This is because many interconnects occur between components, along with connection into a power distribution network. Since a large number of return paths may be present, we can take advantage of this feature and convert "infinity" to one ($\infty \rightarrow 1$). This number one (1) is identified as an image plane. We generally refer to the 0V reference structure of the PCB as a ground plane. In ECL systems, the power plane is referred to as the 0V reference. In reality, any copper laminate in a multilayer stackup provides a return path with minimal impedance for RF return currents. Since RF return currents flow on the copper laminate in the first level using skin effect, the voltage potential (e.g., +5V, +12V, etc.) is not a major concern, except under certain operating conditions. The disadvantage of using a multilayer board lies in cost. For many applications, use of a multilayer design is not economically possible. For this situation, an alternate and effective return path for RF return currents must be established, perhaps through use of a gridded ground system, ground traces, or other creative means, as described later.

Discussion of multilayer boards is predominant in this chapter because technology is evolving at a rapid rate. There is practically no such thing as a slow-speed logic device anymore. Manufacturers of components are constantly improving their yield production using a "die shrink" process. To accomplish die shrink and increase yields, in addition to making their circuit desirable for use in a competitive marketplace, an increase in operating speed becomes mandatory. In addition, the lithography line widths within the die becomes smaller, with a corresponding increase in speed and faster edge rate.

Most "component vendors" concern themselves only with profit, not with EMC compliance. It is generally not a priority issue for these component vendors to recognize that their customers (users) are required, by law in many cases, to have their end product comply with emissions and immunity requirements. According to many component vendors, components do not cause EMI. Their components are always used with other components on a PCB; hence, many vendors consider themselves exempt from regulatory compliance concerns. A faster edge rate device will still work in slower speed products. Why, then, should semiconductor vendors worry about retooling their equipment to build a slower speed device when a faster device can be made available for less money and be pin-for-pin compatible?

A *brief* discussion of single- and double-sided boards will be presented for completeness. High-technology products require use of multilayer stackups.

4.2 5/5 RULE

The 5/5 rule[1] indicates when use of multilayer boards becomes necessary. The rule states that when clock speeds in excess of 5 MHz, or when rise times faster than 5 ns exist, a multilayer board should be used as the "crossover" point, beyond which faster edges and higher frequencies proportionally increase the need for multilayer boards. With proper design and layout techniques, the 5/5 rule can be changed to use faster clock and edge rates, *only* if the designer is aware of the problems that can exist when using these faster edge rate devices and high clock speeds. The designer must have extensive experience in designing high-technology products using a simpler board stackup assignment. This is an extremely difficult task to accomplish with minimal cost [3].

[1]The 5/5 rule and definition were first used by Daryl Gerke and Bill Kimmel [3].

4.3 HOW IMAGE PLANES WORK

In Chapter 2, we examined the need for flux cancellation or minimization. Image planes provide flux cancellation or minimization by allowing RF return currents to image back along its source path differentially. Here the term *differentially* describes the phase relationship between the signal and its return image. A detailed discussion of common-mode and differential-mode currents is found in Chapter 2. When an RF return path is placed in close proximity to a wire or trace, magnetic lines of flux which are opposite in polarity cancel each other out. We now examine the physics of this discussion.

When current travels through a PCB trace, an electromagnetic field is generated by magnetic lines of flux created within the transmission path. Maxwell's equations describe the development of an electric field from magnetic lines of flux, and vice versa. Depending on the length of the routed trace, radiated emissions may be created. Traces and copper planes have a finite amount of inductance. This inductance inhibits current buildup and charge whenever a voltage is applied to the trace or transmission line.

Research has shown [6] that if a two-wire transmission line is slightly unbalanced, the trace will radiate as an asymmetrical dipole antenna. This unbalanced structure will create common-mode radiated emissions at levels much greater than the differential-mode radiation that exists within the closed-loop circuit, detailed in Chapter 2.

Before examining how an image plane works within a PCB, the following briefly summarizes the difference between various types of inductance within the board structure [2]. These are

Partial inductance: the inductance that exists in a wire or PCB trace.

Self partial inductance: the inductance from one wire segment relative to an infinite segment.

Mutual partial inductance: the effects that one inductive segment has on a second inductive segment.

4.3.1 Inductance

At any frequency, a conductive element such as a wire or PCB trace exhibits inductance. The distributed inductance, capacitance, and resistance of traces, vias, and planes on a PCB must be considered at the same time as lumped parameters of all circuit components. The most difficult parameter to investigate or quantify is inductance. Unlike capacitance and resistance, inductance is a dynamic property of a closed-loop current path.

Inductance is defined as the ratio of total magnetic flux that couples (passes through) a closed-loop path to the amplitude of the current that produces the magnetic flux. Inductance is described by Eq. (4.1).

$$L_{ij} = \frac{\psi_{ij}}{I_i} \; henries \tag{4.1}$$

where ψ = magnetic flux and I is the current in the loop structure. If the wire is configured in a closed-loop circuit, the inductance is a function of loop geometry as well as the shape and dimensions of the wire itself.

The inductance of a wire or PCB trace is frequently overlooked when designing a PCB. Inductance is always associated with a closed-loop circuit. To describe the effects of inductance on a loop circuit, we must examine the effects of *partial inductance* and *mutual partial inductance*.

4.3.2 Partial Inductance

Partial inductance is defined as the internal inductance of a conductor due to magnetic flux that is present within the conductor [2]. But this definition is not entirely true.

Inductance is defined only for closed-loop circuits. To simplify the need to study partial inductance, we investigate separate sections of a current loop. This approach allows investigation of the overall effect that a transmission path has in a circuit. To lower the overall inductance of the circuit, or circuit geometry, it is first necessary to reduce the inductance of the section that has the greatest amount of inductance. Reduction may occur by shortening a routed trace length, removing vias, increasing the width of the conductor, or other methods, including trace reorientation. Partial inductance is useful for estimating the voltage drop across part of a circuit due to the inductance of that particular section. Care must be taken since the voltage drop or potential difference is not uniquely defined in the presence of time-varying fields.

The total partial inductance of a closed-loop segment is the sum of all sections. This is shown by

$$L_{\text{total}} = L_{\text{partial segment1}} + L_{\text{partial segment2}} + \dots + L_{\text{partial segment } n} = \sum_{i=1}^{n} Li \tag{4.2}$$

With Eq. (4.2), the static current within each segment is identical. L_{total} is the total flux of current in the loop. With this information, we can define partial inductance for a particular segment as the ratio of flux coupling to the current within a particular segment, Eq. (4.3).

$$L_{\text{partial segment}}\ i = \frac{\psi_i}{I} = \frac{\text{flux due to segment "}i\text{" that couples the loop}}{\text{amplitude of the current in segment } i} \tag{4.3}$$

The concept of partial inductance is for a single loop. Obviously, different loops will have different values of partial inductance.

The total internal inductance of a conductor will decrease, but the internal impedance still increases with the square root of the frequency owing to skin effect. Because of skin effect, the inductance that exists within the center portion of the conductor plays a minor role in the overall inductive performance of the conductor. The parameter of interest is the partial inductance, which is frequency-independent, not the total inductance of the trace. With knowledge of frequency independent inductance, the mutual inductance between two parallel conductors (or a trace over image plane) can be determined by the general equation, Eq. (4.4). A more detailed presentation of partial and mutual partial inductance is provided in Eq. (4.5).

4.3.3 Mutual Partial Inductance

Mutual partial inductance [2,6,9] is the key element that allows an image plane to provide for flux cancellation. Flux cancellation occurs by allowing magnetic lines of flux to link and find an optimal return path for RF currents.

Self partial inductance applies to a given segment of a loop independent of the location or orientation to any other loop segment. Given a current within a wire or trace, a nominal rectangular loop is defined, bounded by the wire segment on one side and infinity on the other side. These two perpendicular wire segments extend from the ends of the segments into infinity. This is illustrated by Fig. 4.2. Since self partial inductance is present between a wire segment and an infinite structure, we can develop the concept of *mutual partial inductance* [9] .

Consider an isolated conductor (or trace), length L, carrying current I. The *self partial inductance* of the conductor, L_p, is the "ratio of net magnetic flux generated by a current I passing through the loop (or between a conductor and through infinity, beyond the trace), divided by the current I within the wire segment" [2].

Self partial inductance is, of course, theoretically independent of the proximity to adjacent conductors. Closely spaced conductors, however, can alter the self partial inductance of one or both of the conductors. This is because one conductor will interact with the other conductor and cause current distributions over the entire length of the conductor to deviate from a uniform condition. This typically occurs when the ratio of wire separation to radius is less than approximately 5:1. A separation radius of 4:1 for two identical wires means that a third wire may fit between the two original wires if the wire radius is identical [2].

Between two conductors, *mutual partial inductance* exists. Mutual partial inductance, M_p, is based on the distance spacing between parallel traces or wire segments. The distance, s, is the ratio of "magnetic flux due to current in the first conductor that passes between the second conductor and into infinity" to "the current in the first conductor that produced it." Mutual partial inductance is observed in Fig. 4.2 with the electrical schematic detailed in Fig. 4.3. The voltage developed across the conductors from this configuration is described by Eq. (4.4) [2] .

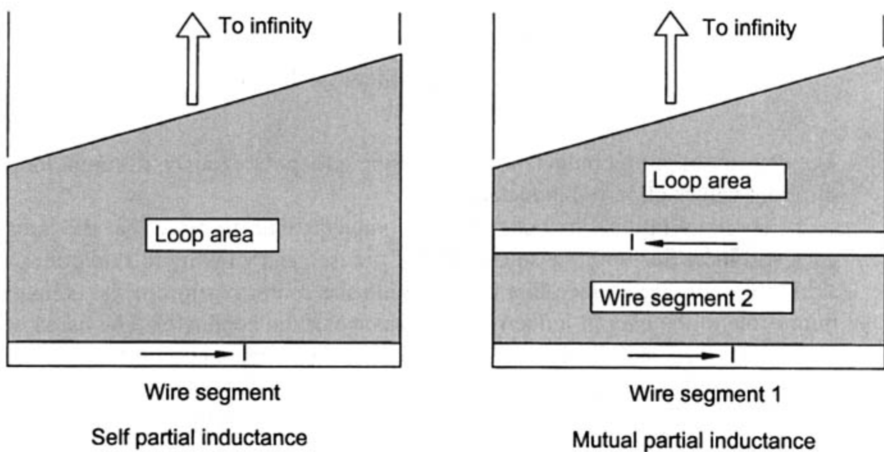


Figure 4.2 Loop area defining self and mutual partial inductance.

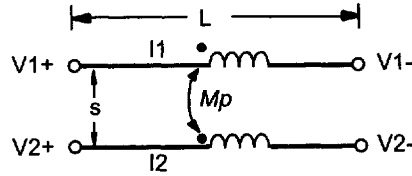


Figure 4.3 Mutual partial inductance between two conductors.

Note: Any trace or conductor contains inductance

$$V_1 = L_{p1}\frac{dI_1}{dt} + M_p\frac{dI_2}{dt}$$
$$V_2 = M_p\frac{dI_1}{dt} + L_{p2}\frac{dI_2}{dt} \qquad (4.4)$$

With the concept of mutual partial inductance, consider the two traces in Fig. 4.3 are now carrying a signal of interest, for example, clock. The trace identified as V_1 is the signal path, and the trace identified as V_2 is the RF current return path. Assume two conductors constitute a signal path and its associated return so that $I_1 = I$ and $I_2 = I_1 = -I$. If there is no mutual coupling between two conductors, the circuit cannot function, for a closed-loop circuit will not exist (Chapter 2). The voltage drop within the circuit of Fig. 4.3 becomes

$$V_1 = (L_{p1} - M_p)\frac{dI}{dt}$$
$$V_2 = -(L_{p2} - M_p)\frac{dI}{dt} \qquad (4.5)$$

According to Eq. (4.5), in order to reduce the voltage drop across a conductor, we must *maximize* the mutual partial inductance between that conductor and its associated conductor within the same circuit. The easiest way to maximize mutual partial inductance is to provide a path for RF return current as close as possible to the signal trace. The most optimal design technique is use of an RF return plane located adjacent to the signal trace with the smallest distance spacing that is manufacturable. An alternative way to maximize mutual partial inductance for single- and double-sided PCBs is to provide an RF return path (trace) adjacent to the signal trace with a distance spacing that is as small as possible.

To view the effects of both partial and mutual partial inductance, consider two traces or a trace over a plane. Partial inductance will always exist in a conductor (by default), and inductance will equate to an antenna at a specific resonant frequency. Mutual partial inductance minimizes the effects of partial inductance. By locating two conductors close together, the individual partial inductance becomes minimized, which is a desired design requirement for EMI compliance within the boundary of an "image" between the conductors.

To optimize mutual partial inductance, the currents in the two conductors must be equal in magnitude and opposite in direction. This is why image planes (and ground traces) work as well as they do. Because mutual partial inductance exists between two parallel wires, a certain amount of inductance will be present. Table 4.1 provides details on the mutual partial inductance between two parallel wires with various spacings [2].

Since mutual partial inductance was examined for signal traces, how does this inductance relate to power and ground planes separated by a dielectric material? The mutual

TABLE 4.1 Mutual Partial Inductance Between Two Parallel Wires

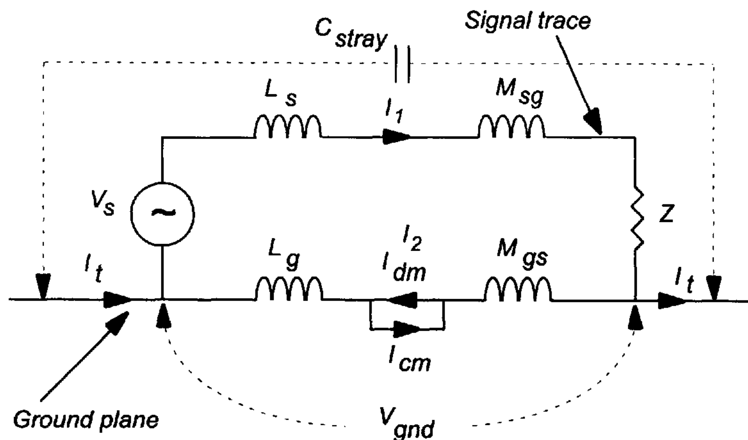
Conductor Separation	Common Length		
	1 inch	10 inches	20 inches
1/2 in. (1.25 cm)	3.23 nH	137.9 nH	344.9 nH
1/4 in. (0.63 cm)	6.12 nH	172.4 nH	414.7 nH
1/8 in. (0.32 cm)	9.32 nH	207.3 nH	484.8 nH
1/16 in. (0.16 cm)	12.7 nH	242.2 nH	555.0 nH

partial inductance between planes is maximized when the distance spacing is minimized. In addition to minimizing mutual partial inductance, interplane capacitance is increased, which is desirable for reasons detailed in Chapter 5. When we maximize the mutual partial inductance between the power and ground planes, RF signal currents that are observed within the power distribution plane are canceled out by equal and opposite RF return currents.

4.3.4 Image Plane Implementation and Concept

A solid plane can produce common-mode radiation. Figure 4.4 illustrates what an image plane structure looks like within a PCB assembly along with mutual partial inductance. In Fig. 4.4, the majority of the RF currents within the signal trace will return on the plane located directly below the signal trace. Within this return "image" structure, the RF return current will encounter a finite impedance (inductance). This return current produces a voltage gradient, which is referred to as ground-noise voltage. Ground-noise voltage will cause a portion of the signal current to flow through the distributed capacitance of the ground plane [6].

Common-mode currents, I_{cm}, are typically several orders of magnitude less than differential-mode currents, I_{dm}. However, common-mode currents (I_1 and I_{cm}) produce



The currents in the return path may also be identified as I2.

Figure 4.4 Schematic representation of a ground plane within a PCB.

higher emissions than those created by differential-mode currents (I_1 and I_{dm}). This is because common-mode RF current fields are additive, whereas differential-mode fields tend to cancel [6,7,8].

To reduce ground-noise voltage, it is necessary to increase the mutual partial inductance between the trace and its nearest image plane. Doing so provides an enhanced return path for signal return current to mirror image back to its source. We calculate ground-noise voltage V_{gnd} using Eq. (4.6):

$$V_{gnd} = L_g \frac{dI_2}{dt} - M_{gs} \frac{dI_1}{dt} \tag{4.6}$$

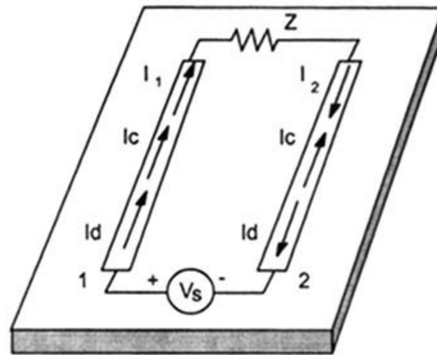
where in Fig. 4.4 and Eq. (4.6)

L_s = partial self-inductance of the signal trace
M_{sg} = partial mutual inductance between signal trace and ground plane
L_g = partial self-inductance of the ground plane
M_{gs} = partial mutual inductance between ground plane and signal trace
C_{stray} = distributed stray capacitance of the ground plane
V_{gnd} = ground plane noise voltage

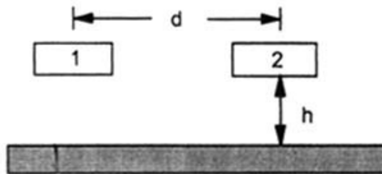
To reduce I_t currents, shown in Fig. 4.4, ground-noise voltage (V_{gnd}) must be reduced. This is best accomplished by reducing the distance spacing between the signal trace and ground plane. In most cases, there is a limitation on ground-noise reduction since the spacing between a signal plane and image plane must be at a specific, finite distance to maintain a constant impedance of the board for functionality reasons. Hence, there are limits to making the distance separation between the two planes any closer than physically manufacturable. Ground-noise voltage can also be reduced by providing an additional path for RF currents to flow through. This additional return path includes ground traces.

Since mutual partial inductance minimizes the creation of radiated RF currents, let's examine how differential-mode, I_{dm}, and common-mode, I_{cm}, currents are affected. Use of image planes significantly reduces these currents, as illustrated in Fig. 4.5. As discussed in Chapter 2, and as will be reaffirmed later in this chapter, differential-mode RF currents are canceled out when equal and opposite currents exist within the signal trace and RF return current path. If the cancellation of currents is not 100%, the amount of current that is left over becomes common mode. It is this common-mode current that functions as an excitation source and develops the majority of EMI that propagates from a product. This is because the leftover RF return current in the return path is added to the primary current in the signal path. To minimize common-mode currents, we must maximize the mutual partial inductance between signal trace and image plane to "capture the flux," hence canceling unwanted RF energy.

When an RF return plane or path is provided within a PCB assembly, optimal performance results when the return path is connected to a reference source. This reference source must be connected to the reference pins of components physically located at both the source and load ends of the transmission line [11]. For TTL and CMOS, the power and ground pins inside a component die (wafer) are connected to a reference source, power and ground. Certain geometrical factors impact these connections. Only when the RF return path is connected to the power and ground pins of a component will a real



Circuit model-2 traces over a plane



Cross section of circuit

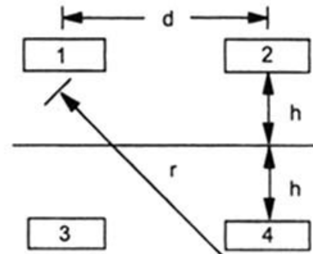
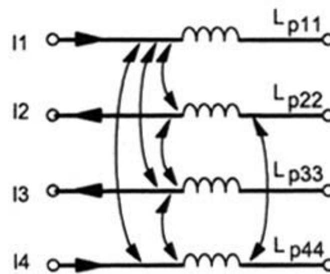


Image traces substituted for image plane



Partial inductance model of the circuit
I3 is the image of I1, while I4 is the image of I2

Figure 4.5 Use of image plane related to partial inductance. (*Source: Introduction to Electromagnetic Compatibility*, Clayton Paul © 1992. Reprinted by permission of John Wiley & Sons, Inc.)

image plane exist. An isolated solid sheet of copper foil (a layer within the PCB structure), that is not connected to any reference source, will not work as an image plane under any condition. How is the return current going to get back to the source if the return path is broken?

An image plane containing differential-mode voltage and currents will produce common-mode currents. Depending on the distance spacing between the trace and image plane, differential-mode currents will be reduced by increased mutual partial inductance. How much differential-mode current travels in the planes is dependent on the minimized distance separation between the two conductive surfaces.

Image planes function because digital components are connected to a power and ground plane structure. The ground connection internal to the device, connected to the ground plane, provides for the reference to exist. This connection internal to the component package is what makes image planes work.

When the image plane is removed, a phantom image return path is created between a trace and plane. The RF image associated with these currents will cancel out along with a reduction of radiated energy because each trace pair (the original current and its image) is closely spaced. For an image plane to perform as desired, the plane should be infinite in size and not contain disruptions, slots, or cuts [2].

4.4 GROUND AND SIGNAL LOOPS (NOT EDDY CURRENTS)

Loops are a major contributor to the propagation of RF energy. RF current will attempt to return to its source through any path or medium: components, wire harnesses, ground planes, adjacent traces, and so forth. RF current is always created between a source and load due to the return path, where there is a voltage potential difference between these two points. Path inductance, however, causes magnetic coupling of RF currents to occur between a source and victim circuit, thus increasing RF losses in the path.

One of the most important design considerations for EMI suppression on a PCB is ground or signal return loop control. An analysis must be made for each and every ground stitch connection (mechanical securement between the PCB and chassis ground) related to RF currents generated from RF noisy electrical circuits. High-speed logic components and oscillators should always be located as close as possible to a ground stitch connection to minimize the formation of loops in the form of eddy currents to the chassis ground. This design requirement will now be examined in detail.

An example of loops that could occur in a computer with adapter cards and single-point grounding is shown in Fig. 4.6. As observed, an excessive signal-return loop area is present. Each loop will create a distinct electromagnetic field and spectra. RF currents will create an electromagnetic radiated field at a unique frequency, depending on the physical size of the loop. Containment measures must now be used to keep these RF currents from coupling to other circuits or radiating to the external environment as EMI. Internally generated RF loop currents are to be avoided.

To expand on the concept of loop area shown in Fig. 4.6, we have Fig. 4.7 which shows the loop area between two components.

To reiterate the importance of minimizing loops within a PCB structure, we examine the effects a loop has in creating EMI. This concept is important in understanding how

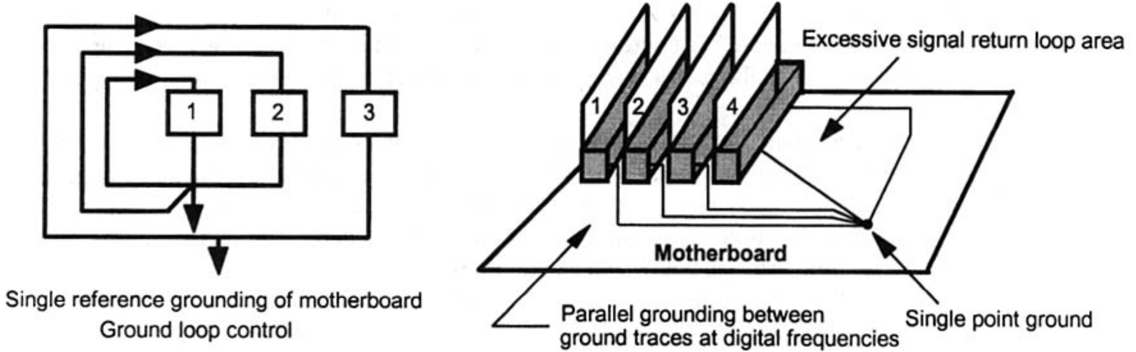


Figure 4.6 Ground loops within a PCB assembly.

RF energy is created within a PCB. (For a discussion of how loops create EMI within components, refer back to Chapter 3, Section 3.4.)

With RF energy concentrated within a loop structure, how can this energy be removed if a return path is not provided for the RF current? A ground connection to chassis ground or a 0V reference source assists in removing this undesirable accumulation of RF current, also identified as loop area control.

4.4.1 Loop Area Control

Figure 4.8 illustrates how various loop areas are created within a PCB structure using both a single- and double-sided assembly and a multilayer stackup. The electromagnetic field induced into a loop structure by a magnetic field can be represented as a voltage source within that loop. This voltage source is proportional to the total area of the loop. To minimize magnetic field coupling, we must minimize the loop area. The electric field pickup reception is also dependent on the loop area forming the receive antenna.

When an electric field is present, a current source is created between a two-conductor system (power and ground). Electric fields do not couple line-to-line but rather line-to-ground, including common-mode currents. Therefore, the only loop valid for this mode of coupling is the conductor to chassis coupling. Of course, the H-field that accompanies the E-field also couples into wiring loops (line-to-line and line-to-ground).

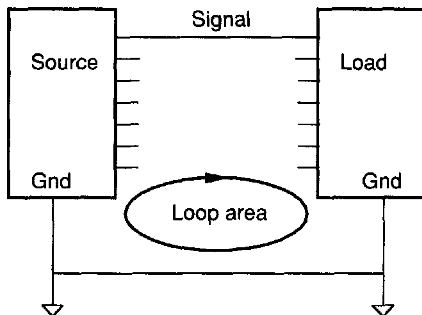


Figure 4.7 Loop area between components.

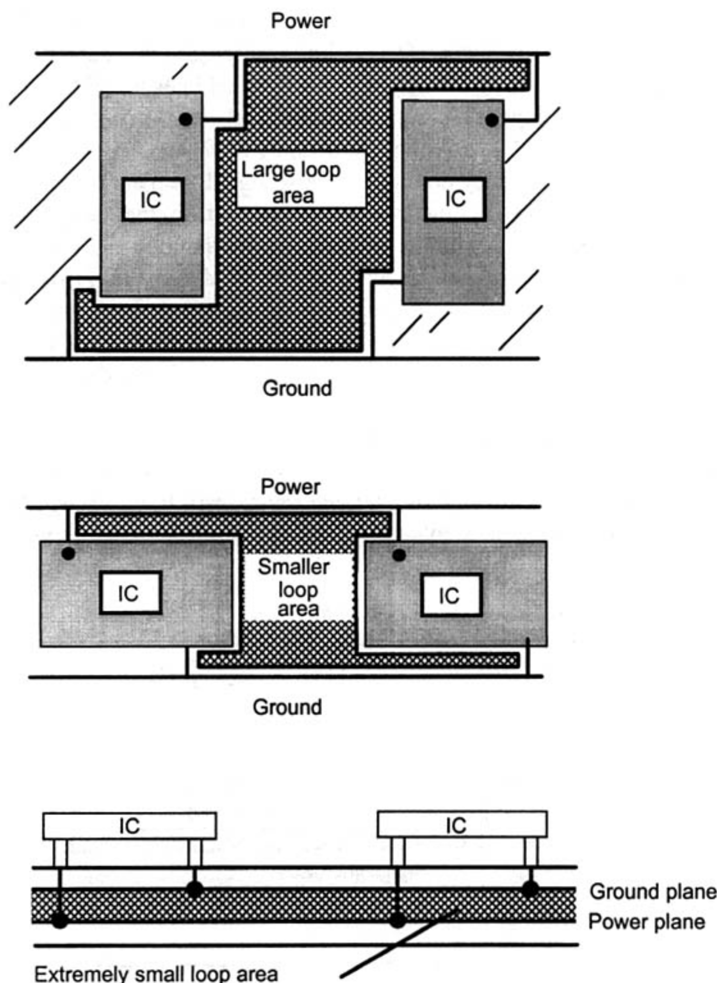


Figure 4.8 Loop areas that exist within a PCB. (*Source: Introduction to Electromagnetic Compatibility*, Clayton Paul © 1992. Reprinted by permission of John Wiley & Sons, Inc.)

It is generally overlooked during a PCB layout that loop areas may be created between the power and 0V reference structure. Figure 4.8 illustrates a poor layout in the top drawing that may be performed by a PCB designer because it is easy to create using computer CAD software. This software permits easy routing of busses between components located next to each other. With a large loop area on the PCB, susceptibility to the pickup of ESD-induced (or other) fields can occur. A multilayer stackup minimizes the potential of ESD disruption, in addition to minimizing creation of a magnetic field that will be radiated into free space.

Using power and ground planes helps reduce the inductance of the power distribution system. Lowering the characteristic impedance of the power distribution system reduces the voltage drop across the board. With less voltage drop, ground bounce potential is minimized. In addition to lowering the characteristic impedance of the structure, we in-

crease the capacitance between the two parallel planes. This capacitance reduces the effects of any induced voltages. (Decoupling is discussed in Chapter 5.)

Large loop areas may be created when signal lines travel between components. This is seen in Fig. 4.9. Signal lines are generally forgotten when analyzing why a PCB has radiated emission problems. Although we may have high signal integrity (time domain), EMI still exists (frequency domain) because signal loop areas create more problems than those of the power distribution system, especially from the viewpoint of ESD. This is because an ESD event may be injected directly into the loop and into the input pins of components. To mitigate the consequences of a harmful disruption from an ESD event, reducing loop area is the easiest technique to use. A power and ground plane distribution network provides a low-impedance path that allows transfer of the ESD energy into a 0V return reference plane. After all, loops are loops, and if they can emit fields, then they also can receive fields.

In addition to reducing ground-noise voltage, an image plane prevents RF ground loops from being developed because RF currents tightly couple themselves to their source trace without having to find an alternate return path home. When loop control is maximized, flux cancellation is enhanced. *This is one of the most important concepts of sup-*

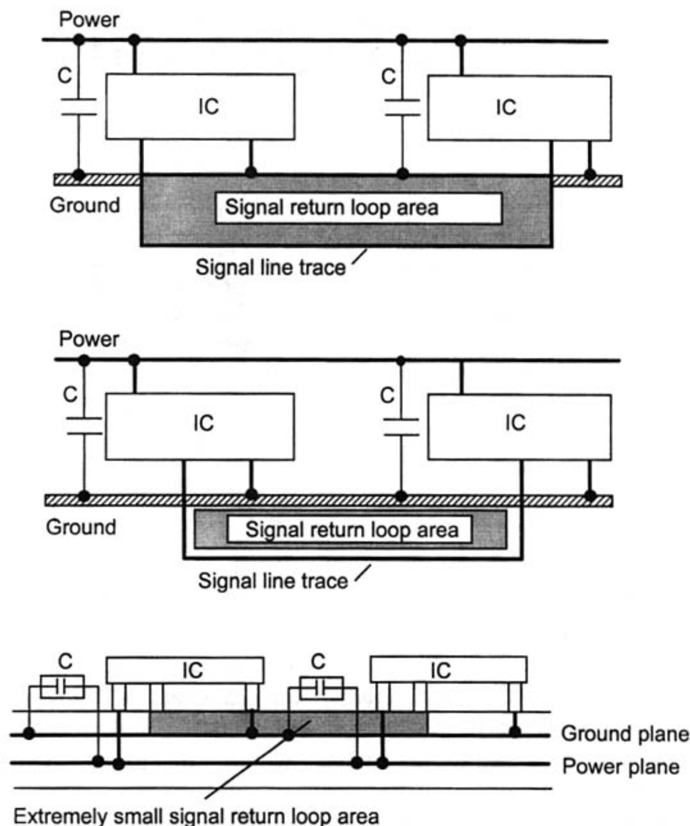


Figure 4.9 Reduction in loop areas that exist within a PCB. (*Source: Introduction to Electromagnetic Compatibility*, Clayton Paul © 1992. Reprinted by permission of John Wiley & Sons, Inc.)

pression of RF currents at the PCB level. Proper placement of an image plane adjacent to each and every signal plane removes common-mode RF currents created by signal traces coupling to its return path. Image planes carry large amounts of RF currents that must be sourced to ground or 0V reference potential. To help remove excess RF potentials and uncontrolled eddy currents, all ground and chassis planes, (if 0V reference is used), can be connected to chassis ground through a low-impedance ground stitch connection [1,6,9,10,11].

We now examine optimal spacings for creating a low-impedance ground stitch connection to remove RF currents into the 0V reference or return structure.

4.5 ASPECT RATIO—DISTANCE BETWEEN GROUND CONNECTIONS

Aspect ratio is a term commonly used in the television industry to refer to the ratio of frame width to frame height. The term also refers to the ratio of a longer dimension to a shorter one. With these definitions, how does aspect ratio relate to EMC? When providing ground stitch connections in a PCB using multipoint grounding to a metallic structure, we must concern ourselves with the distance spacing in all directions of the ground stitch location.

RF currents that exist within the power and ground plane structure will tend to couple to other components, cables, peripherals, or other electronic items within the assembly. This undesirable coupling may cause improper operation, functional signal degradation, or EMI. When using multipoint grounding to a metal chassis, and providing a third wire ground connection to the AC mains, RF ground loops become a major design concern. This configuration is typical with personal computers. (An example of a single-point ground connection for a personal computer was shown in Fig. 4.6).

Because the edge rate of components is becoming faster, multipoint grounding is becoming a mandatory requirement, especially when I/O interconnects are provided in the design. Once an interconnect cable is attached to a connector, the unit at the other end of the interconnect may provide an RF path to a third wire AC ground mains connection (if provided) to its respective power source (e.g., the negative terminal of a battery) or simply through distributive radiation RF impedance to earth or through free space. A large ground loop on the I/O interconnect can cause undesirable levels of radiated common-mode energy. How can we minimize loops that may occur within a PCB structure? The easiest way is to design the board with many ground stitch locations to chassis ground, if chassis ground is provided. The question that now exists is, how far apart do we make the ground connections from each other, assuming the design has the option of specifying this design requirement?

The distance spacing between ground stitch locations should not exceed $\lambda/20$ of the highest frequency of concern, not just the primary frequency (including harmonics). If many high-bandwidth components are used, multiple ground stitch locations are typically provided. If the unit is a slow edge rate device, connections to chassis ground may be minimized, or the distance between ground locations increased.

For example, $\lambda/20$ of a 64-MHz oscillator is 23.4 cm (9.2 in.). If the straight-line distance between any two ground stitch locations to a 0V reference (in either the x- and/or y-axis) is greater than 9.2 inches, then a potential efficient RF loop exists. This loop could

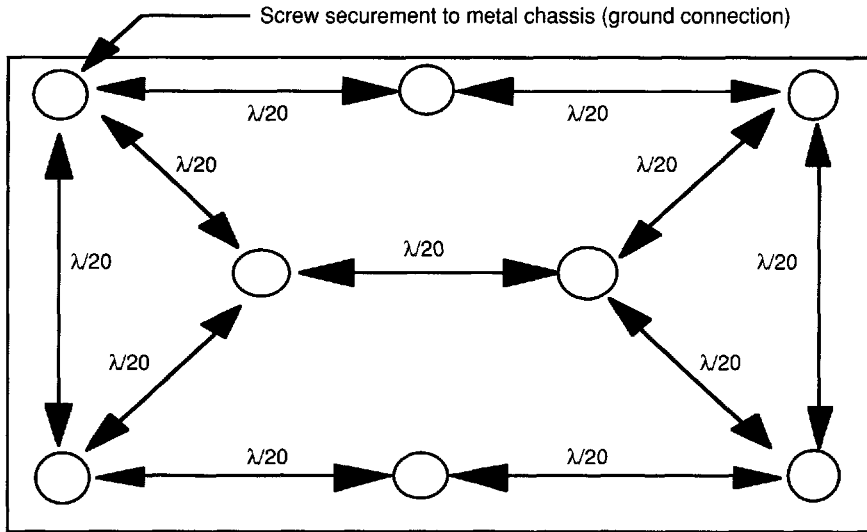


Figure 4.10 Aspect ratio.

be the source of RF energy propagation, which could cause noncompliance with international EMI emission limits. Unless other design measures are implemented, suppression of RF currents caused by poor loop control is not possible and containment measures (e.g., sheet metal) must be implemented. Sheet metal is an expensive Band-Aid that might not even work for RF containment. An example of *aspect ratio* is given in Fig. 4.10 [1].

Proper placement of components is critical in any PCB layout. Most designs incorporate functional subsections or areas (by logical function). Grouping each functional area adjacent to other subsections minimizes signal trace lengths and reflections, and makes trace routing easier along with maintaining signal integrity. Vias should be avoided where possible, for vias increase the inductance of the trace by approximately 1 to 3 nH each. Figure 4.11 illustrates the functional grouping of subsections (or areas) using a stand-alone CPU-motherboard as an example.

Extensive use of chassis ground stitch connections is also observed in Fig. 4.11. High-frequency designs (fast edge rates) develop very high spectral frequency profiles and require new methodologies for bonding ground plane(s) to chassis ground. Use of these multipoint grounding points effectively partitions common-mode eddy currents emanating from various segments on the design from coupling into other segments. Products with clocks above 50 MHz generally require frequent ground stitch connections to chassis ground to minimize the effects of common-mode currents and ground loops present between functional sections. At least four ground points surround each subsection. These ground points illustrate best case implementation of aspect ratio. Note that a chassis bond connection (screw or equivalent) is located on both ends of the DC power connector (Item P) used for powering external peripheral devices. RF noise generated on either the PCB or peripheral power subsystem must be AC shunted to chassis ground by parallel bypass capacitors. These capacitors minimize power-supply-generated RF currents from coupling into signal or data lines. Removal of RF currents on the power connector will

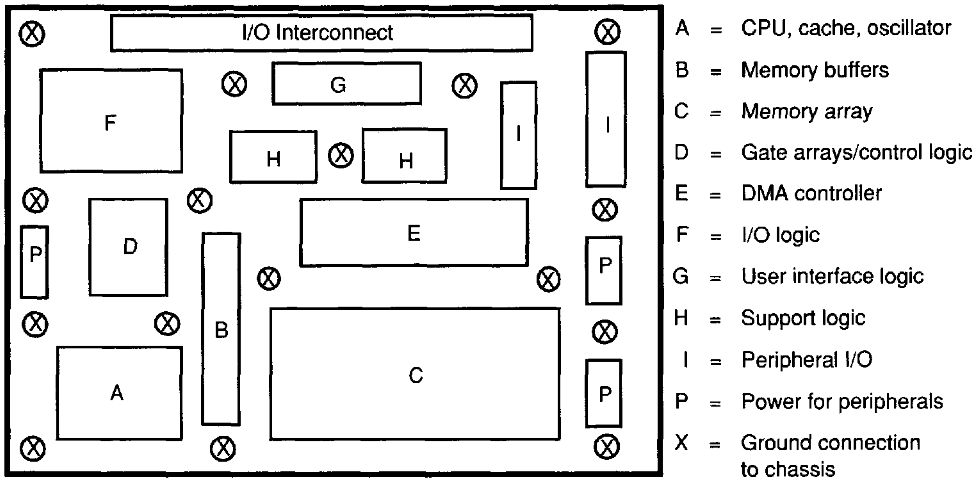


Figure 4.11 Multipoint grounding—implementation of aspect ratio.

optimize signal quality for data transfer between the motherboard and external peripheral devices in addition to reducing emissions [1,10].

Most PCBs can be arranged to consist of functional subsections or areas. A typical personal computer contains the following: CPU, memory, ASICs, I/O, bus interface, system controllers, PCI/IDE bus, SCSI bus, peripheral interface (fixed and floppy disk drives), and other components. Associated with each subsection are different bandwidths of RF energy. Different logic families generate RF energy across the frequency spectrum. The higher the frequency component of the signal, the greater the bandwidth of RF spectral energy. RF energy is generated from the higher frequency components and the time-variant edges of digital and analog signals. Clock signals are the greatest contributors to the generation of RF energy. This is because clocks are periodic signals providing coherent spectral distribution (50% duty cycle) and generally have fast edge rates.

To prevent coupling between different bandwidth areas, functional partitioning is used. Partitioning refers to the physical separation between functional sections. Partitioning is product specific and may be achieved using separate PCBs, isolation, topology layout variations, or other creative means.

Proper partitioning allows for optimal functionality, ease of routing traces, and minimization of trace lengths. It also permits smaller loops to exist while optimizing signal quality. The design engineer will specify which components are associated with each functional subsection. Use the information provided by the component manufacturer to optimize component placement prior to routing any traces.

4.6 IMAGE PLANES

An image plane is a layer of copper (voltage plane, ground plane, or chassis plane) internal to a PCB physically adjacent to a circuit or signal plane. Image planes are used to provide a low-impedance path for RF signal currents to return to their source (flux return), thus completing

the RF current return path and reducing EMI emissions. The term *image plane* was popularized by the German, Ott, and Paul [7], and is now used as industry standard terminology.

RF currents must return to their source one way or another. This return path may be a mirror image of its original trace route, through another trace located in the near vicinity, a power plane, a ground plane, or a chassis plane. RF currents will capacitively (or by mutual inductance) couple themselves to a conductive medium (e.g., low-impedance path such as the copper that makes up a trace or plane). If this coupling is not 100%, common-mode RF currents can be propagated between traces and their nearest image plane. An image plane internal to the PCB reduces ground-noise voltage in addition to allowing RF currents to return to their source (mirror image) in a tightly coupled (nearly 100%) manner. Tight coupling provides for flux cancellation, which is another reason for use of a solid plane. Solid planes also prevent common-mode RF current from being generated in the PCB by those traces rich in RF energy.

Figure 4.12 illustrates the concept and use of an image plane and what happens when tight coupling does not exist between the signal trace and 0V reference (ground) plane. The voltage developed across a return conductor is referred to as ground drop. The lower the value of ground drop between two points on a PCB return structure, the lower the radiated emissions from the PCB.

One concern related to image planes involves the concept of skin effect. *Skin effect* refers to current flow that resides in the first skin depth of the material at high frequencies. Current does not and cannot flow in the center of traces and wires, and is predominately observed on the outer surface of the conductive media. Different materials have different skin depth values. The skin depth of copper is extremely small, above 30 MHz. Typically, this is observed at $6.6 * 10^{-6}$ (0.0017 mm) of an inch at 100 MHz. RF current present on a ground plane cannot penetrate 1 oz. 0.0014″ (0.036 mm) thick copper. As a result, both common-mode and differential-mode currents flow only on the top (skin) layer of the plane. No significant current flows internal to the image plane or on its bottom. Placing an additional image plane beneath this ground plane would not provide additional EMI reduction. If the second plane is at voltage potential (the primary plane at ground potential), a decoupling capacitor will be created. These two planes can now be used as both a decoupling capacitor and dual image planes but with some concern regarding flux cancellation (see Section 2.1) [6].

With regard to image plane theory, the material presented herein is based on a finite-sized plane, typical of all PCBs. Image planes cannot be relied on for reducing cur-

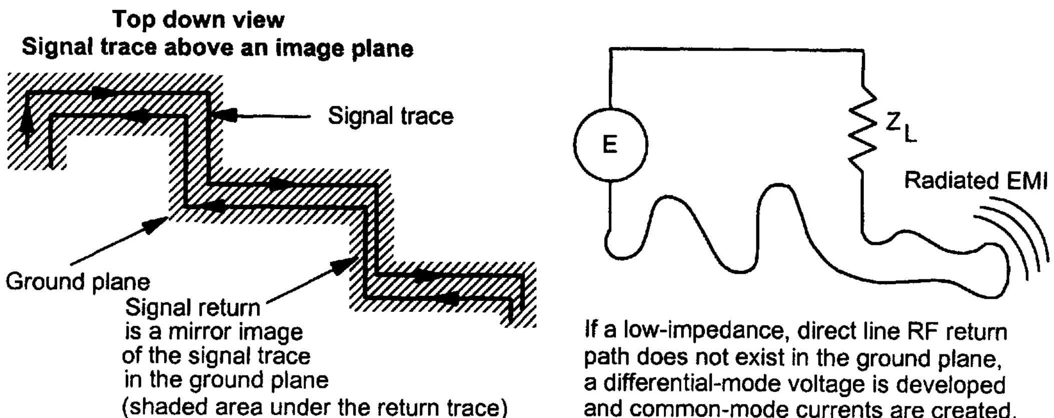


Figure 4.12 Image plane concept.

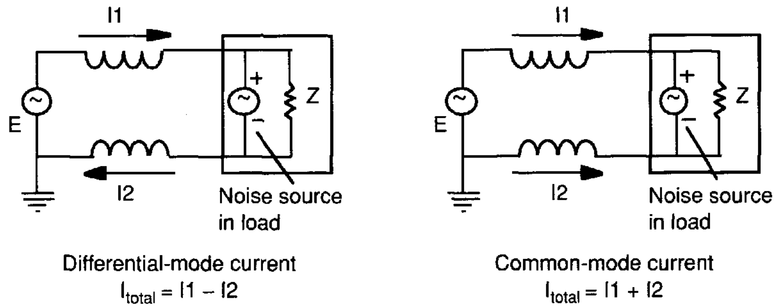


Figure 4.13 *Common-mode and differential-mode currents.*

rents on I/O cables because approximating finite-sized conductive planes is not always valid. When I/O cables are provided, the dimensions of the configuration and source impedance are important parameters to remember [12].

An example of common-mode and differential-mode currents is shown in Fig. 4.13. The measured *E*-field of the differential-mode current will be the difference of I1 and I2. This difference is negligible because of a 180 degree phase difference. The measured *E*-field due to common-mode current is the sum of I1 and I2, which could be substantial due to the summing effect. Common-mode currents are always much smaller than differential-mode currents.

If "three" internal signal planes (stripline configuration) are physically adjacent to each other in a multilayer board stackup, the middle signal plane, (e.g., the one not adjacent to a reference plane), will couple its RF currents to the other two signal planes, thus causing RF energy to be transferred (by mutual inductance and capacitive coupling) to the other two planes. After this first level of coupling, a second level of coupling occurs to the real image or RF return plane. This coupling can cause significant crosstalk to occur, which may include nonfunctionality. Flux cancellation performance is sometimes enhanced when the signal routing layer is adjacent to a ground plane, but not to a power plane, as described throughout this chapter.

4.7 IMAGE PLANE VIOLATIONS

For an image plane to be effective, all signal traces must be located adjacent to a solid plane and must not cross an isolated area of copper. Exceptions can occur using special trace routing techniques. If a signal trace, or even a power trace (e.g., +12 V trace in a +5 V power plane) is routed within a solid plane, this solid plane becomes fragmented (split) into smaller parts. Provisions have now been made for a ground or RF signal return loop to be developed for RF return currents that are observed on the adjacent layer across this violation. This RF loop occurs by not allowing RF current present in a signal trace to seek a straight-line, low-impedance path back to its source.

Figure 4.14 illustrates a violation of the image plane concept. These planes can now no longer function as a solid 0V reference to remove common-mode RF currents. The losses across the plane segmentations may actually produce RF fields. Vias placed in an image plane do not degrade the imaging capabilities of the plane, except where ground slots are provided as discussed next.

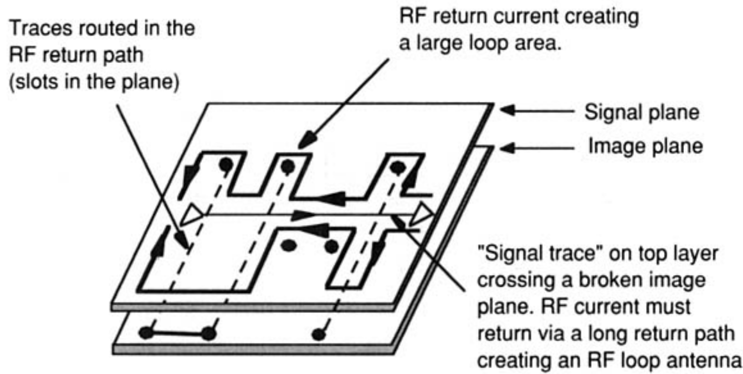


Figure 4.14 Image plane violation with traces.

Another area of concern that lies with ground plane discontinuities is the use of through-hole components. Excessive use of through-holes in a power or ground plane creates the Swiss Cheese Syndrome [5]. The copper area in the plane is reduced because many holes overlap (oversized through-holes), leaving large areas of discontinuities. This effect is observed in Fig. 4.15. The return current flows on the image plane around the through-hole pattern, while the signal trace is on a direct line route across the discontinuity. As seen in Fig. 4.15 [1], the return currents in the ground plane must travel around slots or holes. As a result, extra trace length is present for return currents that must flow around these slots in the image plane. This extra trace length adds more inductance in the signal return trace, $E = L(dI/dt)$. With additional inductance in the return path, there is reduced differential-mode coupling between signal trace and the RF current return path (less flux cancellation). For through-hole components that have a space between pins (nonoversized holes), optimal reduction of signal and return current is achieved through less inductance in the signal return path and the existence of the solid plane.

If a signal trace is routed "around" the through-hole discontinuities (not shown in the left side of Fig. 4.15), a constant image plane (RF return path) would be maintained along the entire signal route. The same is true for the right side of Fig. 4.15. There are no ground plane discontinuities and hence, shorter trace length. The longer trace route on the left side of the figure adds more trace length inductance $E = L(dI/dt)$. This length can cause reflections that affect signal integrity and functionality, and may also create a loop for RF current. Problems arise when the signal trace travels through the middle of slotted holes in the PCB (in an attempt to minimize trace length routing) when a solid plane does not exist in this oversized through-hole area. When routing traces between through-hole components, use of the *3-W Rule* (defined later in this chapter) must be maintained between the trace and through-hole clearance area.

Generally, a slot in a printed circuit board with through-hole components will not cause RF problems for the majority of signal traces that route between the through-hole device leads. However, it can cause electromagnetic fields to be developed around the holes. For high-speed, high-threat[2] signals, alternative methods of routing traces between

[2]High-threat refers to high-bandwidth, RF spectral components that propagates as an electromagnetic field down a transition line or trace. These signals include clocks, video, address lines, analog circuits, and the like. All of these highly sensitive circuits may either radiate RF energy, or be susceptible to an externally induced field disturbance, requiring a mandatory, low-impedance RF return path to complete the closed-loop circuit.

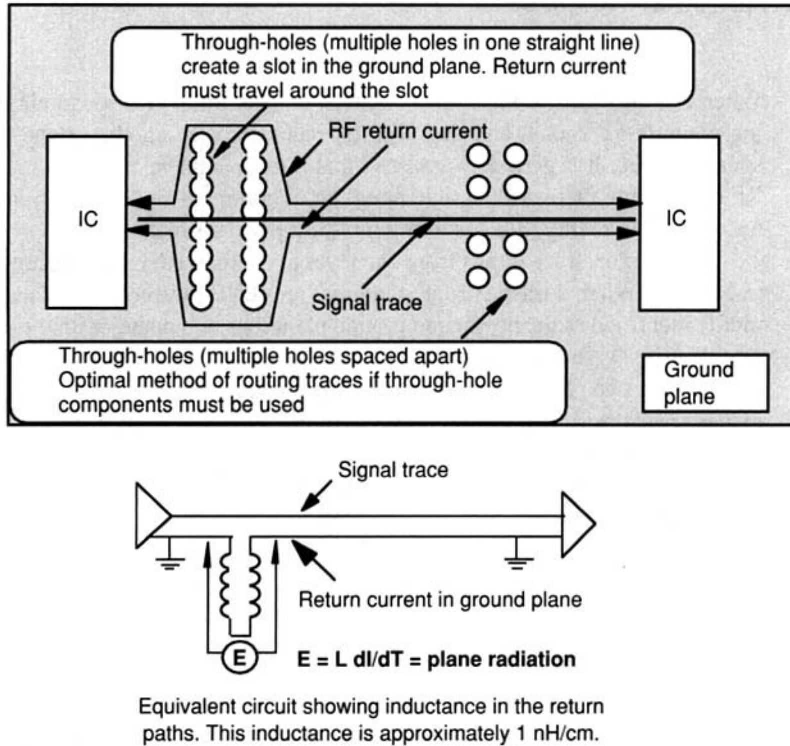


Figure 4.15 Ground loops when using through-hole components (slots in the plane).

through-hole component leads must be devised. For those applications where a trace must traverse across a slot or partition within the PCB assembly, Fig. 4.16 provides a design technique which allows RF return current to jump the slots using capacitors.

Capacitors provide an AC shunt for RF currents to traverse across a moat or slot. A significant performance improvement of up to 20 dB has been observed during functional testing. The capacitor must be chosen for optimal performance based on the self-resonant frequency of the component trace signal. It is cautioned, however, that this technique may result in reactance-based phase shifts in the current relationships between the traces and their images, impacting the magnitude of flux cancellation or minimization.

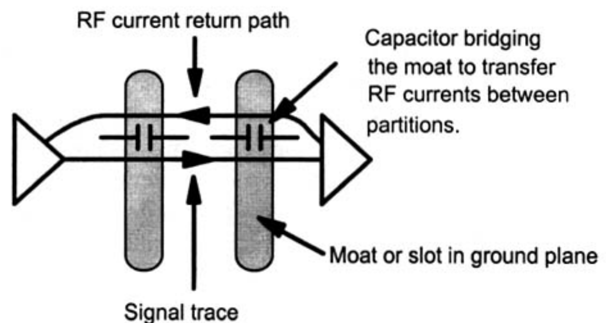


Figure 4.16 Crossing a moat and allowing RF return current to pass.

4.8 LAYER JUMPING—USE OF VIAS

When routing clock or high-threat signals, it is common practice to via the trace to a routing plane (e.g., *x*-axis) and then via this same trace to another plane (e.g., *y*-axis) from source to load. It is generally assumed that if each and every trace is routed adjacent to an RF return path, there will be tight coupling of common-mode RF currents along the entire trace route. In reality, this assumption is partially incorrect.

As a signal trace jumps from one layer to another, RF return current should follow the trace route. When a trace is routed internal to a PCB between two planar structures, commonly identified as the power and ground planes, or two planes with the same potential, the return current is shared between these two planes. The only time the return current can jump between the two planes is at a location where decoupling capacitors are positioned. If both planes are at the same potential (e.g., 0V reference) the RF return current jump will occur at a via connecting both planes to a device or component assigned to that via.

When a jump is made from a horizontal to a vertical layer, the RF return current *cannot* fully make this jump. This is because a discontinuity is placed in the trace route by the via. The return current must now find an alternate low-inductance (impedance) path to complete its route. This alternate path may not exist in a position that is immediately adjacent to the location of the via used for the jump. As a result, RF currents on the signal trace can couple to other circuits and pose problems as both crosstalk and EMI. Use of vias in a trace route will always create a concern in any high-speed, high-technology product.

To minimize development of EMI and crosstalk due to layer jumping, the following design techniques have been found to be effective:

1. Route all clock and high-threat signal traces on only one routing layer as the initial approach concept. This means that both *x*- and *y*-axis routes are in the same plane. (*Note:* This technique is likely to be rejected by the PCB designer as being unacceptable because it makes autorouting of the board nearly impossible.)
2. Verify that a solid RF return path is adjacent to the routing layer, with no discontinuities in the route created by use of vias or jumping the trace to another routing plane.

If a via must be used for routing a sensitive trace (high-threat or clock signal) between the horizontal and vertical routing layer, the designer should incorporate ground vias at "each and every" via location where the signal axis jumps are executed. The ground via is always at 0V potential.

A ground via is a via that is placed directly adjacent to each signal route via from a horizontal to a vertical routing plane. Ground vias can be used only when there are more than one 0V reference planes internal to the PCB. This via is connected to all ground planes (0V reference) in the board that serves as the RF return path for the signal jump currents. This via essentially ties the 0V reference planes together adjacent and parallel to this signal trace location. When using two ground vias per signal trace via, a continuous RF return path will now exist for RF return current throughout its entire trace route. This

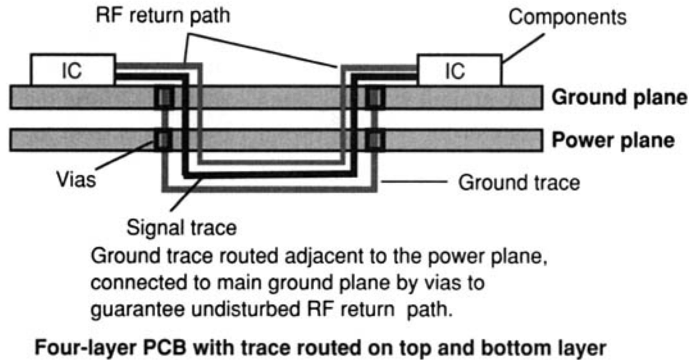


Figure 4.17 Routing a ground trace to assure a compete RF return path exists.

ground via will maintain a constant RF return path (through use of image planes) located 100% adjacent to a signal route.[3]

What happens when only one 0V reference (ground) plane is provided and the alternate plane is at voltage potential as commonly found with a four-layer PCB stackup assignment. To maintain a constant return path for RF currents, the 0V reference plane should be allowed to act as the primary return path. The signal trace must be routed against this 0V reference plane. When the trace must route against the power plane, use of a *ground trace* is required, with the vias at both ends of the ground trace routed parallel to the signal trace tied to the 0V reference plane. Using this configuration, we can now maintain a constant RF return path (see Fig. 4.17).

How can we minimize use of ground vias when layer jumping is mandatory. In a properly designed PCB, the first routed traces will be clock signals, "manually routed." Since much freedom is permitted in routing the first few traces by the PCB designer (e.g.,

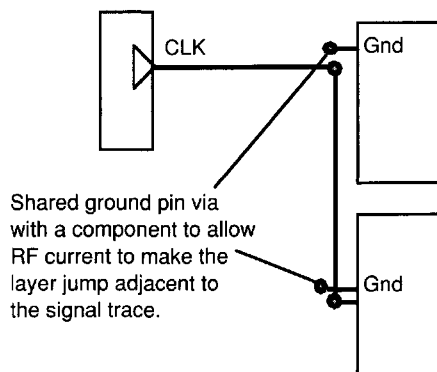


Figure 4.18 How to route the first trace within a PCB.

[3]Use of ground vias was first identified and presented to industry by W. Michael King. Ground vias are also described in [1] and [13].

all clocks and high-threat signals), the designer can route the board using the shortest trace distance routing possible (shortest Manhattan length), making the layer jump adjacent to the *ground pin via* of any component. This layer jump will co-share this component's ground via. The ground via being referenced will perform the function of providing 0V reference to a component while allowing RF return current to make a layer jump as detailed in Fig. 4.18.

4.9 SPLIT PLANES

When multilayer PCB assemblies are used, the power and ground planes are sometimes split on the same plane. An example is separation of analog circuitry from digital logic, isolation of I/O interconnects (detailed under Partitioning in Section 4.10), separation of voltage reference areas (e.g., +5V section from a –48V partition), component isolation, and the need to force RF return currents to travel a designated route through the PCB. This designated RF return path can be likened to a road map. We travel only on the roads provided in a predefined manner. Why not cause RF return currents to do the same thing, travel a predefined road or path?

One of the PCB designer's primary design and layout concerns is to guarantee that overlaps on a split plane do not occur. If an overlap on a plane is present, a finite-sized capacitor will be created between the overlapping plane segments as seen in Fig. 4.19. This finite-sized capacitor, C1, will allow RF energy (which is an AC waveform) to traverse from one plane (e.g., a noisy plane) to a separate, quiet, or isolated plane. The DC voltage potentials of the planes remain intact due to passing the DC voltage from one isolated area to another through filters.

If additional high-frequency isolation is required, we can isolate one plane (power) or both potentials (power and ground) with ferrite bead-on-leads, not inductors. We must be careful with this technique. If both planes contain high-frequency RF noise, it is usu-

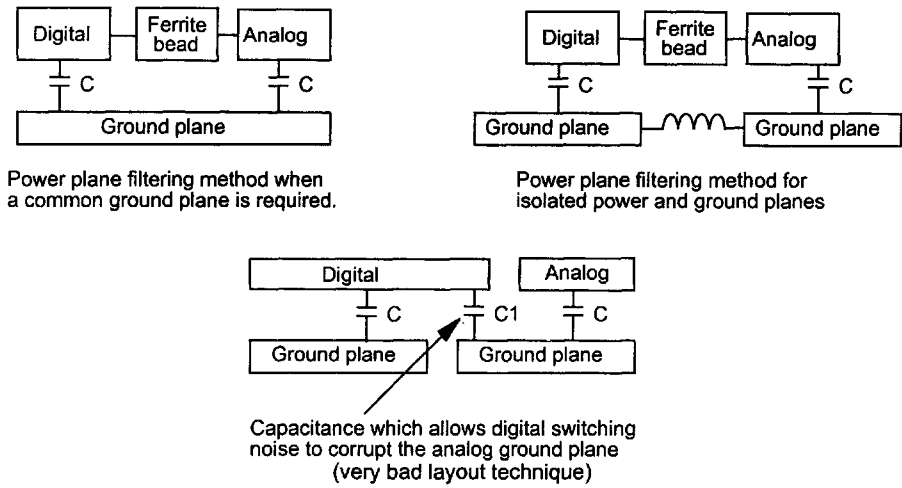


Figure 4.19 Variations on split plane configurations.

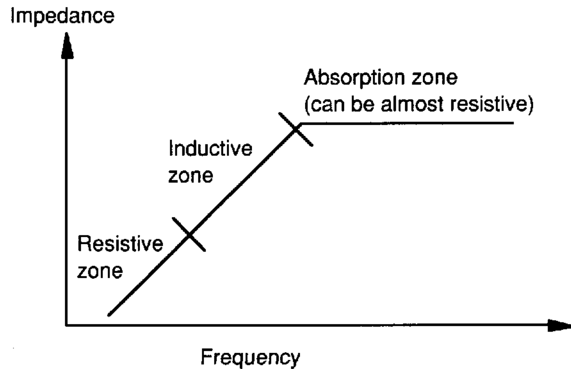


Figure 4.20 Ferrite material performance characteristics.

ally better to isolate both planes. If a common digital-to-analog ground reference is required, and analog power is needed for device operation, the ferrite bead-on-lead should be placed only across the power plane partition.

When a split plane[4] occurs, the common ground plane must be located "directly" under the discrete filter components. All signal traces must then be routed adjacent to this solid ground plane under the filter in an area identified as a bridge. Bridges are discussed later in this chapter. The advantage of this design technique is to maintain the integrity of the 0V reference (image) plane necessary for high-frequency EMI control and to provide an optimal RF return path from load to source.

The reason not to use inductors is easy to visualize and is best shown in Fig. 4.20. Ferrite material has practically zero impedance (or DC resistance) at DC voltage or signal transition levels, including very low-frequency signals. It is essentially transparent to DC voltage and acts as a small inductor or resistor having little effect at low frequencies. At higher frequencies, RF currents are created within the power distribution structure, and the resistive characteristics of the ferrite material dominate, providing a high impedance to the circuit. The high impedance of the material is present until the ferromagnetic properties reaches a predefined operating frequency, where the ferromagnetic material ceases to function as desired. Basically, a ferrite component is a large RF resistor that keeps RF energy from traveling between two isolated locations. An inductor, on the other hand, has a large inductive value with an inductive reactance, $j\omega L$. Inductive reactance is exactly what we *do not want* within a transmission path. Parasitic capacitance will exist between the two terminals of the inductor, plus the capacitance between the inductor windings and 0V reference. With an L and C component present within the device, a resonant circuit is created. Depending on the values of L and C, we may be allowing RF currents, at a particular frequency, to pass between the isolated areas. Once the RF currents pass through the circuit, these RF currents are now allowed to cause harmful disruption to functional circuits, which were supposed to be operated from clean filtered power.

If an isolated plane contains only low-frequency circuits (analog) and another isolated plane has high-frequency (digital) switching currents, it sometimes becomes mandatory to isolate both the power and ground planes between these two areas with ferrites de-

[4]A split plane refers to a solid copper structure that has been segmented into two or more partitions. An example of this split is easily seen in Fig. 4.19. The top left circuit has a continuous ground plane. The other two circuits have been partitioned into separate functional ground planes: analog and digital. One split is connected by a ferrite bead, the other totally isolated.

pending on the device's function and the manufacturer's requirements for power and/or plane isolation. This isolation technique is required only if no high-frequency energy can be allowed to pass between the two areas. If both areas contain only low-frequency components and there are no high-frequency RF energy threats (high-edge rate switching noise), ferrite components are not required. A single-point connection is permissible between the two planes.

4.10 PARTITIONING

Designing I/O circuits involves two basic areas of concern: functional subsystems, and quiet areas. Each is briefly discussed separately below, with more detail presented herein.

4.10.1 Functional Subsystems

Each I/O should be considered as a different subsection on a PCB, for each may be unique in its particular application. To prevent RF coupling between subsystems, partitioning may be required. A functional subsystem is a group of components along with their respective support circuitry. Locating components close to each other minimizes trace length routing and optimizes functional performance. Every hardware and PCB designer generally tries to group components together, but, for various reasons, it is sometimes impractical to do so. I/O subsystems must still be treated differently during layout than any other section of the PCB. This is generally done through layout partitioning.

Layout partitioning enhances signal quality and functional integrity by preventing high-bandwidth emitters (e.g., backplane interconnect, video devices, data interfaces, Ethernet controllers, Small Computer System Interface [SCSI] devices, and central processing units [CPUs]) from corrupting serial, parallel, video, audio, asynchronous/synchronous ports, floppy controller, front panel console displays, local area and wide area networks controllers, and so on. Each I/O subsystem must be conceived, designed, and treated as if the subsystems were separate PCBs.

4.10.2 Quiet Areas

Quiet areas are sections that are physically isolated from digital circuitry, analog circuitry, and power and ground planes. This isolation prevents noise sources located elsewhere on the PCB from corrupting susceptible circuits. An example is power plane noise from the digital section entering the power pins of analog devices (analog section), audio components (audio section), I/O filters, interconnects, and so on, detailed in Fig. 4.21 [1].

Each and every I/O port (or section) must have a partitioned (quiet) ground/power plane. Lower-frequency I/O ports may be bypassed with high-frequency capacitors (usually 470 pF to 1000 pF) located near the connectors.

Trace routing on the PCB must still be controlled to avoid recoupling RF currents into the cable shield. A clean (quiet) ground must be located at the point where cables leave the system. Both power and ground planes must be treated equally, for both planes act as a path for RF return currents. RF return currents from switching devices to I/O con-

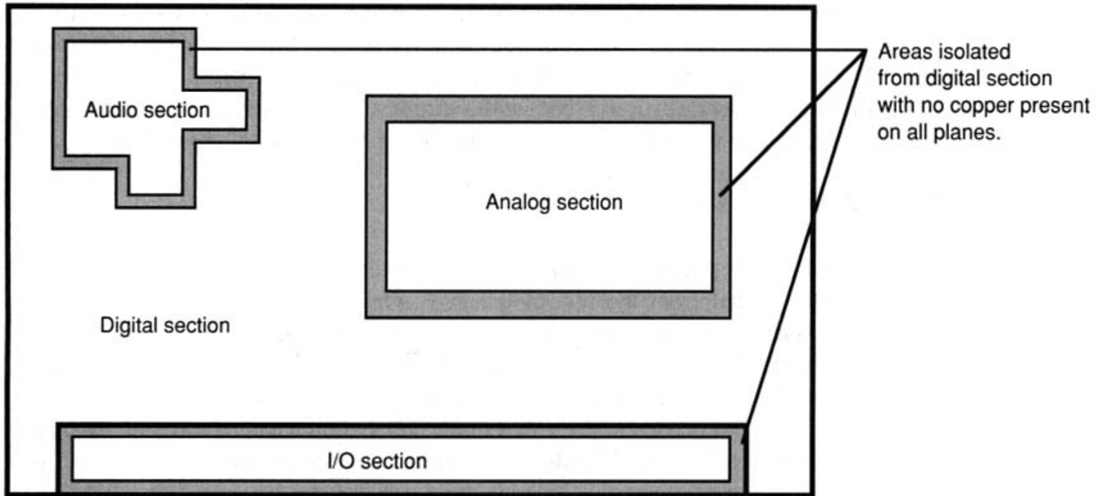


Figure 4.21 Quiet areas.

trol circuitry can inject high-bandwidth switching RF noise into the I/O cables and interconnects.

To implement a quiet area, use of a partition is required. This quiet area may be

1. 100% isolated with I/O signals entering and exiting through an isolation transformer;
2. data line filtered;
3. filtered through a high-impedance common-mode inductor; or
4. protected by a ferrite bead-on-lead component.

The main objective of partitioning is to separate *dirty power and ground planes and other functional areas from clean or quiet zones and areas.*

4.11 ISOLATION AND PARTITIONING (MOATING)

Isolation and partitioning refers to the physical separation of components, circuits, and power planes from other functional devices, areas, and subsystems. Allowing RF currents to propagate to different parts of the board by radiated or conductive means can cause problems not only in terms of EMI compliance, but also with regard to functionality.

Isolation is created by an absence of copper on *all* planes of the board through use of a moat. Absence of copper is created using a wide separation, typically 0.050 inch (50 mils) minimum from one section to another. In other words, an isolated area is an island on the board, similar to a castle with a moat. Only those traces required for operation or interconnect can travel to this isolated area. The moat serves as a "keep out" zone for signals and traces that are unrelated to the moated area or its interface. Two methods exist

to connect traces, and power and ground planes to this island. Method 1 uses isolation transformers, optical isolators, or common-mode data line filters to cross the moat. Method 2 uses a bridge in the moat. Isolation is also used to separate high-frequency bandwidth components from lower bandwidth circuits, in addition to maintaining low-EMI bandwidth I/O in terms of the RF spectrum propagating from I/O interconnects.

4.11.1 Method 1: Isolation

Method 1 involves use of an isolation transformer or optical isolator. An I/O area must be 100% isolated from the rest of the PCB. Only at the metal I/O connector is RF bonding to chassis ground performed, and then only through a low-impedance, high-quality securement path to ground. We want to keep chassis ground outside this isolated area. The use of bypass capacitors from shield ground (or braid) of the I/O cable to chassis ground is sometimes needed in place of a direct connection when required by the interface specification. *Shield ground* (or drain wire) refers to a discrete pin or wire in the interface connector that connects the internal drain wire of the external I/O cable to its mylar foil shield, also located internal to the cable.

Pigtails should not be used under any condition to connect the shell of the BNC connector to chassis ground or to any other ground system. Measurements are well documented showing a 40- to 50-dB difference between a pigtail and a 360° connection of the cable shield to the BNC connector shell in the 15- to 200-MHz region for RF emissions. In addition to improvement in reducing RF emissions, a greater level of ESD immunity is provided due to less lead inductance that is presented to the ESD event. For most applications, the recommendation is to connect the cable shield to the BNC connector shell in a 360° fashion. This backshell then mates with a bulkhead panel containing a solid metallic contact with chassis ground.

Common-mode data line filters may be used in conjunction with isolation transformers to extend common-mode rejection. Common-mode data line filters (usually toroidal in construction) may be used for both analog and digital signal applications. These filters minimize common-mode RF currents carried on the signal traces to the I/O section or cable. If power and ground are required in the isolated area (e.g., +5 VDC for a keyboard or mouse), the moat should be crossed with a ferrite bead-on-lead for the power trace and a single solid trace three times the width of the power trace for a return. Use of a common-mode torroid in the power and ground connections is also an acceptable method. The secondary short-circuit fuse (required for product safety) can be located on either side of the ferrite bead, if required. Sometimes, capacitive decoupling is required to remove digital noise from filtered I/O power. This optional decoupling capacitor can be located with one terminal of the capacitor to the filtered side of the ferrite bead (output side) and the other terminal to the isolated ground plane. The power filtering components can be located across the moat at the far outside edge of the board. Both power and ground trace should be routed adjacent to each other to minimize RF ground loops that can be developed between these two traces if located on opposite sides of the moat. This is shown in Fig. 4.22 [1].

4.11.2 Method 2: Bridging

Method 2 uses a bridge between a control section and an isolated area. A bridge is a break in the moat at only one location where signal traces, power, and ground cross the moat. This is illustrated in Fig. 4.23 [1]. Violation of the moat by any trace not associated

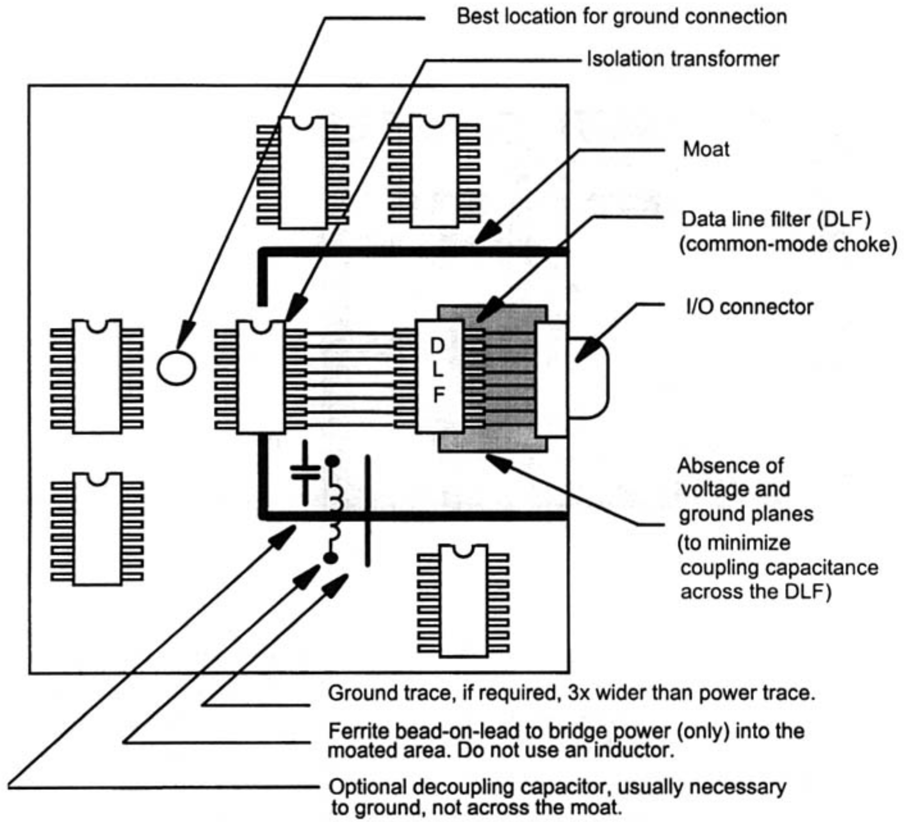


Figure 4.22 Using isolation in moating—Method 1.

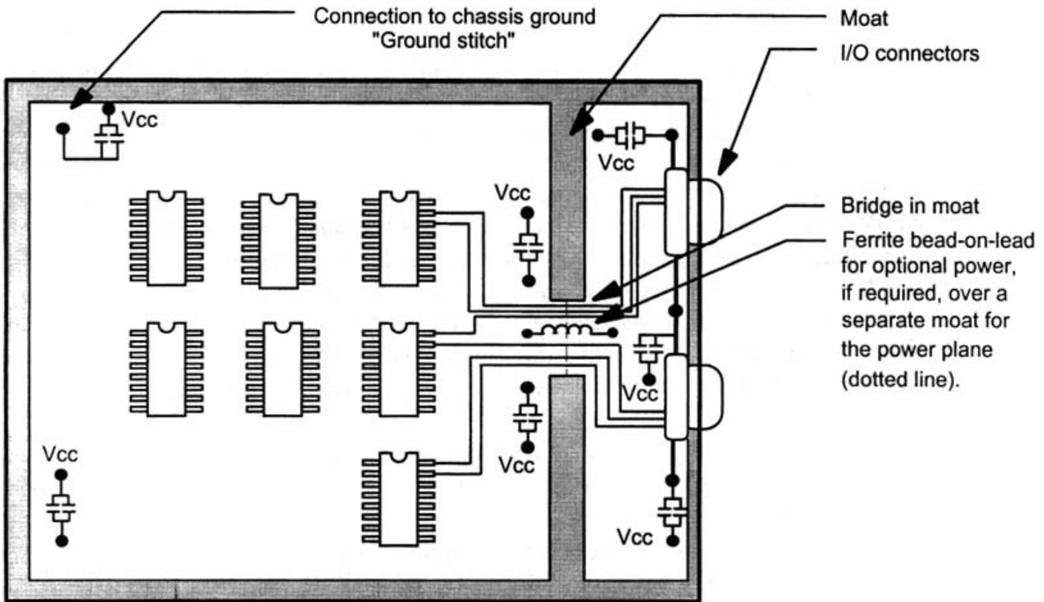


Figure 4.23 Bridging a moat—Method 2.

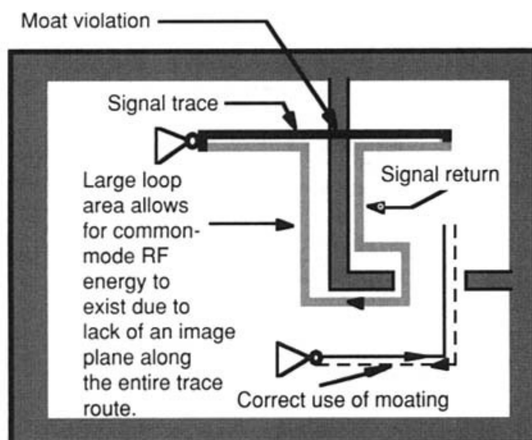


Figure 4.24 Violating the concept of moating.

with the I/O circuit can cause both emissions and immunity problems. RF loop currents will be created, detailed in Fig. 4.24 [1]. RF currents must image back along their trace route. Common-mode noise will be generated between the two separated areas. Unlike Method 1, power and ground planes are directly connected between the two areas; hence, this method forms a partition.

The advantage of using a bridge is similar to the castle concept with a moat. Only the signals that have a passport to cross the bridge will be allowed to pass. With the requirement and need for RF return currents to image back along the trace route, optimal flux cancellation (minimization) will occur. This one image return path is the only path that can be allowed to exist.

Sometimes, only the power plane is isolated, and the ground plane is fully connected through the bridge. This technique is common for circuits where a common ground plane is required, or separately filtered, where regulated power is needed. In this case, a ferrite bead-on-lead is typically used to bridge the moat for the filtered power only. This bead must be located in the bridge area and not over the moat. If analog or digital power is not required in the isolated area, this now unused power plane can be redefined as a second 0V (ground) plane referenced to the main ground plane. When a split plane partition is provided, one should guarantee that the traces that cross through the bridge do so along a solid 0V reference (ground) plane, and not against the split power plane.

When using bridging, grounding both ends of the bridge to chassis or frame ground is highly recommended if multipoint grounding is provided in the chassis and system-level design. Grounding the entrance to the bridge performs two functions:

1. It removes high-frequency common-mode RF components in the power distribution network (ground-noise voltage) from coupling into the partitioned area.
2. It helps remove eddy currents (for improved ground loop control) that may be present in the chassis or card cage. A much lower impedance path to ground is provided for RF currents that would otherwise find their way to chassis ground through other paths, such as RF currents in an I/O cable.

Grounding both ends of the bridge also increases electrostatic discharge immunity. If a high-energy pulse is injected into the I/O connector, this energy may travel to the main control area and cause permanent damage. This energy pulse must be sunk to chassis ground through a very low-impedance path.

Another reason to ground both sides of a bridge is to remove RF ground-noise voltage created by voltage gradients that appear between the partitioned area and main control section. If the RF common-mode noise contains high-frequency RF energy, decoupling capacitors for the RF energy (AC waveform) should be provided at each chassis ground stitch connection.

Figure 4.24 illustrates how traces are routed when using both digital and analog partitions. Since digital power plane switching noise may be injected into the analog section, isolation or filtering may be required. All traces that travel from the digital to analog section must be routed through the bridge. For analog power, a ferrite bead-on-lead should be used to cross the moat. A voltage regulator may also be required. The moat for analog power is usually 100% complete around the entire partition.

Certain analog components require analog ground to be referenced to digital ground but only through a bridge as shown in Fig. 4.25 [1]. Many analog-to-digital and digital-to-analog devices connect their analog ground (AGND) and digital ground (DGND) (indicated on the pin designation) together within the device package. When such is the application of a partition that is internal to the component, only one ground connection between analog and digital ground is required during PCB layout. AGND and DGND should be moated away from each other only when the circuit devices themselves provide separate AGND to DGND isolation *inside* the device package. It is important that the designer consult the recommendation made by the device manufacturer on how to properly isolate or connect AGND and DGND during layout.

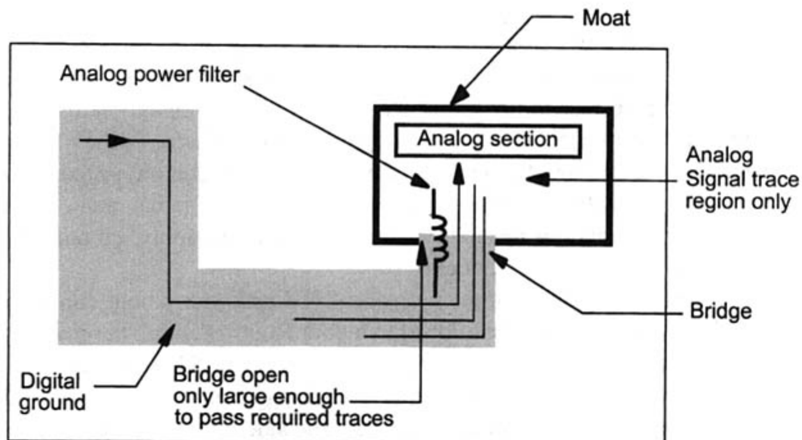


Figure 4.25 Concept of digital and analog partitioning.

4.12 INTERCONNECTS AND RF RETURN CURRENTS

When designing a product with interconnects, either internal or external, a decision must be made concerning how to create a single system that is compatible with all operational subassemblies. It is preferable to have a single system (PCB) rather than several smaller PCBs interconnected by cables assemblies that are not referenced to each other. Having a common reference will limit the voltage drops that are developed between various 0V reference structures (grounds). It is easier to limit this voltage drop when all ground references are located on the same PCB assembly than if they are placed on separate PCBs and interconnected by cables that are highly inductive by the nature of their physical construction.

The impedance between two subsystems can be reduced through use of an image plane or a low-impedance ground grid structure. All ground structures must be connected together in as many locations as is physically possible. The more ground connections, be it through vias, cable connectors, ground stitch connections, and the like, will allow RF return currents to be controlled from the assembly. With less RF return current within the interconnect structure, less RF emissions will be present.

When using cables to interconnect PCBs or peripheral devices to another PCB, creating a low-impedance path to ground becomes difficult because it is difficult to intersperse ground wires, or ground pins in an optimal position within the connector. This is especially true if the connector pinout assignment is random without consideration for the RF return current path during the design cycle. Use of a predefined bus structure may present functionality concerns because the number of signal traces provided may require the majority of available pin connections, which may also significantly far exceed an equal number of RF returns or ground pins. The summation of all RF return currents in a single ground return pin, with many I/O or signal pins, may cause the circuit to be nonfunctional related to EMI (radiated emissions) because of excessive current and ground bounce across the single ground pin.

A typical I/O configuration is shown in Fig. 4.26. Notice that because of a poor pinout assignment, large RF loop currents will occur between power and ground, or between a signal trace (with or without a periodic clock signal) and a 0V RF current return path. High-frequency RF voltages may be developed between the main PCB and interconnect area. These high-frequency voltages can create common-mode currents flowing between the assemblies. These currents accentuate both radiated and conducted emissions. If all components are located on the same PCB assembly, common-mode currents between interconnects must not exist.

For the routing configuration identified as "poor pinout configuration," Fig. 4.26, the clock trace shown is positioned in a poor location within the interconnect assembly; it is not surrounded by a 0V reference (ground). The RF return currents that are created on the clock trace, in addition to the switching currents that exist within the power distribution network, must travel to the opposite side of the connector in its attempt to return to its source (complete the circuit). With a large loop area, a magnetic field is created. This magnetic field creates an electric field that may be observed during compliance testing.

Under the enhanced pinout configuration, optimal pinout design for RF return currents exists, thus minimizing loop areas. The clock trace is routed in a stripline configura-

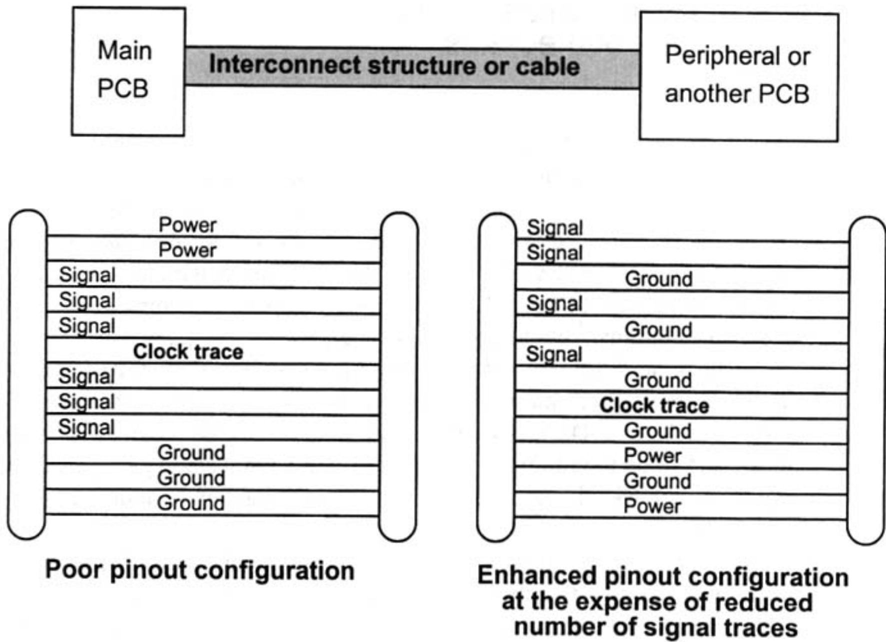


Figure 4.26 Pinout configuration typical of interconnects.

tion. Routing a clock trace stripline within an interconnect provides enhanced system performance and prevents development of RF currents losses. We also have a much lower impedance power distribution system to minimize ground bounce and the transference of high-frequency, high-bandwidth RF energy. This RF energy may be created with certain components injected into the power distribution system. This energy may also be transferred to other components sensitive to RF noise corruption by the power distribution network.

High-speed signals that travel between interconnects should be buffered at the entry point to reduce drive-capability and fan-out concerns, capacitive loading effects, and ground bounce when a signal crosses the interconnect barrier. A buffer reduces RF currents in the interconnect by a factor of four, in addition to reducing common-mode currents. An additional benefit of a buffer allows the source driver to consume less power when driving a loaded trace, especially if a high-impedance interconnect exists which already causes a large resistance-based drop to be developed.

When many nonperiodic signals are present within an interconnect structure, several signal traces may be contained or interspersed between 0V reference traces. The purpose of this configuration is to force the return currents on the interconnect to return to their source by the path of least impedance. In general, the concept is to design the PCB layout to force the RF return currents to travel the way we want them to travel within the PCB assembly. It becomes the designer's job to direct RF currents on the board in an optimal, low-impedance manner. It is not desirable to allow the RF return currents to travel any way they can within an assembly, for a random RF current return path will tend to maximize radiated emissions.

4.13 LAYOUT CONCERNS FOR SINGLE- AND DOUBLE-SIDED BOARDS

Special concerns exist for single- and double-sided PCB assemblies. With high-speed, high-technology products, use of single- and double-sided assemblies presents additional concerns relating to EMC compliance. These concerns are difficult to implement using specialized or advanced layout design techniques. For lower technology designs that are sensitive to cost, the use of single- or double-sided assemblies is frequently desirable. Consideration must be made for the RF return current to complete its return home to the source in an optimal, low-impedance manner.

One should think in terms of using transmission lines for both signal and power. Power and return lines must be routed parallel to each other as they are distributed to the component devices. Dedicated return traces should also be provided for high-threat traces, clocks, and so on to minimize loop structures that radiate and pick up electromagnetic energy. In double-sided boards, loop area control is the key to signal quality and EMI performance.

It is important to note, especially for EMC compliance, that there is *no such thing as a double-sided PCB*, although it physically exists. When analyzing how a double-sided PCB functions, related to EMC compliance, it should be noted that for a typical PCB the standard thickness of 0.062 inch (1.6 mm) is provided for the core material. The distance spacing between the top layer with components and a bottom layer with a ground plane or 0V reference structure is often assumed to provide an image plane for RF return currents created on the top layer. In reality, the distant spacing between the signal trace and image plane is so great that flux cancellation cannot occur efficiently. Flux cancellation cannot occur efficiently because of the lack of mutual partial inductance between the trace and return plane. The field distribution from a signal trace can be small, while the distance separation between trace and plane is extremely large.

The proper way to describe a double-sided PCB is to think of the board as two single-sided designs. We must route both the top and bottom layers of the PCB using design rules and techniques appropriate for single-sided designs.

For example, if the width of the trace is 0.008 inch (2 mm), the field distribution at a distance from the trace approaches 0.008 inch (2 mm). If a reference plane is greater than 0.008 inch (2 mm), then flux cancellation occurs with less efficiency and the RF return current can travel partly through free space. This distance spacing on a double-sided board is typically 0.062 inch (1.6 mm), which is much greater than 0.008 inch (2 mm). This is illustrated in Fig. 4.27.

What is the implementation of a return path for RF currents on single- or double-sided PCBs? We must remember that double-sided PCBs must be considered as two single-sided PCBs. This is difficult to achieve with full level of success. Examples are shown below. To allow for return currents, we must use ground traces (guard trace) or a gridded system at 0V potential. A ground trace or gridded system provides an alternate return path for RF currents. This alternate return path allows RF current to return to the source in a low-impedance manner, which is not an optimal implementation since a full return plane does not exist. For single-sided boards, ground traces are the primary design technique that allows RF currents to return to their source, thus controlling loop areas and, with that EMI.

For both single- and double-sided PCBs, plenty of local filtering or decoupling must occur for every device. Additional small high-frequency filtering to the critical signal

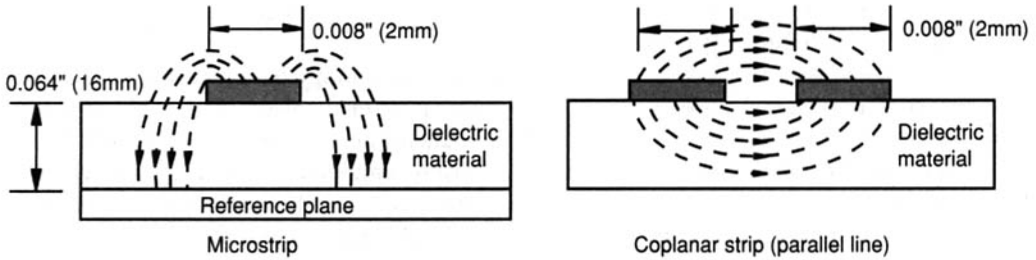


Figure 4.27 Field distribution for microstrip and coplanar strips. (*Source: Introduction to Electromagnetic Compatibility*, Clayton Paul © 1992 Reprinted by permission of John Wiley & Sons, Inc.)

lines must also occur directly at the component. We do not have the benefits of a ground plane; hence, different design techniques must be implemented.

4.13.1 Single-sided PCBs

For single-sided PCBs, there is only one conceptual design technique that provides for RF return currents. This technique is to use a ground trace (guard trace) that is placed as physically close to the high-threat signal trace as possible. This is shown in Fig. 4.28. The power and ground return traces must also be routed parallel to each other with decou-

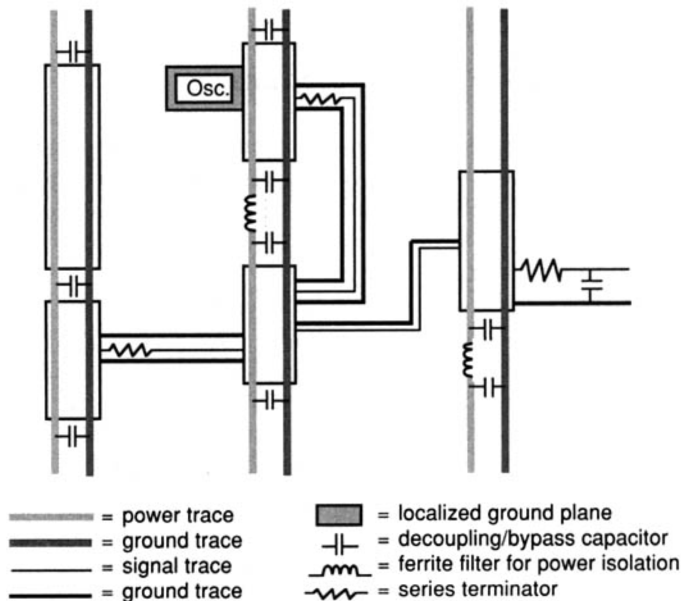


Figure 4.28 Single-sided routing for RF return currents.

pling capacitors provided for each and every component that injects switching energy into the power distribution system.

When a gridded power and ground layout methodology is provided, care must be taken to guarantee that the grids are tied together in as many places as possible. If a grid system is not used, RF loop currents from components may not find a low-impedance RF return path by any reliable means, thus exacerbating emission. By routing power and return traces together in parallel runs, a low-impedance, small loop area transmission line structure can be created, depending on how the parallel runs are implemented during layout. Signal traces referenced to the 0V structure can still create significant current loops if the distance spacing between the trace and 0V reference is excessive.

A problem with single-sided PCBs centers on how traces are routed between components when a power and ground grid exists. In almost every application, it becomes impractical to fully grid a single-sided board. The most optimal layout technique is to use ground fill to substitute as an alternate return path for loop area control and reduced impedance for RF return currents to travel home. This ground fill must be connected to the 0V reference point in as many places as possible.

4.13.2 Double-sided PCBs

There are two types of implementation for providing an alternate return path for RF currents.

1. Symmetrically placed components (e.g., memory arrays)
2. Asymmetrically placed components

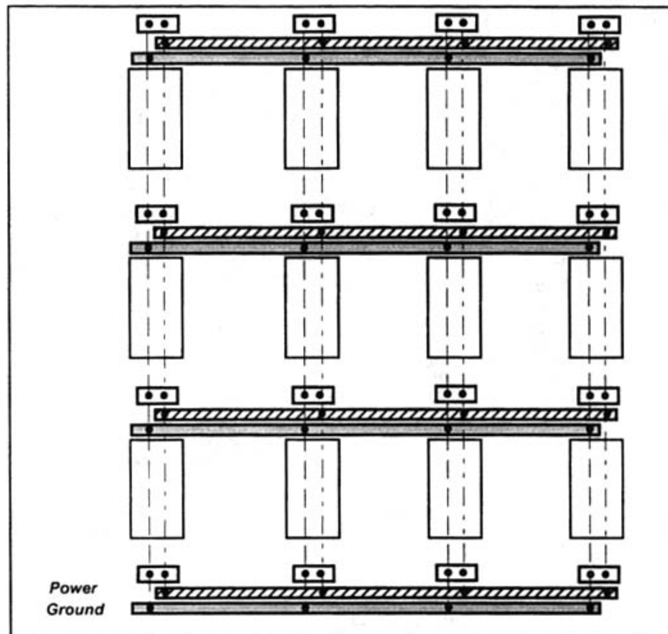
4.13.3 Symmetrically Placed Components

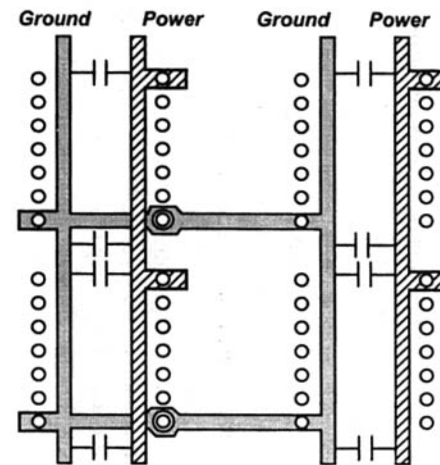
There is one primary implementation technique for providing a low-impedance path for RF return currents for two-layer boards related to EMC compliance. The first is for older technology (slow speed components). These designs usually consist of Dual-In-Line Packages (DIPs) placed in a straight row or matrix configuration. Very few products currently use this technique or technology.

Routing horizontal traces on the solder side and vertical traces on the circuit side is the most commonly used technique for double-sided boards. This becomes a design rule that is usually not violated when using symmetrically placed components. The power trace is routed on the top (or bottom) layer, while the ground trace is routed on the opposite layer. All interconnects are made using plated through-holes. For areas that are not being used for either power, ground, or signal traces, ground fill must be used to aid in providing a low-impedance path to ground for RF return currents.

To summarize Fig. 4.29:

- Layer the power and ground in a grid style with the total loop area formed by each grid square not exceeding 1.5 square inches (3.8 square cm), although faster edge-times may demand smaller grids.
- Run power and circuit traces orthogonally to each other, power on one layer, ground on the other layer.
- Locate decoupling capacitors between the power and ground traces at all connectors and at each IC.





Closeup of power and ground grid

1. **Top of board has all vertical traces.**
2. **Bottom of board has all horizontal traces.**
3. **Feedthroughs where power and ground traces intersect.**
4. **Decoupling capacitors between power and ground at connectors and at each IC.**
5. **Signal lines follow vertical/horizontal pattern.**

Figure 4.29 Two-layer PCB with power and ground grid structure.

A power and ground grid system works because the grid structure provides a common return path for RF currents when an image plane is not present.

4.13.4 Asymmetrically Placed Components

Asymmetrically placed components are found in many current designs. This layout design is commonly used in low-frequency analog systems—less than 1 kHz and nearly all low-speed, older technology products.

- Route all power traces in a *radial fashion* from the power supply to all components on the same routing layer. Minimize the total length of all traces.
- Route all ground and power traces adjacent (parallel) to each other. This minimizes loop currents that may be created by high-frequency switching noise (internal to the components) from corrupting other circuits and control signals. Ideally, the only time these traces should be separated by a distance not greater than the width of any individual trace is when they must separate for connection to the decoupling capacitor. Signal flow should parallel these ground paths.
- Prevent loop currents by not tying different branches of a tree to another branch.

In examining Fig. 4.30, observe that at low frequencies, parasitic L and C generally do not cause problems as they do in high-frequency application. For this situation, single-point grounding is possible.

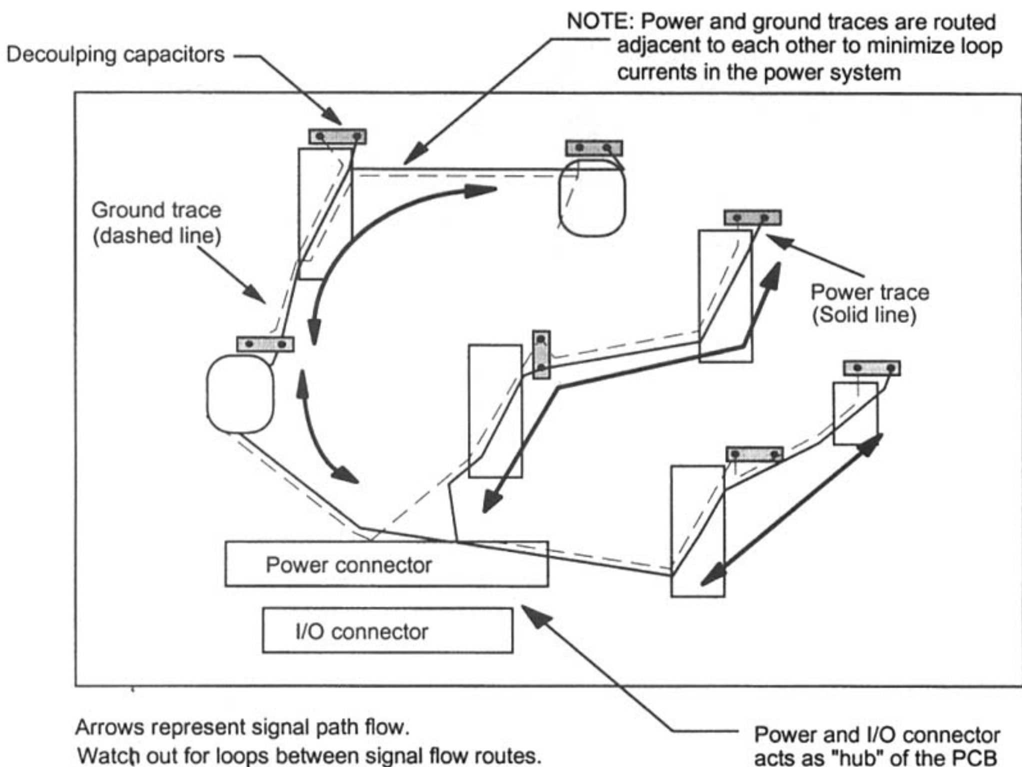


Figure 4.30 Two layer board with radial structure for power routing and flow migration.

In Fig. 4.30, the following is noted. For high-frequency applications, control the surface impedance *(Z)* of all signal traces and their return current path. When used in a low-frequency application, instead of impedance control, topology layout is a primary concern. Loop currents can be prevented from being created by not having components tied together.

4.14 GRIDDED GROUND SYSTEM

A gridded ground system is an effective method of reducing trace inductance and allows for an RF current return path to exist. This grid system can be incorporated within the design layout and is usually found on only single- or double-sided PCBs. When a multilayer structure is provided, a gridded ground system is not sufficient to provide significant control of RF currents as the image planes are more efficient for flux cancellation. A gridded ground system contains both horizontal and vertical ground paths on the PCB, shown in Fig. 4.31. A grid size spacing of 0.5 inch (1.27 cm) is typical, although larger spacing is acceptable depending on the edge rate of the signals and the complexity of the component layout. A generally accepted criterion for grid spacing is one-twentieth of a wavelength, based on the highest frequency that the grid is expected to handle. The main objective is to limit trace inductance by limiting the space between the grids and to make the ground grid and interconnecting elements as "fat" as possible.

A good rule of thumb is to use a grid size whose spacing allows a grid to exist between every IC on the board. This spacing provides an alternate RF return path when a ground plane cannot be implemented. This grid could exist on single-sided boards (extremely difficult, if not impossible); however, it is more optimal to implement a grid on a double-sided board. When using a double-sided stackup assignment, the x-axis traces are

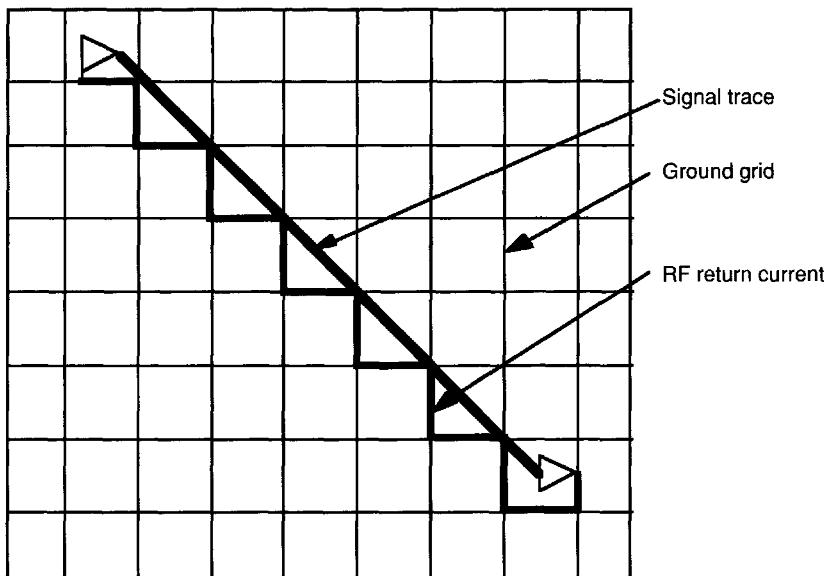


Figure 4.31 Gridded ground structure.

usually routed on the top layer, while y-axis traces are located on the bottom side. These traces are connected together by vias wherever they jump layers. This layer jumping allows ample room for necessary signal routing and interconnects. The ground grid on one side of the PCB is connected to the ground grid on the opposite side of the board using as many vias as possible.

The voltage developed across a return conductor is referred to as ground drop or ground bounce. The lower the value of ground drop between two points on a PCB return structure, the lower the radiated emissions from the PCB.

In studying Fig. 4.31, we notice that if the grid spacing was smaller than that provided, the RF return current would mirror image back closer to the signal trace with enhanced mutual partial inductance. Because there is no straight-line path, a convoluted loop area is created which enhances creation of RF energy.

To optimize the design and layout of a PCB using a gridded ground structure, it is imperative to design the grid structure before component placement occurs or signal traces are routed. It becomes difficult to implement a gridded structure after the board is routed. This grid adds no per-unit cost to the product. For single- and double- sided boards, this grid structure may be the only noise suppression technique possible.

A common question regarding the grid structure is, "How wide do I make the traces"? The optimal answer is, "as wide as possible." In reality, the grid can be made with a narrow conductor, since the impedance of the traces are added together in parallel, thus creating a total low-impedance return path. This impedance will still be higher compared to that of an image plane. The only design concern is to guarantee that the width of the traces can handle the 0V return current (from the power supply, not RF return current). Note that a grid developed from narrow traces is preferred to not having a grid at all.

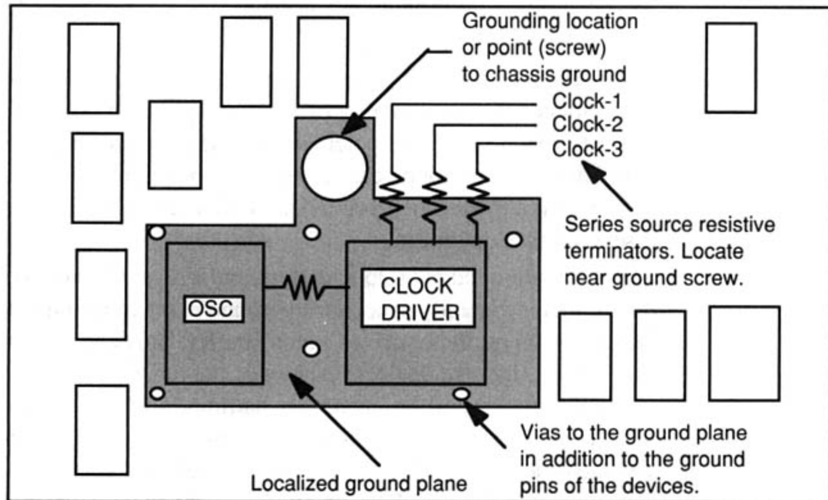
4.15 LOCALIZED GROUND PLANES

The following layout techniques allows for the capture of RF flux generated internal to components and oscillators. This design concept is called a localized ground plane, and it forms a part of the partition concept.

Oscillators, crystals, and all clock support circuitry (e.g., buffers, drivers, etc.) can be located over a single localized ground plane. This localized ground plane is on the component (top) layer of the PCB and ties directly into the main internal ground planes of the PCB through both the oscillator ground pin and a minimum of two additional ground vias. This ground plane should also be positioned next to and connected to a ground stitch location. An example of this localized ground plane is shown in Fig. 4.32 [1].

The following are the main reasons for placing a localized ground plane under the clock generation area:

- Circuitry inside the oscillator demands RF currents. If the oscillator package is a metal can, the DC power pin is relied on for both DC voltage reference and a path for RF currents to be sourced (or sunk) to ground from the oscillator circuitry. Depending on the type of oscillator chosen (CMOS, TTL, ECL, etc.), RF currents created internal to the package can become so excessive that the ground pin is unable to efficiently source this large *LdI/dt* current with low loss (*L* from



Note 1: Do not run any traces on layer 1 through the localized ground plane.
Note 2: If two microstrip layers exist, do not route any traces on layer two of the localized ground plane (route keep-out area).
Note 3: The localized ground plane is a solid copper plane without solder mask bonded to the main ground plane(s) by vias "and" bonded to the ground stitch location by a screw or equivalent method.

Figure 4.32 Localized ground plane.

the pin lead) to ground. As a result, the metal case becomes a monotonic antenna. The nearest image or ground plane (internal to the PCB) is sometimes two or more layers away and is thus inefficient as a radiated coupling path for RF currents to ground.

- If the oscillator is a surface-mount device, the situation mentioned above is made worse because SMT packages are often plastic. RF currents created internal to the package can radiate to free space and couple to other components. The high impedance of the PCB material, relative to the impedance of the ground pin of the oscillator, prevents RF currents to be sourced to ground. SMT packages will always radiate more RF energy than a metalized case.
- Placing a localized ground plane under the oscillator and clock circuits provides an image plane that captures common-mode RF currents generated internal to the oscillator and related circuitry, thus minimizing RF emissions. This localized ground plane is also at RF hot potential. To contain differential-mode RF current that is also sourced to the localized ground plane, multiple connections to all system ground planes must be provided. Vias from the localized plane, on layer 1, to the ground planes internal to the board will provide this lower impedance path to ground. To enhance performance of this localized ground plane, clock generation circuits should also be located adjacent to a chassis ground (stitch) connection. Connect this localized ground plane to the plated through-hole, 360° connection, preferably not using a wagon wheel configuration. Ensure a low-impedance RF bonding connection to ground exist. Connection through traces to a ground stitch location can defeat a low-impedance connection. While thermal relief "wagon

wheel" connections usually are acceptable, they also degrade the performance of the low-impedance connection.

- When using a localized ground plane, *"do not run traces through this plane"!* This violates the functionality of an image plane. If a trace travels through a localized ground plane, the potential for small ground loops or discontinuities exists. These ground loops can generate problems in the higher frequency range. Why install a plane when you defeat its functional use by running traces through it severing its continuity?
- Support logic circuitry (clock drivers, buffers, etc.) must be located adjacent to the oscillator. Extend this localized ground plane to include this support circuitry. Generally, an oscillator drives a clock buffer. This buffer is usually a super-high-speed, fast edge rate device. Because of the functional characteristics of this driver, RF currents will be created at harmonics of the primary clock frequency. With a large voltage swing and drive current injected onto the signal trace, both common-mode and differential-mode RF currents will exist. These currents can cause functionality problems and possible noncompliance to EMC requirements.

14.5.1 Digital-to-Analog Partitioning

Concerns exist for proper partitioning of digital-to-analog circuits, components, and functional subsections. Because of the application of the circuit partition, and how the component manufacturer designed the silicon substrate, a common ground reference structure may or may not be required. If the vendor designed its component for filtered analog power using a common digital/analog ground, then it is only necessary to filter the power plane or power pin.

If the component has designed into the silicon a separate partition for a distinct digital ground and distinct analog ground, the component itself may be partitioned in the layout on the PCB depending on the transfer characteristics across the device's silicon partition. This partition is achieved through use of moating between the component pins. All analog discrete components must reside within the analog section as detailed in Fig. 4.33.

Within Fig. 4.33, we have two configurations, both with a localized ground plane and moating within the multilayer stackup. We can extrapolate this localized ground plane to be both a formal power and ground plane within a multilayer stackup assembly. The only difference between the localized ground plane and the internal ground plane is that the localized plane is on the top first layer directly under the component or oscillator.

While constructing the PCB during component placement and the partitioning implementation stage, we may sometimes create a very convoluted shape that zigzags between the pins of a component if the component manufacturer did not provide an optimal pinout configuration that allows for ease of digital-to-analog partitioning.

For both design applications, the analog power input to the device is filtered with a ferrite bead-on-lead and capacitors. The filtered side of the bead is located within the "quiet" analog plane or localized ground plane. The output of the analog device, if required, is filtered with an appropriate device. This device may be another ferrite device or an inductor, based on functional application and use.

If partitioning is performed on the power and ground plane structure, the moat must occur on all planes present within the board stackup assignment. It becomes critical that overlapping planes do not occur as was detailed in Fig. 4.19. It is imperative to prevent

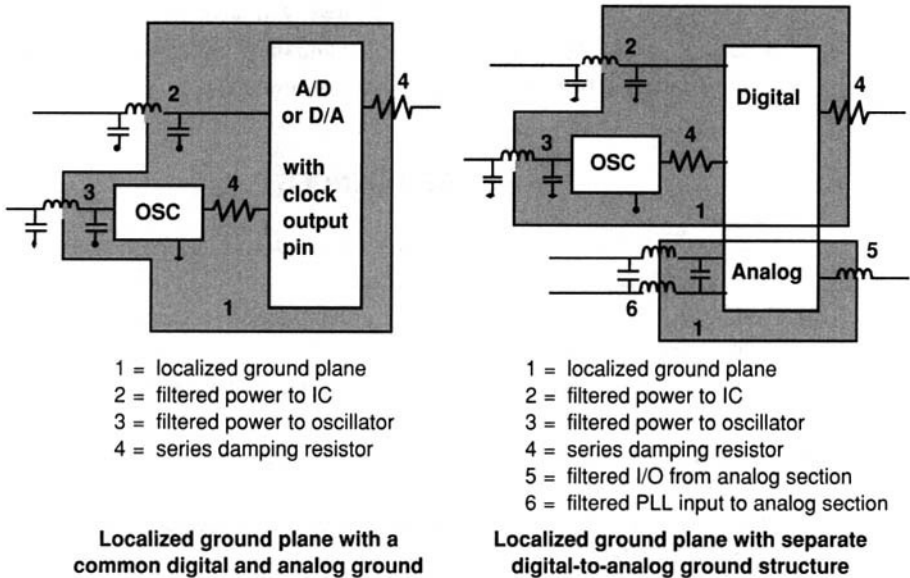


Figure 4.33 Localized ground plane—digital-to-analog partition. (*Source: Designers Guide to Electromagnetic Compatibility*, EDN. © 1994. Cahners Publishing Co. Reprinted with permission.)

capacitive coupling between noisy digital planes and quiet analog planes, thus circumventing possible resonances from developing common-mode noise.

4.16 SUMMARY

An image plane is a term commonly used to identify a return path for RF currents to complete their journey home. This plane consists of a solid copper sheet laminated within a multilayer PCB stackup assignment. An image plane provides a low-impedance RF transmission path for magnetic lines of flux to mirror image themselves against their source transmission line. The closer the distance spacing between source and return path, the more enhanced flux cancellation becomes. Higher density PCB stackups provide approximately six to eight dB of RF suppression per image plane pair due to enhanced flux cancellation.

Benefits of Multilayer Boards

- One or more planes can be dedicated exclusively to power and ground. The principal benefit is due to the presence of the first solid plane.
- A well-decoupled power distribution system exists.
- Circuit loop areas are reduced, thereby reducing differential-mode radiated emissions and susceptibility. Reduction of differential-mode currents will keep common-mode RF energy from being created.

- The signal and power return path (ground) will have minimal impedance levels.
- Characteristic impedance of traces is maintained throughout a trace route.
- Crosstalk will be minimized between adjacent traces.

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