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9

Grounding

9.1 REASONS FOR GROUNDING—AN OVERVIEW

Grounding is required within most products. Although this ground may be fully connected, isolated, or floating, a ground structure must still be present. Grounding is often confused with providing a current return path for signals. In reality, only a few grounding issues are related to PCBs. These concerns relate to providing a reference connection between analog and digital circuits and a high-frequency connection between the PCB return plane and an external metal chassis.

Grounding, though probably the most important aspect of a design, is least understood by many engineers. It is not easy to understand intuitively and does not usually allow for straightforward definition, modeling, or analysis since many uncontrolled factors affect its performance. Every circuit is ultimately referenced to a ground source and cannot be left to chance; it must be designed in from the very beginning. One cannot assume that because a ground system is present, for example, a metal enclosure, optimal performance will be achieved. Desired performance is not easily achieved if no thought is given to its design.

Grounding is one primary method of minimizing unwanted noise pickup and partitioning circuit segments. Proper implementation of PCB ground methods and cable shields will prevent a majority of noise problems. One advantage of a well-designed ground system is protection against unwanted interference and emissions for basically zero cost in material usage.

9.2 DEFINITIONS

The word *grounding* is vague and means different things to different people. For logic designers, it refers to a reference level for logic circuits and components. For system and mechanical engineers, ground is the metal housing or chassis that connects circuits. For

electricians, it refers to the third wire safety ground as mandated by their respective National Electric Codes.

To prevent confusion, the following words used in this chapter are defined as follows.

Bonding. Making a low-impedance electrical connection between two metal surfaces.

Circuit. Multiple devices with a source impedance, load impedance, and interconnects. For digital circuits, multiple sources and loads may be part of one circuit where all devices are referenced to the same point or use a common signal return conductor. For EMC, circuits usually originate in one location and terminate in another.

Circuit Referencing. The process of providing a common 0V reference voltage for multiple circuits to allow communication between the two. Circuit referencing is one of the most important reasons for providing a ground reference. This reference point is not intended to carry functional current.

Earthing (British term). The connection of the safety ground wire to earth at the service entrance of a building.

Equipotential Ground Plane. A solid piece of metal used as a common connection point for power and signal referencing. This plane may not be at equipotential levels for RF frequencies owing to its electrically large size.

Ground Loop. A circuit that includes a conducting element (plane, trace, wire) assumed to be at ground potential where return currents pass through. At least one ground loop will be present within a circuit. Although a ground loop is acceptable, the severity of the problem for currents flowing through the loop depends on the unwanted signals that may be present, which can cause system malfunction.

Ground Stitch Location. The process of making a solid ground connection from a PCB to a metallic structure for the purposes of providing systemwide ground referencing regardless of which grounding methodology is used.

Grounding. A generic term with as many definitions as there are engineers. This word must be preceded by an adjective.

Grounding Methodology. A chosen method for directing return currents in an optimal manner appropriate for the intended application.

Holy Ground. Sometimes referred to as the actual location used. *See also* Single-point ground.

Hybrid Ground. A grounding methodology that combines single-point and multipoint grounding simultaneously, depending on the functionality of the circuit and the frequencies present.

Multipoint Ground. A method of referencing different circuits together to a common equipotential or reference point. Connection may be made by any means possible in as many locations as required.

Referencing. The process of making an electrical connection or bond between two circuits that allows the 0V reference from both circuits to be identical.

RF Ground. The process of providing a ground reference point using a specific methodology to allow a product to comply with both emissions and immunity requirements.

Safety Ground. The process of providing a return path to earth ground to prevent the hazard of electric shock through proper connection and routing of a permanent, continuous, low-impedance, adequate fault capacity conductor that runs from a power source to a load.

Shield Ground. The process of providing a 0V reference or electromagnetic shield for both interconnect cables and main chassis housing.

Single-point Ground. A method of referencing many circuits together at a single location to allow communication between different points. All signals will thus be referenced to the same location.

When discussing grounding concepts, it is best to use an adjective to better define what we want, such as signal ground, chassis ground, safety ground, and analog ground.

9.3 FUNDAMENTAL GROUNDING CONCEPTS

The two primary areas related to grounding are

1. Safety ground (including protection against the effects of lightning and electrostatic discharge).
2. Signal voltage referencing ground.

If a ground is connected by a low-impedance path to earth, this method is identified as a safety ground. Signal grounds may or may not be connected to earth potential. Connection of the two ground methods may be unsuitable for a particular application and may exacerbate EMC problems.

Safety grounding minimizes or prevents a voltage difference between exposed conducting surfaces. The more conductors we make available to reduce the voltage difference to extremely low levels, the less chance of electric shock may be present to harm someone or cause death. The more ground connections, the less chance of harm to the operator.

Signal voltage referencing ground provides for all parts of an electrical system to be referenced to a common source. For signal referencing, the voltage difference typically must be less than a few millivolts. The implementation of signal voltage referencing, the number of ground connections, and their location must be chosen carefully. Few critically located connections between signal voltage points can allow a product to be either compliant or noncompliant to EMC regulations.

Common misconceptions exist regarding grounding. Most analysts believe that ground is a current return path and that a good ground reduces circuit noise. This belief causes many to assume that we can sink noisy RF currents into the earth, generally through a building's main grounding structure. This is valid if we are discussing safety grounding, not signal voltage referencing.

Current requires a return path to complete a closed-loop circuit. We usually only consider AC or DC supply current and not RF current. Although an RF return path is mandatory, it need not be at ground potential. Free space is not at ground potential. Analog ground is isolated from digital or chassis ground to prevent disruption to sensitive circuits. Not all currents within a system require a safety ground or a signal voltage refer-

ence. For example, low-voltage battery-operated devices do not require any external safety ground connection, for no shock hazard exists.

To guarantee that a system works within a specific design requirement, signal ground may not be the same as current return. Signal currents should not flow on grounding conductors except under certain conditions. Regardless of application, for both safety and signal referencing, we must either reduce the ground voltage difference between two circuits or avoid having a voltage potential difference at all.

Why is safety ground discussed in a book about EMC and PCBs? The reasons are obvious. Many PCBs contain hazardous voltages. These include power supply assemblies, telecommunication circuits, relay-driven instrumentation control units, power switching modules, and the like. User safety cannot be separated from EMC. The field of regulatory compliance includes both product safety (meeting essential safety requirements based on National Electric Codes or governmental mandated legislation) and EMC limits for emissions and immunity. Product safety standards mandate the amount of creepage and clearance distance between traces to prevent electric shock to the user. For example, the distance spacing that must be used for a product safety requirement between hazardous voltages on traces may prevent optimal flux cancellation from a voltage or signal trace to a ground fill or ground trace for single- or double-sided PCBs.

Creepage and clearance is of concern because AC or high-voltage traces may be subject to an abnormal failure condition. Failures include primary-to-secondary, primary-to-ground, or primary-to-primary. To prevent a shock hazard due to an abnormal failure, traces must be routed with a specific amount of spacing (distance) between high-energy (voltage) traces and secondary or ground circuits. This requirement is especially critical in power supplies and related circuitry.

When routing AC voltage traces, one should use sufficient trace width and spacing to comply with legally mandated creepage and clearance requirements. The following definition of creepage and clearance is extracted from, and is identical to, all international product safety standards.

- Creepage is the shortest path between two conductive parts, or between a conductive part and the bounding surface of the equipment, measured along the surface of the insulation.
- Clearance is the shortest distance between two conductive parts, or between a conductive part and the bounding surface of the equipment, measured through air.
- Bounding surface is the outer surface of the electrical enclosure considered as though metal foil were pressed into contact with the accessible surface of insulation material.

When dealing with ground currents, several fundamental concepts must be remembered.

- Whenever a current flows across a finite impedance, a finite voltage drop occurs (Ohm's law). As stated in Ohm's law, there can never be "zero volt potential" in the real world. The units may be in the pico range (voltage or current). Still, a finite value will exist.
- Current must always return to its source. This return may consist of numerous paths with various amplitudes provided for each return current proportional to

the finite impedance within each and every path (Kirchhoff's law). Unintended currents can travel in alternate return paths which may not be designed to handle these currents.

To illustrate these fundamental concepts, Fig. 9.1 shows two subsystems connected to a metallic plate, chassis, or other item identified as ground. These subsystems may be analog, digital, or another defined source. If digital, the power (+Vcc) current returns to its source, the power supply through a return system. Current is constantly changing when devices switch logic states, consuming power. In analog circuits, the return current may contain low-frequency or high-frequency narrowband or broadband signals. Analog signals generally have dedicated return or "grounds" that are different from digital logic.

As can be observed in Fig. 9.1a, the return current path of Subsystem #2 travels through the same return line as Subsystem #1. The two currents add up at the power supply source. Since a return path will have a finite impedance, either resistive or inductive, currents within the return structure will cause a voltage potential to be developed between the two subsystems. The ground point of Subsystem #1 is varying at a rate proportional to the signals in Subsystem #2. By virtue of this coupling through a common impedance, the power source now sees two separate voltage potentials simultaneously.

So far, this has been a discussion about ground-noise voltage. What about the voltage that is observed at the load? The voltage of the ground point for Subsystem #2 is $Z_{g1}I1 + (Z_{g1} + Z_{g2})I2$. Subsystem #2 contains the signals of Subsystem #1 through Z_{g1} in addition to its own signal. This situation is identified as common-impedance coupling.

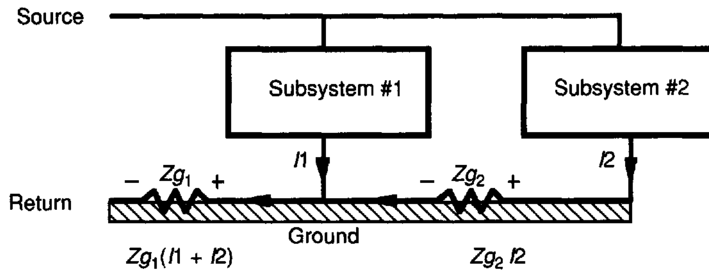


Figure 9.1a Common-impedance coupling in a ground structure. (*Source:* Clayton Paul, *Introduction to Electromagnetic Compatibility*, © 1992. Reprinted by permission of John Wiley & Sons.)

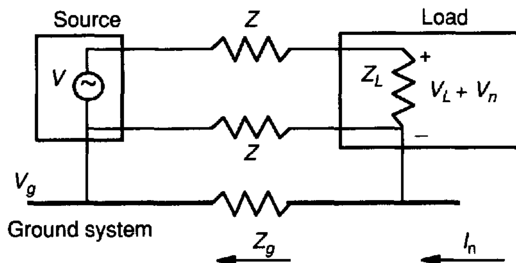


Figure 9.1b Conductive coupling of ground noise with interconnecting cables.

Figure 9.1b illustrates a connection commonly found in data communications where a signal (e.g., RS-232) and its return path are provided. Let's assume the source is a computer and the load is a monitor or modem located some distance away. The ground system common to both devices is the third wire safety ground within their respective power cord. This power cord ground has a high impedance at RF frequencies. In this case, the noise source from the external system drives a noise current I_n into the safety ground wire, which is common to all devices. Let's assume load Z_L is greater than the return wire impedance Z and the power wire impedance Z_g. The ground noise developed on the return wire adds to the signal voltage of the load, described by

$$V_n = \frac{Z - Z_g}{Z + Z_g} * (V_g) \tag{9.1}$$

A misconception regarding ground impedance is the type of impedance that exists. Most engineers assume that ground impedance is at DC potential or has low-frequency resistance. At high-frequency of operation, 30 MHz and above, the primary impedance component that is observed is inductive, not *resistance* or *skin effect*. Resistance and skin effect are negligible compared to the inductance. As presented in earlier chapters, inductance is approximately 15 nH/inch for a 0.020-inch trace. Using $X_L = 2\pi fL$, at 100 MHz, the inductive reactance is 9.43 Ω/inch. A #28AWG wire (radius of 6.3 mils) has an inductive reactance of 65.9×10^{-3}Ω/inch. As observed, there is a significant magnitude of difference between resistance and inductance at 100 MHz. This is why resistance is not a concern at RF frequencies.

When designing a product, minimal or zero cost may be incurred during the design cycle when grounding is taken into consideration. A well-designed ground system, not only on the PCB, but systemwide, will offer both improved emissions and immunity protection. A grounding system that was not thought about during a design cycle, or re-implemented from a design on a different product (because it once worked on that product, so why redesign?), is a sign of system failure related to system functionality or EMC compliance.

The important areas of concern include the following.

- Minimize or reduce current loops by careful layout of high-frequency components.
- Partition areas of the PCB, or system, to keep high-bandwidth noise circuits from low-frequency circuits.
- Design the PCB, or system, to keep interfering currents from affecting other circuits through a common ground return path.
- Carefully select ground points to minimize loop currents, ground impedance, and transfer impedance of the circuit.
- Consider the current flow through the ground system as it relates to noise being injected into or from a circuit.
- Connect very sensitive (low noise-margin) circuits to a stable ground reference source.

The next section examines various ground systems and how they apply to a product's overall design. Following this examination, there is a description of how to implement grounding methods in an optimal manner.

9.4 SAFETY GROUND

The primary concern associated with a safety ground is the protection of people, animals, and other living creatures from the hazard of electric shock. When a product is at a hazardous voltage potential, serious injury or death may occur.

If the system is powered by AC voltage above certain levels (defined below), exposed metal must be bonded to a "green or green/yellow stripe wire" safety ground provided within the AC mains power cord. This requirement also applies to battery-operated devices if the battery charger is built into the module unit or built onto the PCB, powered by AC mains voltage. If the unit operates from DC voltage, then only the remote power charger unit needs to comply. If a conflict occurs between EMC compliance and product safety, safety takes precedence. No exception to this requirement exists.

Electric shock occurs when current passes through the human body. Currents on the order of a milliampere can cause a reaction in persons of good health and may cause indirect danger due to involuntary reaction. Higher currents can have more damaging effects. Voltages up to 42.4 VAC peak, or 60 Vdc, are not generally regarded as dangerous under dry conditions. Electrical parts that have to be touched or handled should be at earth potential or properly insulated to prevent electric shock.[1]

Under normal conditions, any voltage (absolute value) greater than 42.4 VAC peak, or 60 VDC, that may exist on a PCB (or system) is considered hazardous and requires special attention by a product safety compliance engineer.

How does all this discussion about hazardous voltages affect PCBs? Telecommunication circuits operate at –48Vac. Power supplies are sometimes provided on a PCB connected to AC mains voltage. Solenoids drive 115V or 230V motors. Process control equipment generally uses voltages above 42.4 VAC peak. These are only a few examples of PCBs that may contain hazardous voltages; hence, this chapter requires a discussion on safety grounds within PCBs.

In Fig. 9.2, the stray impedance between voltage potential (PCB) at point V_1 and chassis is identified as Z_1. The stray impedance between chassis and ground is identified as Z_2. The potential of the chassis is the impedance of Z_1 and Z_2 acting as a voltage divider. The chassis potential, relative to the PCB, is

$$V_{\text{chassis}} = \left(\frac{Z_2}{Z_1 + Z_2}\right) \tag{9.2}$$

This potential could reach hazardous levels, enough to cause a shock hazard to exist.

It must never be assumed that as long as everything is connected to earth ground through an appropriate means (green/yellow wire, braid strap, and the like), then all is well. This ground wire will have a high impedance at RF frequencies which varies as the frequency varies. In general, safety earth ground is not required for EMC compliance. Examples are battery-powered units. A good low-impedance connection to an RF reference point provided by a local chassis, frame, or other metallic structure is necessary and in many instances must be provided in parallel with safety earth ground for those devices connected to an AC mains source.

[1]This description of electric shock hazard is extracted from the international product safety standard, EN 60950, *Specification for safety of information technology equipment, including electrical business equipment.*

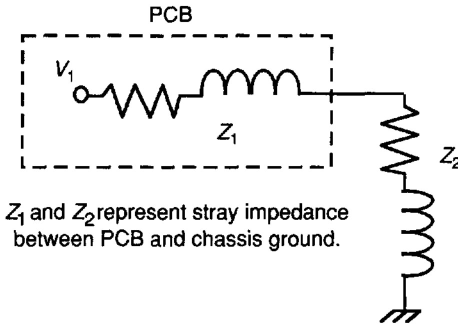


Figure 9.2 Stray impedance from PCB to chassis ground.

If we observe common-mode emissions emanating from a power cord, a safety earth ground connection may be required. A line filter can be installed at the mains power inlet which places the line filter in series between the mains wall receptacle and the system. Internal to the line filter are capacitors from line to ground ("Y" capacitors) which shunt the RF currents to ground. For this application, the ground wire is a return path for RF currents.

At times it is beneficial that the safety earth ground path be removed from the RF generation circuit [8]. This is best accomplished by inserting a choke (RF conductor) in series with the earth return. This choke provides an alternative path for interference currents to remain within the system. These currents are hopefully prevented from radiating to the external environment by a Faraday shield or Gaussian structure (sheet metal covers).

To summarize, a voltage potential at hazardous levels must not exist. Under an abnormal fault condition, such as the PCB shorting out and energizing a metal chassis housing, the housing can assume full-voltage potential and create a shock hazard.

9.5 SIGNAL VOLTAGE REFERENCING GROUND

The majority of design concerns related to EMC compliance lies in signal ground and referencing one circuit to another. As discussed earlier, both source and load must be at the same voltage reference level for proper functionality. Logic circuits base their voltage transition states at a 0V reference level. If the reference level between two circuits is not the same, functionality concerns occur such as noise margin erosion and threshold levels for logic switching (in addition to the creation of a ground-noise voltage). This ground-noise voltage will cause common-mode currents to be developed, which is exactly what is not wanted.

A *ground* is usually defined as an equipotential point that serves as a reference potential between two or more items. This term is not representative of actual applications, since digital ground may be completely different from analog ground, which may also be different from chassis ground. This term also does not emphasize the return path that currents at RF frequencies take. There may be less inductance between a noisy circuit and a ground point than the connection to an equipotential point. RF current will always take the path of "least impedance." At low frequencies, where $R >> \omega L$, the current will take

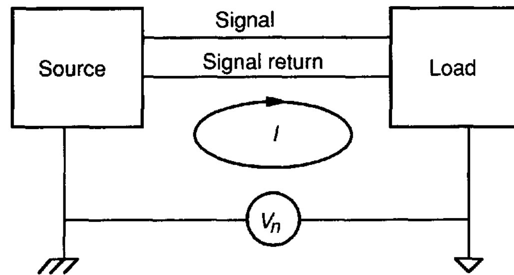


Figure 9.3 Typical grounding observed between two circuits. (*Source:* H. Ott, *Noise Reduction Techniques in Electronics Systems*, 2nd edition © 1988. Reprinted by permission of John Wiley & Sons, Inc.)

the path of least resistance, as resistance dominates the impedance. At high frequencies, $R << \omega L$, inductance dominates.

A better definition of signal ground is a low-impedance path for signal current to return to its source. This is applicable to any application or environment. Current is the item of concern, not voltage. If a voltage difference exists between two circuit points through a finite impedance, current will be created (Ohm's law). The current path in the ground structure determines the magnetic coupling between circuits. Since a closed-loop path is present, with current flowing in the loop, a magnetic field is developed (see Chapter 2). The physical size of the loop area determines the frequency of the radiated emissions. The current level determines the amplitude of the radiated noise.

Designers must always keep in mind the path that RF current will take during a product design. They cannot concern themselves only with functionality and with how well their chosen logic devices work based on simulation data. The design engineer and PCB designer must work together to ascertain the anticipated path through which the return currents will flow during component placement. The question to ask is, "Where will the current flow?" Any conductor carrying current will have a voltage drop associated with it, along with its corresponding current. This current is usually at RF potentials.

The signal ground system is determined by the type of product design, frequency of operation, logic devices used, I/O interconnects, analog and digital circuits, and product safety (electrical shock hazard).

A typical grounding scheme used to describe the signal ground concept is shown in Fig. 9.3 where the load is connected to one ground reference point and the source is connected to another reference. Ground-noise voltage, V_n, is caused by losses in the return path.

In implementing a grounding methodology, two basic categories exist, single-point and multipoint. Within each methodology, hybrid combinations may exist. The signal ground methodology that is best for a particular application is dependent on the design. Several different methods may be used at the same time, only if the designer understands the concept of current flow and return paths.

9.6 GROUNDING METHODS

Many grounding methods and terms have been devised, including digital, analog, safety, signal, noisy, quiet, earth, single-point, and multipoint. Grounding methods must be specified and designed into a product and not be left to chance. Designing a good grounding

system is also cost effective in the long run. In any PCB, a choice must be made between two basic concepts of grounding; single versus multipoint. Interactions with other grounding methods can exist if they are planned for in advance. The choice of grounding is dependent on product application. It must be remembered, if single-point grounding is used, to be consistent in its application. The same rule exists for multipoint grounding. A multipoint ground should not be mixed with single-point ground unless the design allows for isolation or partitioning between planes and functional subsections!

The discussion that follows is divided into three main grounding concepts. These concepts are single-point, multipoint, and hybrid.

9.6.1 Single-point Grounding

A single-point ground connection is one in which ground returns are tied to a single reference point within a product design. The intent of this "holy" ground location is to prevent currents from two different subsystems (at different reference levels) from sharing the same or common return path for RF currents, thus producing common-impedance coupling.

Single-point grounding is best when the speed of components, circuits, interconnects, and the like is in the range of 1 MHz or less, which means that the effect of distributive transfer impedances is minimal. At higher frequencies, the inductance of the return path will start to become noticeable. At still higher frequencies, the impedance of the power planes and interconnect traces becomes noticeable. These impedances can be very high if the trace lengths coincide with odd multiples of a quarter-wavelength based on the edge rate of the periodic signals. With a finite impedance in the current return path, a voltage drop is developed, along with creation of unwanted RF currents.

Owing to the significant impedance at RF frequencies, these traces and ground conductors will act as loop antennas and radiate RF energy based on the physical size of the loop. A convoluted loop is still a loop, regardless of shape. At frequencies above 1 MHz, a single-point ground generally is not used for this reason. However, exceptions do exist if the design engineer recognizes the pitfalls and designs the product using highly specialized and advanced grounding techniques.

In Fig. 9.4, two methods are shown for single-point grounding: series and parallel connection. The series connection is in a daisychain fashion. This type of configuration allows common-impedance coupling between the ground reference of each subsystem, which is undesirable at frequencies above 1 MHz. This figure only shows the inductance

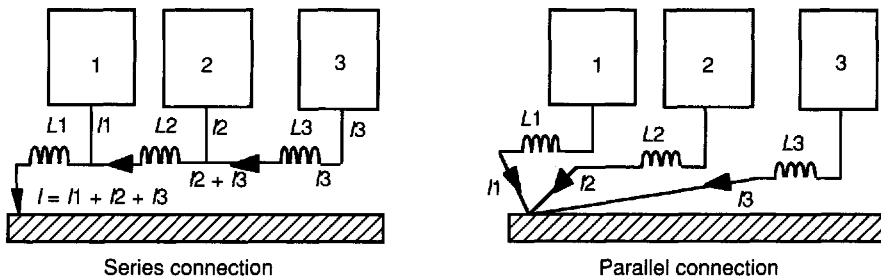


Figure 9.4 Single-point grounding methods. *Note:* Inappropriate for high-frequency operation.

within the ground path. Distributed capacitance is also present among the three circuits to ground. When both inductance and capacitance are present, a resonance will occur. For this configuration, three different resonances are possible.

For series connection, the total amount of current that is observed across the final return path L_1 is the summation of $I_1 + I_2 + I_3$. The voltage potential at I_1 (V_A) and I_3 (V_C) is also not at zero potential, and is described by

$$V_A = (I_1 + I_2 + I_3)\,\omega L_l \tag{9.3}$$

$$V_C = (I_1 + I_2 + I_3)\omega L_1 + (I_2 + I_3)\omega L_2 + (I_3)\omega L_3 \tag{9.4}$$

With this widely used configuration, a large amount of current across this finite impedance will produce a voltage drop. The voltage reference between circuits and the reference structure may be sufficient to cause the system to fail to work as desired. During the design cycle, one must be aware of the pitfalls of using series connection for single-point grounding. This grounding method should not be used when widely different power levels are present, since high-power consuming circuits produce large ground currents, which in turn will affect low-level components and circuits. If this method must be used, the most sensitive circuits must be located immediately at the input power location and as far away from low-level components and circuits.

A more optimal single-point ground method is parallel. Using this method has a disadvantage, however, in that each current return path may be at a different impedance value, thus exacerbating ground-noise voltage. If multiple PCBs are provided within an assembly, or if various subassemblies are combined within an end-use product, a particular return path may be physically long, especially if wires are used as the interconnect method. The ground wires may also possess a large impedance that will negate the desired effect of a low-impedance ground connection. Many products fail emissions testing when multiple PCBs are tied together in a parallel fashion, believing that a "holy" ground connection will solve their problems. Like series connection, distributive capacitance is also present from each circuit to ground. The designer should maintain the inductance value from each circuit to ground using this configuration to be approximately the same, but rarely is this the case. As a result, the resonance between each circuit to ground should be approximately the same and may not affect circuit operation to the extent multiple unique resonances will.

Another problem associated with using single-point grounding with wires is radiated coupling, which may occur between the wires, the wire and PCB, or the wire and chassis housing. (Internal radiated noise coupling is discussed later in this chapter.) In addition to RF radiated coupling, crosstalk may occur depending on the physical distance spacing between the current return paths. This coupling may occur by either capacitive or inductive means. The amount of crosstalk that may be present is dependent on the spectral content of the return signal. Higher frequency components will radiate more than lower frequency components.

Single-point grounds are usually found in audio circuits, analog instrumentation, 60-Hz and DC power systems, along with products packaged in plastic enclosures. Although single-point grounding is commonly used in low-frequency applications, it is occasionally found in extremely high-frequency circuits and systems. This application is permitted when a design team understands all the problems that exist with inductance in different ground return structures.

Use of single-point grounding on a CPU-motherboard or adapter (daughter) card allows loop currents to be present between the ground planes and chassis housing if metal is used as the chassis. Loop currents create magnetic fields. Ground loops are examined in greater detail later in this chapter.

Magnetic fields create electric fields, which will radiate RF currents. It is nearly impossible to effectively implement single-point grounding in personal computers and similar devices because different subassemblies and peripherals are grounded directly to the metal chassis in different locations. A distributed transfer impedance exists between the chassis and the PCB that inherently develops loop structures. Multipoint grounding places these loops in regions where they are least likely to cause problems (e.g., they can be controlled and directed rather than allowed to transfer energy inadvertently).

An example of poor implementation of single-point grounding is shown in Fig. 9.5. In this example, the A/D 0V reference is isolated within both the digital and analog section under the assumption that the open connection point (bridge) will provide optimal single-point connection as long as the analog section is not bonded to any other ground location. Single-ended signals are routed across the gap in the area of the converter's moat or isolated area. If low-frequency (kHz) noise frequencies are a problem, the 0V reference connection should be placed as near to the A/D device as possible. Analog and digital power must be isolated from each other referenced by an appropriate filter.

In Fig. 9.5, various current and voltage sources are present. RF return current travels through the bridge. The bridge provides a low-impedance RF return path for all signals that travel to the analog section by either crossing the moat or traveling through the bridge. Since a closed-loop path must be present for signal functionality, any RF energy crossing the moat must complete its return through the bridge.

Since a moat is present, a common-mode voltage potential will be developed at the point furthest from the bridge. The impedance between the two power sources will be different based on the inductance of the power and ground plane structure. With this common-mode voltage, a common-mode RF current loop current is developed, which travels through both the digital and analog sections. Once a loop is created with RF currents, a magnetic field structure exists, causing possible RF emissions.

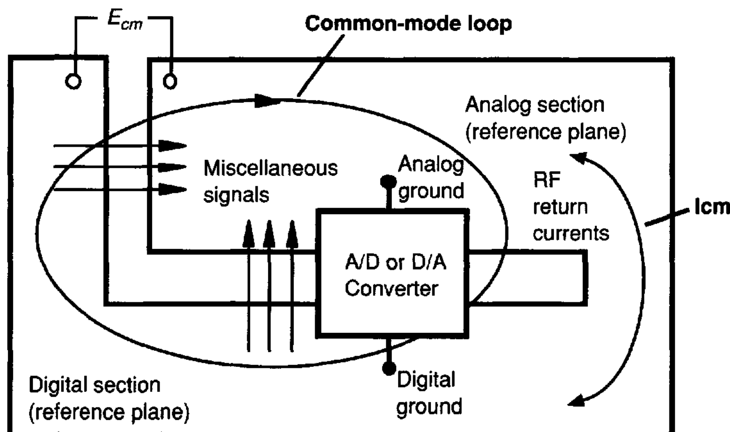


Figure 9.5 Bad implementation of single-point (connection) grounding.

Another bad implementation of single-point grounding in a multicircuit system is detailed in Fig. 9.6. The ground wires are noncurrent-carrying conductors (RF return path). The interconnect wires connected between circuits (Circuit #1 to Circuit #2 and Circuit #1 to Circuit #3) are identified as "GND" by the circuit designer or component manufacturer. These ground connections become part of the signal return path for currents that travel between circuits. These ground traces create an RF current loop, increase self-inductance of the traces, and develop a stray magnetic field between circuits and the 0V reference point. In addition, parasitic capacitance, C, between Circuit #1 and ground and Circuit #3 and ground is shown, along with inductance, L, from all circuits to the single-point ground connection. This small amount of LC may create a resonance that occurs at a frequency or harmonic of an oscillator, thus exacerbating systemwide problem.

To summarize, single-point grounding is not ideal when dealing with products operating above 1 MHz.

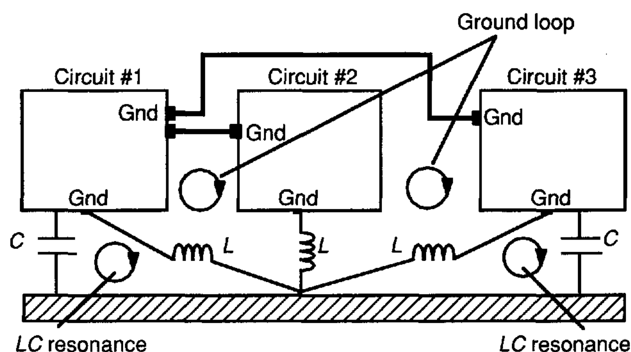


Figure 9.6 Another bad implementation of single-point grounding.

9.6.2 Multipoint Grounding

High-frequency designs generally require use of multiple chassis ground connections to a common reference point in order to minimize ground impedance. Multipoint grounding minimizes ground impedance present in the RF current return path because there are more low-impedance paths to take. Low planar impedance is caused primarily by the lower inductance characteristic of solid power and ground planes or by additional low-impedance ground stitch connection to the chassis reference point.

When a low-impedance ground plane is provided in a multilayer PCB, or a chassis ground stitch connection is provided between the PCB and metal chassis, it becomes important, like single-point grounding, that trace length (or wire length) be kept as short as possible to minimize lead-length inductance. In very high-frequency circuits, the length of the ground leads must be kept to a small fraction of an inch (cm). When using low-frequency circuits, multipoint grounds should be avoided since ground currents from all circuits flow through a common ground impedance, the ground plane. The common impedance of the ground plane can be reduced by using a different plating process on the surface of the material [2]. Increasing the thickness of the plane has no effect on minimizing plane impedance, for RF currents travel on the skin surface layer of the material.

A general rule of thumb is that for frequencies less than 1 MHz, single-point grounding is preferred. Between 1 MHz and 10 MHz, single-point grounding may be used only if the longest length trace or ground stitch connection is less than 1/20 of a wavelength, assuming long edge times and low-frequency spectra. Each and every trace must be considered.

Multipoint grounding minimizes inductance between noise generation circuits and a 0V reference point. This minimization occurs because many parallel RF current return paths exist in parallel, as illustrated in Fig. 9.7. Even with many parallel connections to a 0V reference, ground loops may still be created between each ground stitch location physically distant from other ground connections. These ground loops are prone to magnetic field pickup of ESD energy or creation of radiated EMI. To prevent loop currents between ground locations, it is important to measure the physical distance spacing between the ground connections and to implement the design technique identified in the section "Aspect Ratio" in Chapter 4, where the physical distance between two ground stitch connections should not exceed 1/20 of a wavelength of the highest frequency present within the functional subsection being grounded.

In very high-frequency circuits, lengths of ground leads from components must also be kept as short as possible. Trace lengths as long as 0.020 inch (0.005 mm) add inductance to a circuit of approximately 15–20 nH per inch (depending on trace width). This inductance may permit a resonance to occur when the distributed capacitance between the ground planes and chassis ground forms a tuned resonant circuit. The capacitance value, C, in Eq. (9.5) can be determined through knowledge of the impedance of copper planes. Impedance of cooper planes is discussed in Chapter 4.

$$Z = \frac{1}{2\pi f\sqrt{LC}} \tag{9.5}$$

where Z = impedance (ohms)
f = resonant frequency (Hz)
L = inductance of the circuit (henries)
C = capacitance of the circuit (farads)

Equation (9.5) describes most aspects of frequency domain concerns. This equation, though simple in form, requires knowledge of how to calculate both L and C, which by themselves are not easy to determine, use, and implement.

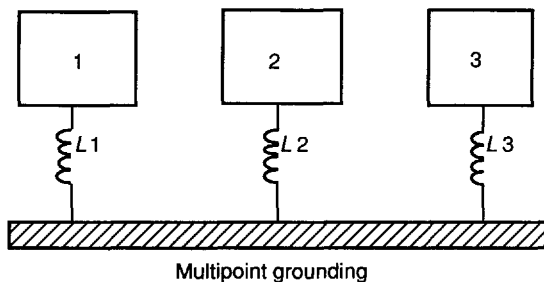


Figure 9.7 Multipoint grounding.

9.6.3 Hybrid or Selective Grounding

A hybrid ground structure is a combination of both single- and multipoint grounding. This configuration is used when mixed frequencies are present within a PCB. Figure 9.8 shows two hybrid ground methods. For the capacitive coupling version at low frequencies, the single-point configuration is dominant, whereas the multipoint configuration works at high frequencies. This is because the capacitor shunts high-frequency RF currents to ground after the single-point connection goes inductive. The key to success is understanding both the frequency present and desired direction of ground current flow.

The inductive coupling version is used when multiple ground stitch locations must be connected to a chassis ground reference for safety reasons and low-frequency connections. The chokes, *L*, prevent RF currents from entering the chassis ground, while allowing low-frequency AC or DC voltages to be referenced to their respective 0V point. The choke keeps the RF current internal to the PCB and forces the return currents to travel through the lowest impedance path to ground the single-point connection (wire), which is at a much lower impedance level than the chokes.

Using capacitors or inductors in a ground topology allows us to steer RF currents in a manner that is optimal for our design. One can take control of the PCB layout by defining the path that the RF currents will take. Failure to recognize the RF current return path may result in either emissions or susceptibility problems.

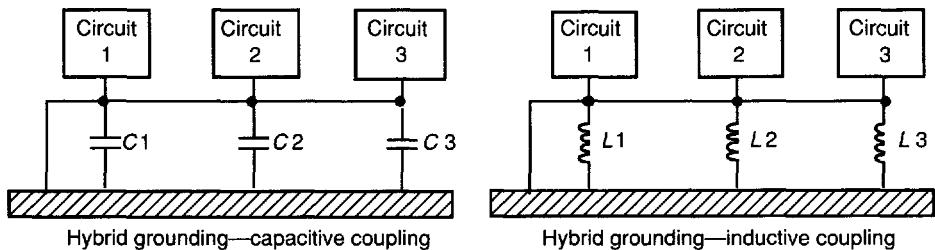


Figure 9.8 Hybrid grounding. (*Source:* H. Ott, *Noise Reduction Techniques in Electronics Systems* © 1988. Reprinted by permission of John Wiley & Sons.)

9.6.4 Grounding Analog Circuits

Many analog circuits are low frequency in operation. Single-point grounding is best for these sensitive circuits but only at the "bridge" between digital and analog. The primary objective is to prevent large ground currents from other noisy components (digital logic, motors, power sources, relays) from sharing a sensitive analog ground path. Ground loops must also be avoided with all sensitive low-frequency analog circuits. With low-frequency analog circuits, it is easy to control both intended and unintended currents.

The degree of quiet required of the analog ground depends on the sensitivity of the analog inputs. The signal-to-noise ratio determines how much interference is allowed to exist before functionality concerns arise. For example, a low-level analog amplifier that requires a 10 μV input is more susceptible to disruption than a 10V input signal. Therefore, a very clean ground system must be present for the 10 μV input amplifier. For higher level analog circuits, ground requirements are less stringent.

Digital circuits affect analog components owing to switching noise from the logic gates internal to digital devices. Usually, there are many significant levels of ground bounce within the power and ground distribution in digital systems. High-speed CMOS components inject more noise into the ground reference than TTL because of higher peak switching currents. CMOS also creates more radiated emissions for the same reasons.

Separate ground references should be provided for both digital and analog, especially if sensitive analog circuits are present. A common reference point must still exist for D/A and A/D converters. This is best achieved at only one point on the PCB; two locations are not permitted at any time. It may sometimes be required to provide a passive filter, such as a ferrite bead between digital and analog circuits. These filters are effective at higher frequencies where parasitic capacitances will attempt to form a ground loop.

Occasionally, complete isolation must occur between analog and digital sections. This is best accomplished by use of optical isolators or isolation transformers, especially when extremely sensitive analog circuits are used alongside digital components.

9.6.5 Grounding Digital Circuits

With higher speed digital circuits, multipoint grounding is preferred because high-frequency currents are developed based on ground-noise voltage and the voltage drop across the layout field of the digital devices. The primary design objective is to acquire a uniform potential common-mode reference system. Single-point grounding does not work well for this reason as parasitics will alter the ground paths desired. Ground loops are usually not a digital problem, as long as a low ground reference impedance is maintained. Ground loops are discussed later in this chapter.

Many digital circuits do not require a ground reference source with filtering. Digital circuits have noise margins in the hundreds of mV and can typically withstand a ground-noise gradient of tens to hundreds of millivolts. Ground "image" planes within the multilayer board are optimal for signal currents, whereas multipoint grounding to chassis is desired to control common-mode return losses.

9.7 CONTROLLING COMMON-IMPEDANCE COUPLING BETWEEN TRACES

A concern associated with common-impedance coupling is to minimize the effects that occur when two metallic structures share a common return path. Two main concepts are used to control common-impedance coupling.

- Lowering the common impedance to a minimum value.
- Avoiding having a common-impedance path.

9.7.1 Lowering the Common-Impedance Path

A ground system requires a metal conductor: trace, wire, strap, chassis frame, PCB planes, and the like. All conductors have a frequency response dependent on the material and geometry. Any conductor will have a DC resistance by

$$R = \rho l/A \text{ (ohms)} \tag{9.6}$$

where R = DC resistance
l = length of the conductor in the direction of current flow (m)
A = cross-sectional area of the conductor perpendicular to the current flow (mm^2)
ρ = resistivity of the material (ohms • mm^2/m)

Resistivities, ρ, of various materials are

copper	$1.7 * 10^{-3}\ \Omega \cdot mm^2/m$
aluminum	$2.8 * 10^{-3}\ \Omega \cdot mm^2/m$
steel	$1.7 * 10^{-2}\ \Omega \cdot mm^2/m$

With common-impedance coupling, skin effect becomes a major factor. (Skin effect was briefly examined in Chapter 2.) As the frequency increases, current through a conductor will migrate toward the edge of the conductor identified as the skin. The area of the conductor available for current flow decreases while resistance increases. For a round conductor, skin effect is illustrated in Fig. 9.9.

Conductors have an intrinsic inductance value that is different from overall inductance. Overall inductance is also identified as external inductance, which is a function of loop area enclosed by the conductor. Internal inductance is not a function of this loop area. For a round conductor, internal inductance is

$$L = 0.2 \cdot l\left[ln\left(\frac{4l}{d}\right) - 1\right] \tag{9.7}$$

where L = internal inductance (μH)
l = conductor length (m)
d = conductor diameter (m)

This equation shows that inductance, L, increases linearly with length, l, while an increase in diameter, d, will reduce the total inductance logarithmically (a proportionally small degree only).

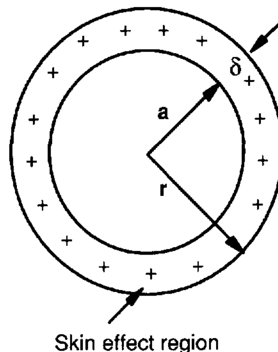


Figure 9.9 Current flow in a conductor—skin effect. (*Source:* Oren Hartal. *Electromagnetic Compatibility by Design* © 1994. Reprinted by permission of R&B Enterprises.)

Rectangular straps and multilayer power planes have a smaller inductance per unit length than that of round wire. The reason for this difference is that a flat strap (and extending this to a ground plane) has a larger perimeter than a round wire with the same cross-sectional area. Inductance of a ground strap is calculated as

$$L = 0.2 \cdot s\left(ln\frac{2s}{w} + 0.5 + 0.2\frac{w}{s}\right) \tag{9.8}$$

where L = inductance of the ground strap (μH)
s = strap length (m)
w = strap width (m) [must be larger than the thickness by a factor of 10 or more].

When $s/w > 4$ (length-to-width ratio), Eq. (9.8) can be approximated by

$$L = 0.2 \cdot s \cdot ln\frac{2s}{w} \tag{9.9}$$

Equation (9.9) shows that a strap has lower inductance than a round wire and is more useful as a method of providing a low-impedance ground connection at high frequencies. Extending this analysis to a solid plane internal to a PCB, we find that the plane has an impedance that is extremely small compared to a wire or strap except for the perturbations to the planes caused by annular anti-pads around vias. This is the primary reason why ground planes work as well as they do at high frequencies while minimizing common-impedance coupling.

9.7.2 Avoiding a Common-Impedance Path

To reduce common-impedance ground coupling, care must be taken to identify all return paths This is best achieved when all reference connections from different system circuits follow a dedicated and separate path to a single-point ground connection.

Figure 9.10 illustrates a star configuration for providing power and ground to various subsystems. This implementation technique requires additional wiring and interconnect hardware, not to mention cost.

To help implement an improved method of common impedance grounding, functional circuits must be separated by the power distribution network for each area in addi-

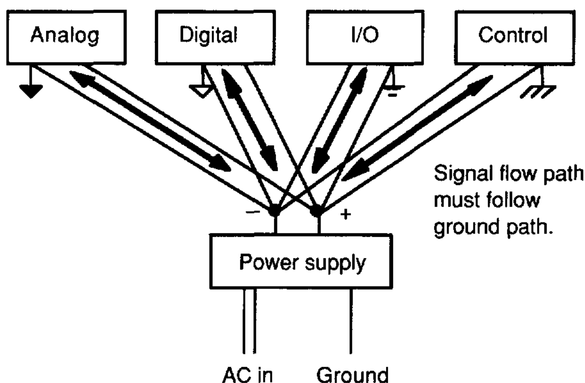


Figure 9.10 Separation of grounds to avoid common-impedance coupling. (*Source:* Oren Hartal, *Electromagnetic Compatibility by Design* © 1994. Reprinted by permission of R&B Enterprises.)

tion to the 0V reference required by logic circuitry. What this means is that we segregate circuits by logical function. Logical function includes the following list and does not include special circuitry that may be required or used, application dependent [4].

- Digital
- Analog
- Audio
- Video
- I/O
- Control logic
- Power supply

By separating noise-generating circuitry to prevent common-impedance coupling, increased noise immunity occurs. Each area must be connected by itself to the main 0V reference (as shown in Fig. 9.10), usually a safety wire ground connection.

As observed, preventing common-impedance coupling is best implemented with single-point grounding, which realistically may not be an option during the design cycle. As examined in the next section, single-point grounding is best when the signal within the circuit is 1 MHz or less containing low-frequency Fourier spectra, while multipoint is preferred for higher frequency signals.

What happens when a product must be multipoint grounded and when common-impedance coupling is to be avoided? For Fig. 9.11, a system must operate in a low-

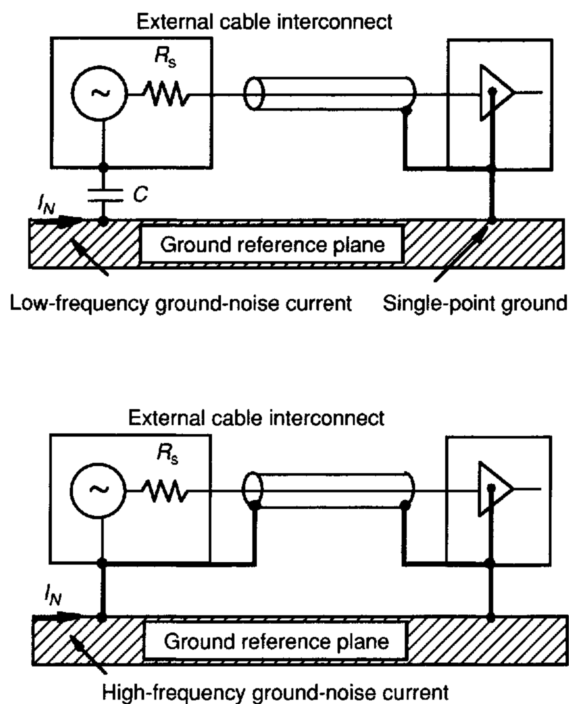


Figure 9.11 Single-point grounding for low frequencies and multipoint for higher frequencies.

frequency environment that requires single-point grounding. An I/O interconnect has high-frequency noise on the cable shield as a result of exposure to externally induced high-energy radiated fields. This cable shield must be single-point grounded if the frequency of operation is less than 1 MHz. For higher frequency signals, *both* ends of the cable shield must be connected to the 0V reference plane.

To solve this problem of attempting a single-point ground connection for low-frequency circuits, a bypass capacitor must be optimally selected for the frequency range of interest, and installed at the end of the cable shield, which is not DC connected to ground. (Optimal selection of this capacitor was described in Chapter 5.)

Other methods of avoiding common-impedance coupling, in addition to using single-point grounding, are available. These are use of an isolation transformer, common-mode choke, optical isolator, or balanced circuitry. These options are examined later in this chapter in the section "Ground Loops."

9.8 CONTROLLING COMMON-IMPEDANCE COUPLING IN POWER AND GROUND

When there are many circuits switching simultaneously, with widely different voltage and current swings (logic family dependent) and all powered from the same power distribution system, coupling of RF energy will probably occur between devices. The power distribution system will always have a finite impedance by virtue of its existence. With an impedance in the planes and with current being consumed by active logic devices, a voltage drop will occur. This voltage drop develops common-mode ground-noise voltage. (Ground-noise voltage is discussed in detail in Chapter 3.) Because a plane structure exists for an entire PCB assembly, ground-noise voltage that is present on one section of the board may be transmitted to other sections, causing both signal quality and EMC problems.

Figure 9.12 illustrates the concept of common-impedance coupling in the power and ground planes. The noise on Device 1's ground reference is described by

$$V_{\text{noise1}} = (I_1 + I_2)(R_{p1} + R_{g1} + Z) \tag{9.10}$$

If Device 2 consumes more current than device 1, with output impedance of the source negligible, we can determine the total amount of ground-noise voltage impressed across device 1. If device 1 is susceptible to disruption, serious concerns develop.

$$V_{\text{noise1}} = I_2(R_{p1} + R_{g1}) \tag{9.11}$$

When investigating a design to minimize common-impedance coupling within a power distribution system, one should take into account the impedance that is presented by that power distribution network. Depending on the design, the supplied voltage and return (ground) may be provided through use of round conductors or flat straps. Equation (9.12) illustrates the amount of inductance that will exist for various configurations. Knowledge of this inductance for these configurations will help the designer understand why RF noise created from one device causes harmful interference to another device. Table 9.1 provides information on the inductance of these conductors operating at 1 MHz [4].

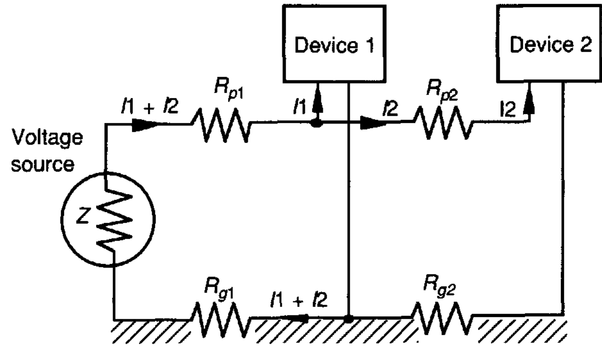


Figure 9.12 Common-impedance coupling in a power and ground structure.

$$Lo_{(\text{round})} = \frac{\mu_o s}{2\pi} \cdot \left[ln\left(\frac{4s}{d}\right) - 1\right] \quad \text{round conductor}$$

$$Lo'_{(\text{round})} = \frac{\mu_o s}{2\pi} \cdot ln\left(\frac{4h}{d}\right) \quad \text{round conductor over a plane} \tag{9.12}$$

$$Lo_{(\text{flat})} = \frac{\mu_o s}{2\pi} \cdot \left[ln\left(\frac{8s}{w}\right) - 1\right] \quad \text{flat strap}$$

$$Lo'_{(\text{flat})} = \frac{\mu_o s}{2\pi} \cdot ln\left(\frac{2\pi h}{w}\right) \quad \text{flat strap over a plane}$$

where s = conductor length (meters)
w = width of the conductor (mm)
h = height above ground plane (cm)
d = diameter of conductor (mm)
L = inductance (henry)
$\mu_o = 4\pi * 10^{-7}$

Inductance increases with the length of the conductor and decreases with width. With this increase, it becomes important to keep the length of the conductor as short as possible. Also, the wider the trace, the lower the impedance.

The best way to minimize common-impedance coupling within a power distribution system is to provide separate power and ground sources to specific switching devices. This works well with single- and double-sided PCBs. When separate power and ground

TABLE 9.1 Inductance of Various Conductors at 1 MHz

Conductor Type	Width (mm)	Length (m)	Diameter (mm)	Height (cm)	Inductance (μH)	Reactance (Ω)
Round	—	1	1		1.7	11
Round above a plane	—	1	1	1	0.7	4
Flat strap	10	1			1.3	8
Flat strap above a plane	10	1		1	0.37	2

Source: Oren Hartal, *Electromagnetic Compatibility by Design* © 1994. Reprinted by permission of R&B Enterprises.

planes exist in a multilayer stackup, common-impedance coupling is minimized due to the low impedance of the power distribution system.

9.9 GROUND LOOPS

Ground loops are a primary source of RF noise. RF noise is effectively produced when the physical distance between multipoint ground locations are significant (>1/20 of a wavelength) and connection is made to the main reference ground, usually at AC or chassis potential. In addition, low-level analog circuits can also create ground loops. When a ground loop occurs, it is necessary to isolate or prevent RF energy transference from one circuit corrupting other circuits. A ground loop consists of part signal path and part grounding structure.

Figure 9.13 illustrates what a ground loop looks like within a PCB that is mounted in a chassis where V_n represents common-mode ground loss within the PCB. I_{cm} represents the shunt of current V_n through the chassis. Two separate ground locations are provided, one for each circuit. A difference in ground reference exists between the two circuits due to its finite impedance that occurs between the common reference trace. Unwanted noise from one circuit may be injected into the other circuit. The magnitude of the ground-noise voltage, compared to the signal level in the circuit, is of prime importance. If the signal-to-noise margin is affected, design techniques must be implemented to ensure optimal circuit functionality. All components must have a reference point to determine where the 0V circuit reference is located such that the voltage-level transition is appropriate for the logic family used.

How does one avoid ground loops when a difference in 0V reference exists? Two primary design techniques may be used during the design and layout stages of the PCB.

- Remove one of the grounds (convert to a single-point system)
- Isolate the two circuits using any of the following:
  Transformer
  Common-mode choke
  Optic isolator, or
  Balanced circuitry

Figure 9.14 illustrates the circuit of Fig. 9.13 with modifications to reduce I_{cm}. The first modification provides ground-loop isolation using a transformer. When using a trans-

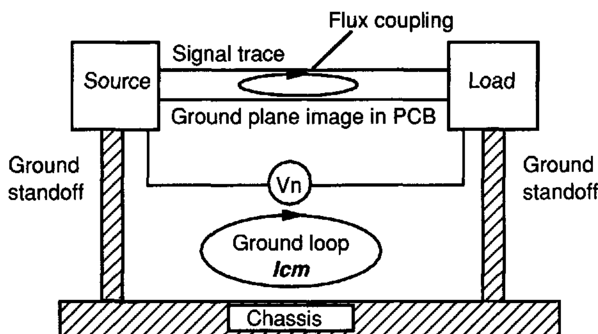


Figure 9.13 Ground loop between two circuits.

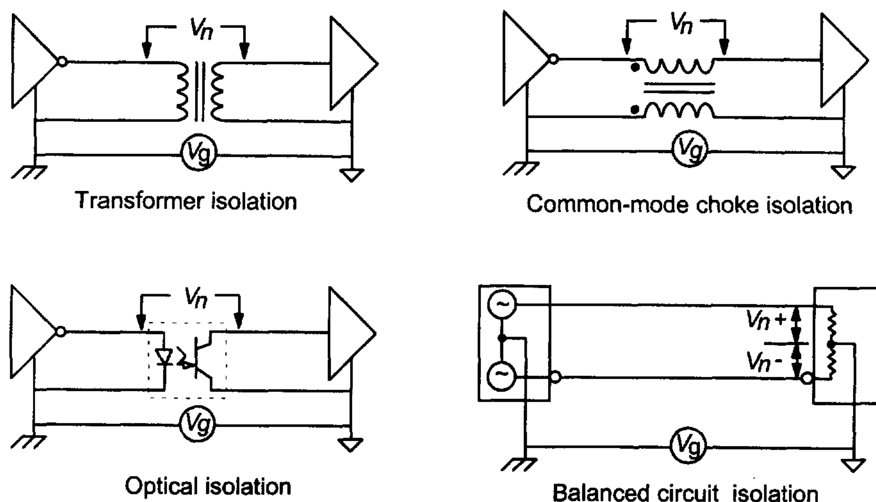


Figure 9.14 Breaking up ground loops between two circuits. (*Source:* H. Ott, *Noise Reduction Techniques in Electronics Systems* © 1988. Reprinted by permission of John Wiley & Sons.)

former, ground-noise voltage will be observed only at the input terminals of the transformer. Any noise coupling that occurs is a result of parasitic capacitance between the input and output windings of the transformer. To prevent parasitic capacitance, the use of a shield may be provided between the primary and secondary windings, connected to the main AC reference point or chassis ground. A disadvantage of using a transformer is physical size, amount of PCB real estate required, and additional cost. In addition, if multiple signals are to travel between isolated areas, a transformer is required for each signal.

Common-mode chokes are also shown in Fig. 9.14 as another technique. The advantage of using common-mode chokes is to remove common-mode currents. If the 0V reference between two components is not at the same reference level due to a finite impedance with the return path, the voltage drop observed will create common-mode noise. A common-mode choke will pass the DC level of the signal while attenuating the high-frequency AC component that is also present within the transmission line. The common-mode choke has no effect on the differential-mode signal of interest. It is the differential-mode signal we want, not common-mode currents. Multiple windings may be wrapped around the same core structure, increasing the density or number of signal lines that the choke can handle.

Optical isolation is another technique used to prevent ground loops and minimize I_{cm}. An optical isolator breaks the transmission path completely. A continuous metallic connection cannot occur between two circuits. This metallic connection is required for the propagation of an electromagnetic field down a PCB trace or wire. These isolators are best suited when a large voltage reference potential exists between circuits. Ground-noise voltage appears across the input of the optical transmitter. These optical isolators are best suited for digital logic designs owing to the nonlinearity of the device when used with analog circuitry.

Balanced circuits include using differential pairs to transmit a signal from source to load. By using differential transmission paths, the currents in both lines are equal. This balance causes a rejection of common-mode currents that may be present within the network.

Many differential-input components manufacturers provide a Common-Mode-Rejection-Ratio (CMRR) number within their data sheets. CMRR is defined as the ratio of

$$\frac{\text{common-mode voltage, } V_{cm}\text{, applied to both inputs required to generate output voltage, } V_o}{\text{differential voltage, } V_{dm}\text{, applied between the inputs to generate output } V_o}$$

CMRR identifies how much common-mode noise will be rejected from entering the device. The better the balance between the differential pairs, the greater the amount of common-mode rejection. At high frequencies, achieving a large CMRR value may be difficult to accomplish.

Common-Mode-Rejection-Ratio (CMMR) is mathematically defined as

$$\text{CMRR} = 20 \log \left| \frac{V_{cm}}{V_{dm}} \right| \text{ dB } \quad (V_0 = \text{constant}) \tag{9.13}$$

Using the circuit of Fig. 9.15, we can calculate CMMR as

$$\text{CMMR} = -20 \log \left| \frac{R_1(Z_b - Z_a)}{(Z_a + R_1)(Z_b + R_1)} \right| \text{dB} \tag{9.14}$$

One item to note in Fig. 9.15 is the location of the image plane and chassis plane. The differential-mode transmission line system is referenced from the 0V plane, not the chassis plane. Any I_{cm} that is developed between source and load must flow in the 0V (ground) reference. This distinction must be noted when using differential-mode components. The termination resistors, Z_a and Z_b, must be chosen with a tight tolerance value to assure impedance matching between the two traces. If an impedance imbalance is present, I_{cm} is increased. The development of I_{cm} is described in Chapter 4.

When using Eq. (9.14), the tolerance rating of the resistors is the critical parameter concerned, whereas the R_s resistors are provided to match transmission line impedance to ensure the functionality of the circuit.

When dealing with differential-mode circuits to minimize I_{cm}

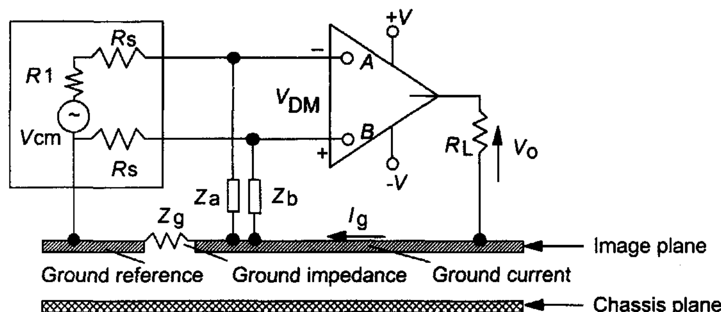


Figure 9.15 Circuit representing common-mode-rejection-ratio.

1. The impedance control of the signal lies only in the image plane.
2. Signal flux is bound to the internal image plane, not the chassis. The chassis is too far away to be of any significant value.
3. The chassis plane only shorts out the common-mode loss that occurs across the image plane.

9.10 RESONANCE IN MULTIPOINT GROUNDING

Problems that arise in PCBs using multipoint grounds are resonances that occur between ground stitch locations and the AC reference or chassis plane. While the AC reference or chassis plane may be at 0V potential referenced to a particular ground structure, this AC reference may be completely different from the 0V reference of the digital or analog circuitry. This difference in reference levels is more apparent when high-frequency, high edge rate signals are present.

Depending on the distance spacing between ground stitch locations, a resonance can occur, depending also on spectral excitation. This resonance exists because parasitic capacitance and inductance are also present between the power and ground planes, in addition to capacitance and inductance induced by the mounting ground stitch standoff mounting posts as shown in Fig. 9.16.

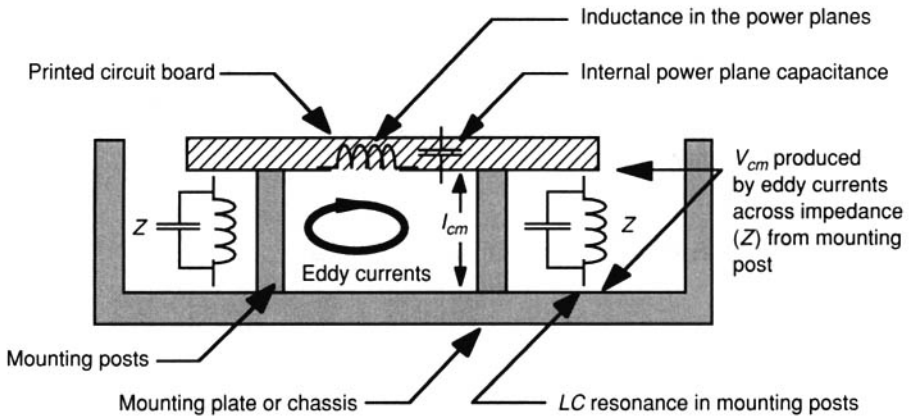
Figure 9.16 illustrates a PCB's image plane secured to a metal mounting plate. In this figure, we see that both capacitance and inductance are present. Capacitance exists between the power and ground planes internal to the PCB. The planes themselves have a finite impedance between ground stitch locations. Using Eq. (9.5), we can determine the self-resonant frequency of the power and ground plane structure, which is difficult to do mathematically. Use of a network analyzer will provide a quick way of determining the *actual* self-resonant frequency between ground points. Multiple measurements are required since the self-resonant frequency of the PCB is dependent on the inductance of the planes, based on the distance spacing of the network analyzer and ground locations for the test probe. Capacitance will, however, remain fixed between the power and ground planes.

Since the PCB's power and ground plane structure is self-resonant at various frequencies, the same analysis for self-resonance is applied to the metallic structure that is used to secure the PCB. This metallic structure may be a chassis for a motherboard, a mounting plate used in a cardcage with a backplane, a shield partition between two boards, or other application not identified herein. Again inductance will occur between the mounting standoffs relative to the actual location of the PCB. Now that we have identified inductance, what about the capacitance?

Because there is a finite distance between the PCB and the metallic structure, capacitance and transfer impedance exist. For example, the PCB can be considered as the positive plate of a capacitor, at voltage potential, and the metal structure as the negative plate, with air as the dielectric medium.

In addition to the overall inductance of the metallic material (which is extremely small), and the parasitic capacitance between the PCB and mounting plate, the standoffs used to secure the board to the chassis (generally pemstuds) are extremely inductive, as described below. These mountings are sometimes the cause of EMI failure.

The explanations of why the standoffs are inductive does not primarily have to do with the standoff itself, but with the metal screw used with the standoff. The screw con-



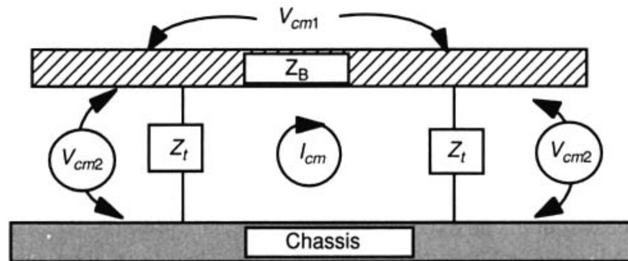


Figure 9.16 Resonance in a multipoint ground to chassis.

tains inductance that may be several orders of magnitude greater than the inductance of the PCB or parasitic inductance of the overall assembly. The reasons why screws are inductive is best illustrated in Fig. 9.17. It is difficult to model screw inductance because of the large number of parameters that cause this inductance to exist. Some of these parameters include material composition, the number of threads that makes contact with the standoff, thread spacing, pitch of the threads, plating material provided, compression strength, and length of the screw from top to bottom.

A screw contains a helical thread, and the edge of the screw thread is the part that mates with the standoff. We cannot guarantee that all threads will make 100% solid bonding contact with the standoff. The standoff must be physically larger in diameter than the screw diameter to allow the screw to be inserted. As a result, we will always have incidental contact between *some* of the threads, not the entire length of the screw. This is observed in Fig. 9.17.

A helical thread performs the same function as a helical antenna when a RF current travels through the screw. This current is located on an extremely thin surface of the helical thread because of skin effect. A voltage potential is developed between the bottom and top of the screw. This voltage reference difference exacerbates creation of RF current.

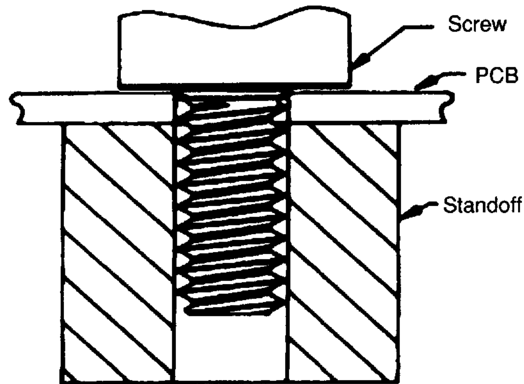


Figure 9.17 Problems grounding the PCB by screws to a standoff.

In addition to the helical thread, a coating of plating material is provided on the screw by its manufacturer. When metal-to-metal contact and rubbing occur between the screw and standoff, the plating can get scraped off, thus exposing the screw to the external environment and pollution based on intended application. Galvanic corrosion can develop, making the screw nonconductive (an insulator) in extreme conditions. If the intended application is to allow a low-impedance, common-mode ground reference path, one cannot exist if corrosion occurs. As such, a screw must be used only for compression between the PCB and metallic structure, and must not be relied upon to transfer RF currents to the 0V reference or ground system. Large mounting pads provided on the bottom of the PCB that overlaps the standoff walls help make the desired low-impedance ground connection, not the screw. The mounting pads of the PCB must be secured against the walls of the standoff. The standoff is usually installed in the chassis with a good bond connection by the sheet metal fabricator. Thus, if a low-impedance path to ground is required for the PCB, this is done through the walls of the standoff, not the screw threads!

Digital circuits must be treated as high-frequency analog circuits. A good low-inductive, 0V reference return is necessary on any PCB containing many digital circuits. The ground planes internal to the PCB (more so than the power planes) generally provide a lower inductive ground-image reference for the power supply and signal return currents. This allows use of constant impedance transmission lines for signal interconnects. When making a ground plane (0V reference) to chassis plane connection, it is necessary to provide for high-frequency decoupling of RF currents.

These high-frequency RF currents are created by the self-resonance of the power and ground plane structure losses caused by via anti-pad holes and the switching noise from digital circuits. High-quality decoupling capacitors should be used at each and every ground connection between the power and ground plane. Optimal selection of decoupling capacitors is detailed in Chapter 5.

9.11 FIELD TRANSFER COUPLING OF DAUGHTER CARDS TO CARD CAGE

RF fields generated from a PCB (components, ground loops, interconnect cables, and the like) will couple to a metallic structure. As a result, RF eddy currents will develop in the structure and will circulate within the unit creating a field distribution. This field distribu-

tion may then couple to other circuits, subsystems, interconnect cables, peripherals, and power supplies. One of the most significant ramifications of this field distribution is to develop a common-mode potential between a backplane and the metallic card cage. This potential will exhibit the spectral energy signature not only of the backplane, but the daughter cards as well. In addition, this field will be observed during radiated testing in the near field ($< \lambda/4$) or as a plane wave at a distance greater than $\lambda/4$ at the frequency of concern. Proper implementation of suppression techniques on a PCB, along with proper referencing of the backplane to the card cage to short out the distributively derived potentials, will minimize field transfer coupling between the boards to the backplane and card cage assembly.

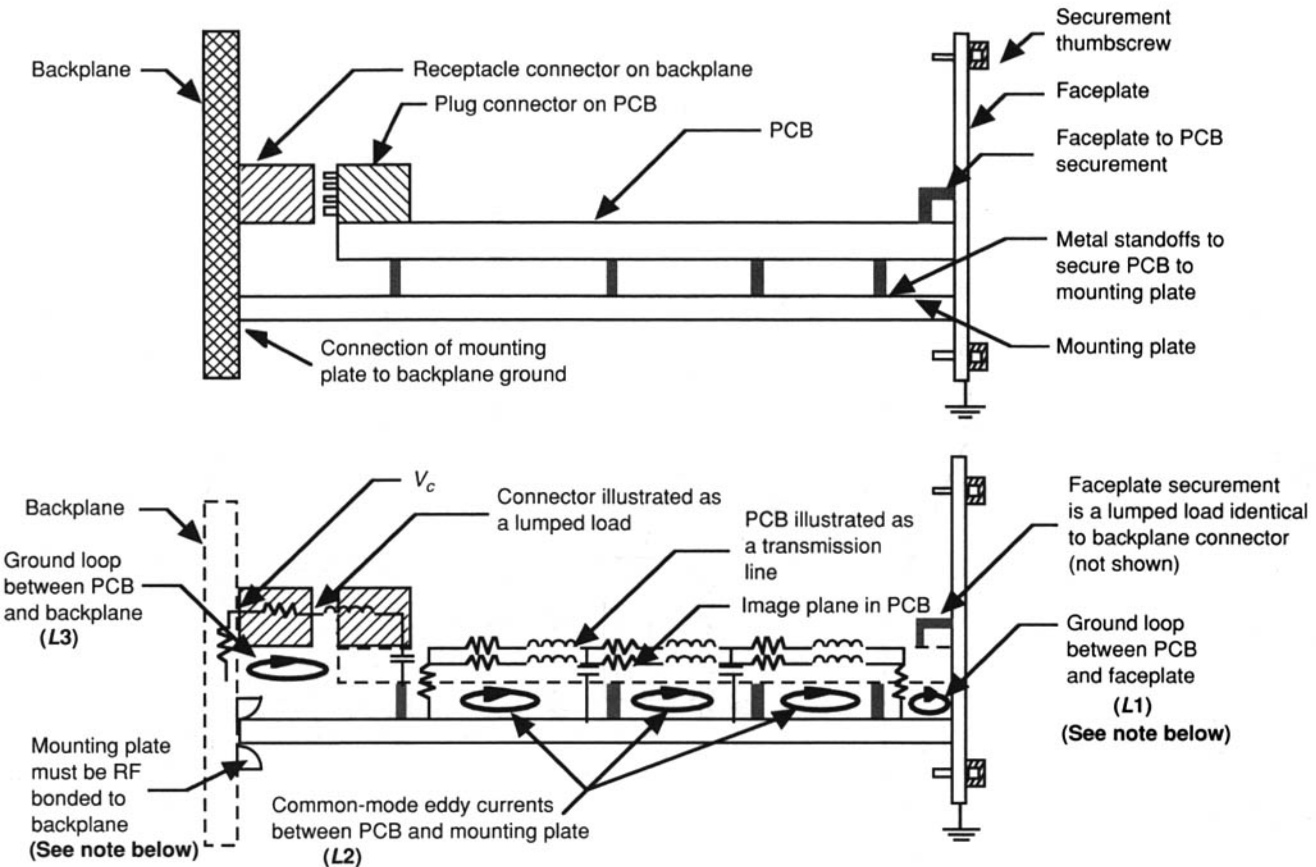
The *proper referencing* of the backplane to the card cage noted above takes the form of establishing a very low-impedance RF reference between the backplane and the card cage. This reference method is mandatory to short out the potentials caused by eddy currents developed at and by the daughter cards coupling to the sheet metal. These currents are coupled to the card cage through distributive transfer impedances (often in the low tens of ohms) and then through attempts to *close the loop* by coupling to the backplane. If the common-mode reference impedance between the backplane and the card cage is not significantly lower than the distributive "driving source" (of the eddy currents), an RF voltage will be developed between the backplane and the card cage. This voltage will have the spectral energy profile signature not only of the backplane but also of the daughter cards. This voltage will cause any interconnects that are provided on the backplane to radiate the spectral profile-even DC wire. The spectral voltage developed in this mechanism may contribute to interboard coupling using the backplane-to-card cage relationship as an intermediary![2]

Simply put, the common-mode spectral potential between the backplane and card cage must be shorted out. This may take the form of frequently connecting the backplane ground plane to the card cage (chassis) at regular intervals around the perimeter of the backplane. Alternatively, an "AC chassis plane" can be configured internal to the backplane, positioned immediately adjacent to a logic return plane. A distributive transfer impedance will thus be established between both the AC chassis and the return plane. The chassis plane may also serve as a Faraday partition within the assembly. The location of an AC chassis plane within the backplane must be such that it is never used as an image return reference for signal traces. That is, it must be "capped" by logic ground planes. Generally, to be reasonably effective, the RF transfer impedance between the logic ground planes and the AC chassis plane must be equal to or less than 1 Ω, thereby shorting out the common-mode potential between the daughter cards-card cage-backplane-to-card cage.

The reader is cautioned that the best EMI and system performance will be gained when the signal impedances are well controlled and referenced to ground planes (or 0V reference) rather than voltage planes. In addition, the intrinsic parallel-plane power impedance distribution must be established at as low a value as is reasonably possible.

In Fig. 9.18, if the top and bottom layer of the backplane or daughter card is a solid AC chassis plane, a lower impedance connection to chassis ground is available to both the backplane connector(s) and faceplate screw securement of the PCB. This low-impedance path will now source RF currents to chassis ground, thus preventing ground loops L_1 and L_3 from producing RF potentials between the faceplate to PCB and backplane to PCB, re-

[2]The propagational mechanisms and solutions were derived and modeled by W. Michael King.



Note: To control potential V_C, the mounting plate must be bonded to the backplane with a low-impedance connection. Without this connection, the mounting plate will couple (or transfer) common-mode eddy currents to the chassis or adjacent printed circuit boards. Common-mode eddy currents are to be avoided at all times if EMC compliance is required.

To control loop $L1$, the faceplate must be RF bonded to the mounting plate.

Figure 9.18 Backplane interconnect impedance considerations.

spectively. With solid bonding of logic ground to chassis ground, potentials from ground loop L_2 are also minimized.

All routing layers must be internal (stripline) to the backplane, with both top and bottom layers as solid AC chassis planes. With the outer layers an AC plane, direct chassis connection from logic ground to chassis ground can easily be achieved using bypass capacitors between the planes.

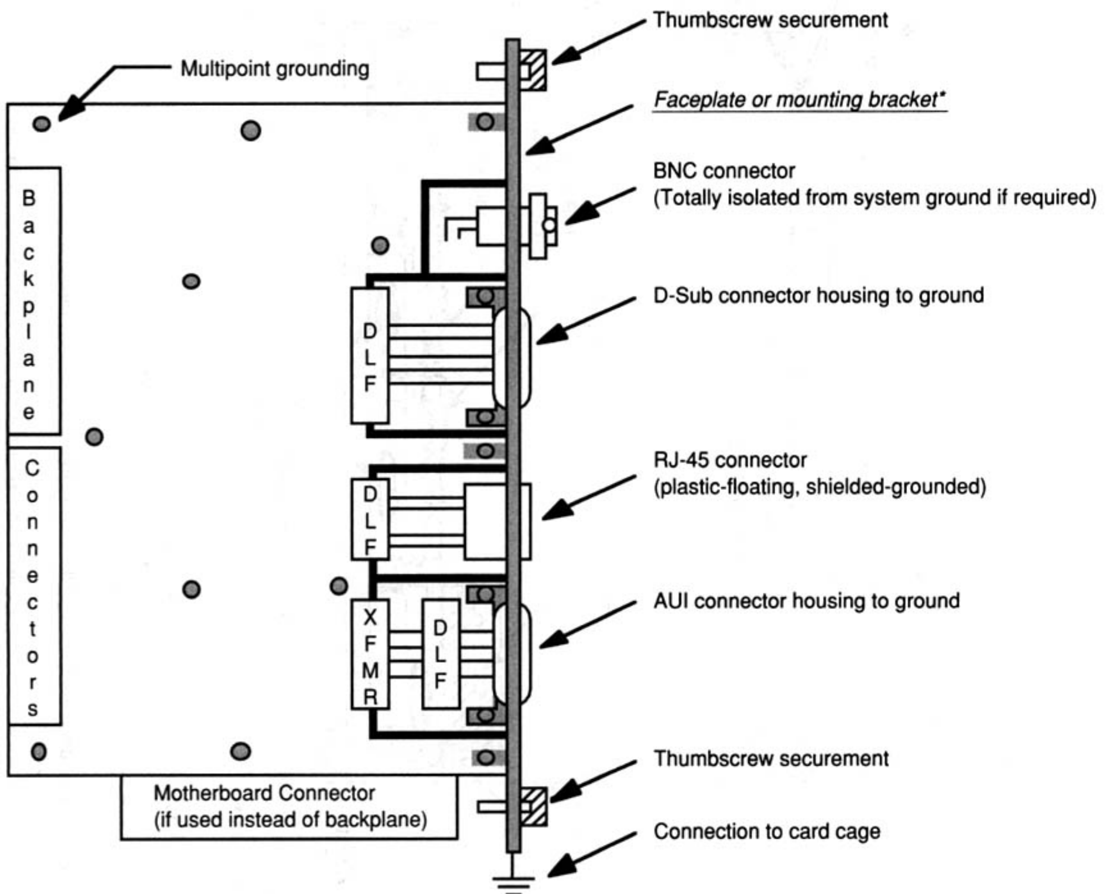


Figure 9.19 Multipoint grounding of I/O faceplate or bracket.

9.12 GROUNDING (I/O CONNECTOR)

For products that are low-frequency and that may use single-point grounding, this section is generally not applicable. For low-frequency products, low-impedance connection between logic ground and chassis ground not only can cause electromagnetic interference but can also prevent proper functionality. This is especially true for audio circuits that are devoid of digital processing. For a circuit at "low-frequency," to the extent that it qualifies for single-point grounding, the combination of signal levels, packaging techniques, and all operating frequencies must be such that transfer currents to the case (or external surfaces) through distributive transfer impedance is insignificant in comparison to the operative signal levels *or* the desired EMC criteria.

For products using *multipoint grounding*, this section is applicable whenever an I/O interface is used. Most modular PCBs contain a mounting bracket, faceplate, bulkhead connector, or securement means between control logic and the outside world. This securement may contain various I/O connectors, or it may be a blank panel (e.g., EISA/ISA/PCI adapter bracket). This bracket must be RF bonded by a low-impedance metal path directly to chassis ground. This bracket grounding may also be bonded to logic ground for functionality reasons.

Multiple ground connections must be provided from the ground planes of the PCB to the I/O bracket. Multiple ground points in the appropriate locations redirect RF ground loops between grounding locations on the bracket, distributive transfers to the case, and the opposite end of the PCB. The better the grounding, the more sourcing of RF currents to chassis ground. Figure 9.19 shows how to properly ground a mounting bracket to both chassis and logic ground. All I/O areas are isolated from control logic by a moat, which is also commonly identified as a partition cut, split plane, gap, or isolated area.

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