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8

Trace Termination

Before examining use of terminations, a thorough understanding of both the environment and the relationship that traces have to the overall PCB assembly must be achieved.

Trace termination plays an important role in ensuring optimal signal integrity as well as minimizing creation of RF energy. To prevent trace impedance problems and provide higher quality signal transfer between circuits, termination may be required. Transmission line effects in high-speed circuits and traces must always be considered. Even if the clock speed is low, say 4 MHz, and the driver and receiver are in the FCT family (2-ns edge rate), the reflections from a long trace route and fast edge rate can cause the receiver to double clock on a transition. Any signal that clocks a flip-flop is a possible candidate for causing transmission line effects regardless of the actual frequency of operation.

At what point in the design cycle should transmission line effects be considered? The following are some suggestions:

1. Clock lines, FIFO read and write strobe, and any signal that is used to latch or clock a flip-flop either externally in a circuit or internally in an off-the-shelf device (e.g., SIMM modules).
2. When using high-speed logic, such as ACT, FCT, FTTL, ASTTL, BCT, ABT, BTL, GTL, GaAs, or ECL.
3. CMOS components, as CMOS is susceptible to latch-up when a high-to-low transition goes much below the low-voltage transition state (approximately 2 volts).
4. On address and data lines when the designer is pushing the speed of the technology used, along with extremely fast edge rates on device inputs.

Less concern is generally given to transmission line effects with address and data signals, provided the system is synchronous. Designers must consider worst-case setup

and hold times with 2–4 ns of safety incorporated into the timing diagram. Designing in a safety margin guarantees that transmission line effects won't typically cause any harm as long as they have settled down by the time the clock or strobe latches them into a register. EMI problems may be increased however, if the signals ring and have overshoot and undershoot.

EXAMPLE

Given a 50-MHz signal (20 ns edge-to-edge), the minimum setup time for flip-flops is 2 ns. The worst-case delay from the source driver to the load is 17 ns. With this example, there is 1 ns to spare after accounting for setup time. If the trace is 6 inches long, transmission line effects will add approximately 2 ns, making the round-trip travel time 21 ns. There is a 1-ns delay over the desired requirements rather than 1 ns under.

8.1 TRANSMISSION LINE EFFECTS

When high-speed, fast edge rate signals are used within a digital design, transmission line effects are observed. Traces must be considered as a transmission line if the round-trip propagation delay of the signal traveling in the trace exceeds the switching-current transition time between logic states. Faster logic devices and their corresponding increase in edge rates are becoming more common in the sub-nanosecond range. A very long trace in a PCB can become an antenna for radiating RF currents or causing functionality problems.

A PCB trace looks very different for high signal speeds than it does at DC levels. For example, a typical PCB trace has a DC resistance of 12 milliohms per inch. When a signal wave propagates down a trace, the trace impedance will range from the few tens of ohms to as much as 100 ohms. Characteristic impedance is identified by the letter Z_o. Characteristic impedance is equal to the square root of L/C where L is inductance and C is capacitance. The ratio of voltage to current is constant only for a matched transmission line. The (x) subscript indicates variations along the line.

$$Z_o = \sqrt{\frac{L_o}{C_o}} = \frac{V_{(x)}}{I_{(x)}} = \frac{V_{(x)}^{+} + V_{(x)}^{-}}{I_{(x)}^{+} - I_{(x)}^{-}} \tag{8.1}$$

where + = forward wave and − = reverse wave.

What mechanism makes transmission lines the preferred choice for data transfer? A transmission line provides a constant impedance path from a source to load without discontinuities. Discontinuities affect signal integrity and may corrupt the voltage levels of the intended signal to a nonfunctional value. Ringing, reflections, overshoot, undershoot, and crosstalk are also problem areas observed in traces that are not routed as a transmission line. If a shield is added to the transmission line, a coax exists. A coax is the best transmission line for signal functionality. This is in addition to minimizing, or preventing RF currents from being created and causing harmful interference to other electronic equipment. A shield around the transmission line also enhances RF immunity protection from externally generated RF sources.

If the load impedance is greater than the characteristic impedance of the trace, Z_o (transmission line), positive reflections will occur. This will result in a higher voltage level at the load than that of the voltage supply, for example, a 6.5V signal with a 5.0V voltage source. If the termination impedance is less than the characteristic impedance, a negative reflection will cause the termination voltage to be less than that of the signal source. Reflections create overshoots. Overshoots affect adjacent lines or traces, as coupling is enhanced by the larger amount of voltage that exists. This coupling may cause induced logic errors, increase edge transition times, and may affect signal timing requirements. When one load is at a logic HI state, and the other end of the transmission line is LOW (typical of TTL), ringing oscillatory resonances occur. The ringing "oscillatory" resonance allows overshoot to alternate in consecutive reflections. The conditions described are illustrated in Fig. 8.1.

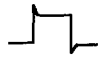
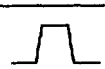
Source Z	Load Z	EMI results	Waveform at Load
Z_o	Z_o	None	
Z_o	High	Trace-trace coupling	
Z_o	Low	Edge rate changes	
Low	High	Trace coupling, EMI and crosstalk	

Figure 8.1 Transmission line effects. (*Source:* Oren Hartal, *Electromagnetic Compatibility by Design*, © 1994. Reprinted by permission of R&B Enterprises.)

8.2 TERMINATION METHODOLOGIES

The need to terminate a PCB trace is based on several design criteria. The most important criterion is the existence of an electrically long trace within a PCB. (Electrically long traces are discussed in Chapter 7.) In this chapter, the length of a routed trace on the PCB is discussed before termination is required. When a trace is electrically long, or when the length exceeds one-sixth of the electrical length of the edge rate, the trace requires termination. Even if a trace is short, termination may still be required if the load is capacitive or highly inductive to prevent ringing.

The easiest way to terminate is to use a resistive element. Two basic configurations exist, source and load. Several methodologies are available for these configurations. The five most commonly used termination methods are as follows and are detailed in Fig. 8.2. A summary of termination methods is presented in Table 8.1. Each termination method is discussed in depth in this chapter.

1. Series termination
2. Parallel termination

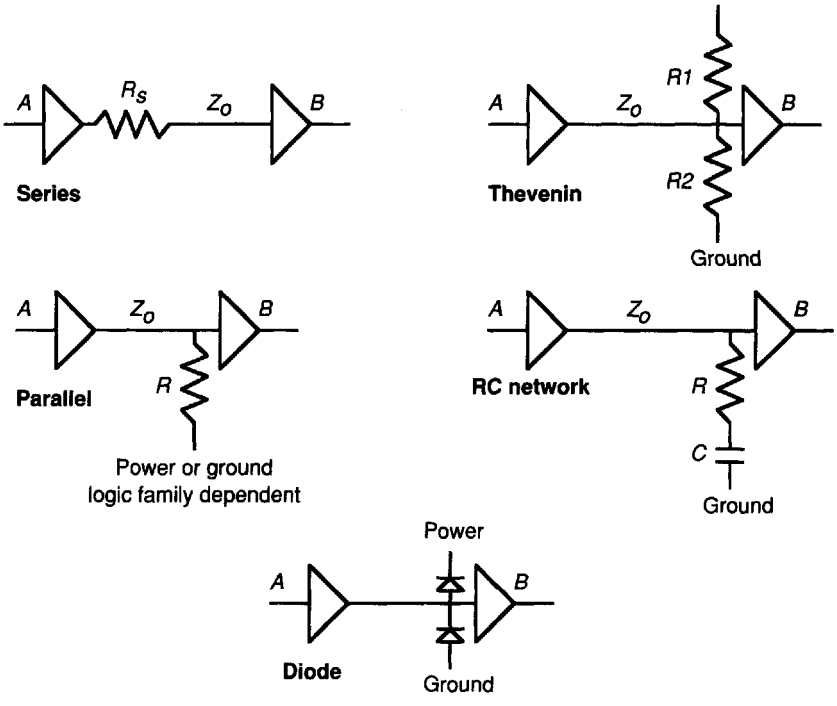


Figure 8.2 Common termination methods.

3. Thevenin network
4. RC network
5. Diode network

Termination not only matches trace impedance and removes (or reduces) ringing and reflections, it may also sometimes slow down the edge rate of the clock signal if incorrect values are applied. Inappropriate termination may degrade signal amplitude and integrity to the point of nonfunctionality. Reducing either dI/dt or dV/dt within the trace will reduce the creation of RF currents generated by high-amplitude voltage and current levels.

Another way to describe this dI/dt and dV/dt concern is to relate these functions to Ohm's law, $V = IR$. The following text demonstrates very briefly how to translate Ohm's

TABLE 8.1 Termination Types and Their Properties

Termination Type	Added Parts	Delay Added	Power Required	Parts Values	Comments
Series	1	Yes	Low	$R_s = Z_o - R_o$	Good DC noise margin
Parallel	1	Small	High	$R = Z_o$	Power consumption is a problem
Thevenin	2	Small	High	$R = 2 * Z_o$	High power for CMOS
RC	2	Small	Medium	$R = Z_o$ C = 20–600 pF	Check bandwidth and added capacitance
Diode	2	Small	Low	—	Limits undershoot; some ringing at diodes

law into a "simple" electromagnetic concepts using the equation $V_{ref} = I_{RF}*Z$. If the impedance (Z) of the trace remains constant, then both dV (RF voltage) and dI (RF current) will increase or decrease with the time-variant pulse of the signal. With less RF voltage and RF current, less radiated or conductive RF energy is generated, along with all the EMI undesirable side effects; hence, EMI performance improves. In addition to less RF currents, the edge rate of the signal may also be increased (slower edge rate), along with a reduction of spectral RF energy. However, if the value of Z is too large, then nonfunctionality may occur due to excessive signal degradation. To guarantee proper functionality at all times, Z must be optimally calculated.

Before the different termination methodologies are examined, a baseline network is provided. The following discussions are based on the simple model of Fig. 8.3.

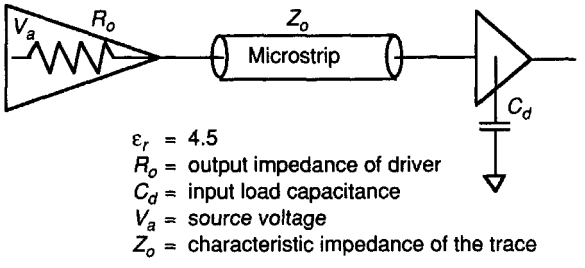
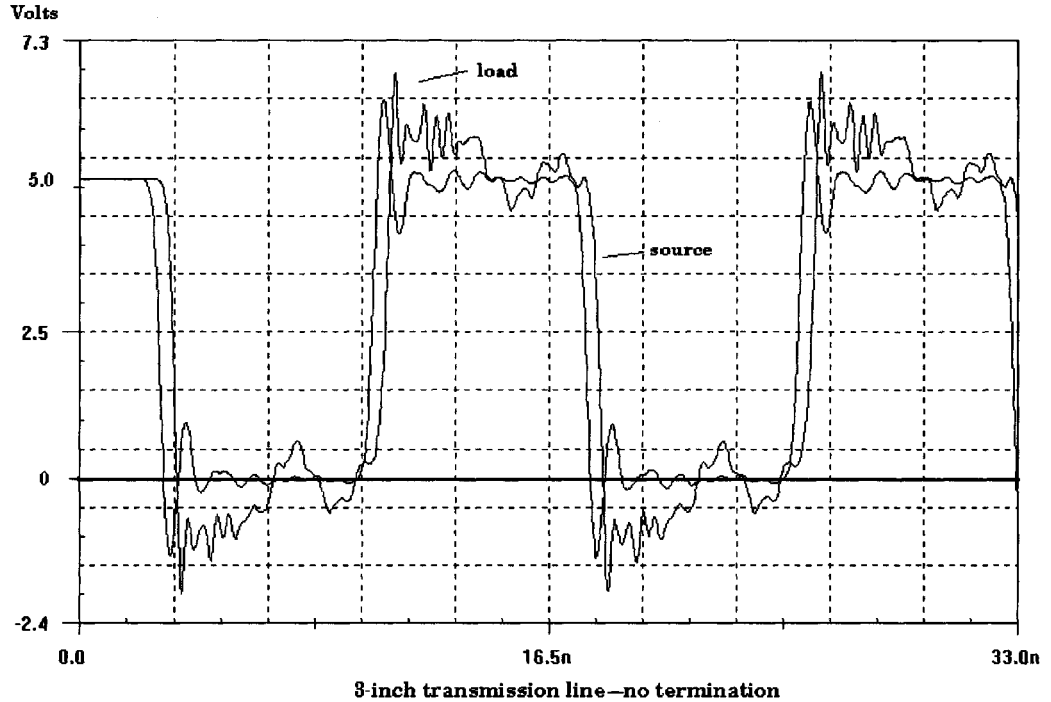


Figure 8.3 Simple baseline model for reference purposes.

Using this baseline model, we can examine the two simulation plots in Fig. 8.4. The edge rate of the driver is 0.8 ns for this 66-MHz, CMOS voltage level. Because components are going through die shrink and edge rates are decreasing, a realistic value of edge rate has been used in this analysis for clock drivers commonly used within high-technology products.

One plot shows the effects of this simple model using a 3-inch (7.6-cm) trace. The other plot shows an 18-inch (45.7-cm) trace, typical of a PCB layout in many designs. Notice that no termination is provided. The electrically short trace, 3 inches, shows a nearly perfect waveform from the source, along with a typical waveform at the load with minor overshoot and undershoot, typical with an improperly designed transmission line. According to Chapter 6, an electrically long trace for an 0.8-ns signal is 5.8 inches, round-trip. The round-trip propagational delay for a 3-inch trace is 6 inches; hence, the value of 3 inches was chosen to approximate the breaking point for a long transmission line. If the trace were less than 3 inches, the signal at the load would be identical to that of the source driver.

The item of interest in Fig. 8.4 is the 18-inch trace. The propagation delay of a microstrip transmission line with an ε_r of 4.5 is 1.72 ns/ft (0.36 ns/cm). At 18 inches, the time it takes for signal propagation is 2.5 ns, one-way travel. As observed in the plot, the signal is received at the load 2.5 ns after the source signal leaves the driver. This is what occurs with propagational delay (path time) within a transmission line. For critical nets where timing skew is important, an engineer must learn what the finished routed length of a trace is in the PCB artwork prior to releasing the artwork for manufacturing. If SPICE or any other transmission path analysis is done on a typical 3-inch trace, and the PCB designer uses an 18-inch trace in a synchronous system operating at frequencies of 100 MHz and above, signal integrity concern becomes mandatory. Details on propagation delay within a PCB trace were presented in Chapter 6. The discussion that follows is based on this baseline data.



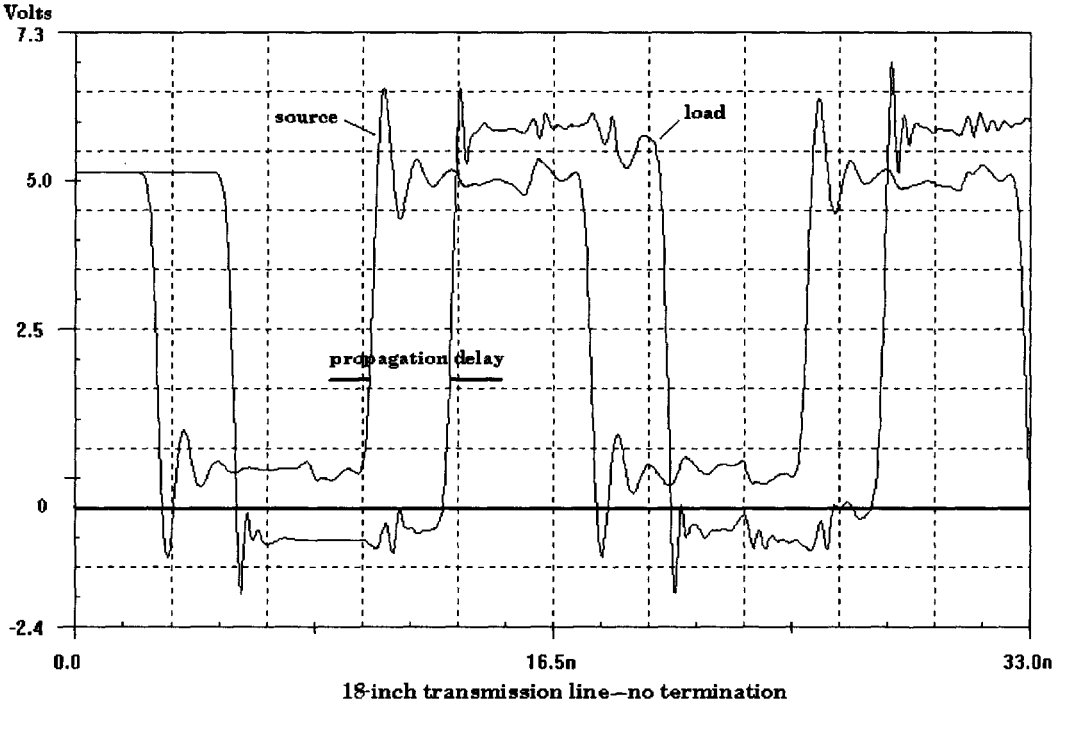


Figure 8.4 Baseline plots for reference purposes.

8.2.1 Source Termination

Source termination [3] provides a mechanism whereby the output impedance of the driver and resistor matches the impedance of the trace. The reflection coefficient at the source will be zero. Thus, a clean signal is observed at the load. In other words, the resistor absorbs the reflections.

The discussion that follows is summarized below.

1. A series termination provides a 50% reduction in drive voltage from the output of the resistor before traveling from source to load.
2. The reflected signal from the load will propagate back to the source at a 50% voltage level.
3. A reflection coefficient of +1 (open circuit) is observed at the far end. This means that the 50% reflected signal, plus the incoming 50% source signal, will add together and provide the full voltage level signal at the load without reflections.

8.2.2 Series Termination

Series termination is optimal when a lumped load or a single component is located at the end of a routed trace. A series resistor should be used when the driving device's output impedance, R_o, is less than Z_o, the loaded characteristic impedance of the trace. This resistor must be located *directly* at the output of the driver without use of a via between the component and resistor (Fig. 8.5). The series resistor, R_s, is calculated by

$$R_s = Z_o - R_o \tag{8.2}$$

where R_o = output resistance of the source driver
Z_o = characteristic impedance of the transmission line
R_s = series resistor

For example, if R_o = 22 Ω and trace impedance, Z_o = 55 ohms, R_s = 55 − 22 = 33 Ω. Use of a 33-ohm series resistor is common in today's high-technology products. The series resistor, R_s, can be calculated to be greater than or equal to the source impedance of the driving component and lower than or equal to the line impedance, Z_o. This value is typically between 15 and 75 (usually 33) ohms.

Series terminations minimize the effects of ringing and reflection. Source resistance plays a major role in allowing a signal to travel down a transmission line with maximum quality. If a source resistor does not exist, there will be very little damping. The system will ring for a long time (tens of nanoseconds). PCI drivers are optimal for this function because they have an extremely low-output impedance. A series resistor at the source that

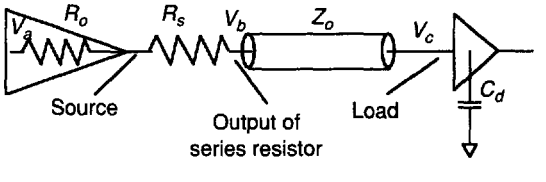


Figure 8.5 Series termination circuit.

is about two-thirds of the transmission line impedance will remove ringing. A target value for a *slightly underdamped system* (to make edges sharper) is to have $R_s = 2/3Z_o$. A wavefront of slightly more than half the power supply voltage proceeds down the transmission line and doubles at the open circuit far end, giving the voltage level desired at the load. The reflected wavefront is almost completely absorbed in the series resistor. Sophisticated drivers will attempt to match the transmission line impedance so that no external components are necessary.

When $R_s + R_o = Z_o$, the voltage waveform at the output of the series resistor is at one-half the voltage level sourced by the driver assuming a perfect voltage divider exists. For example, if the driver provides a 5V output, the output of the series resistor will be 2.5 volts. The reason for this is described by Eq. (8.3). If the receiver has high-input impedance, the full waveform will be observed immediately when received, while the source will receive the reflected waveform at $2 * t_{pd}$ (round-trip travel).

$$\Delta V_b = \Delta V_a \left(\frac{Z_o}{R_o + R_s + Z_o} \right) \tag{8.3}$$

Problems with Impedance Matching

The main problem with series termination is observed when the driving device has different output impedance values in both the LOW and HI states. This problem affects TTL logic and some CMOS devices as well. Both TTL and CMOS have different output impedances in both the logic HI and LOW state. This difference in output impedance, as well as the series resistor, may allow the trace impedance to vary from 55 Ω to 10 Ω depending on the logic state. This impedance mismatch condition may cause poor signal quality and possible nonfunctionality. In addition, certain load devices may have different input and output impedances that are not intuitively known. Hence, use of a series resistor may not be optimal under this condition of varying input/output impedances. Despite the compromises, it can still be effective.

The 1/2 V_{max} plateau can place the signal in an indeterminate logic state that can lead to improper operation should a bus structure be provided with multiple loads at various routed spacings. Signal integrity issues exist for multiple devices located on a routed bus, *except* for the receiver at the end of the net.

A well-designed CMOS clock driver should have approximately the same output impedance in both the HI and LOW logic state. This design requirement prevents many other termination problems from occurring. An additional advantage of using a series resistor is that a DC current path to ground or power is not set up. Without a DC current path, V_{OL} and V_{OH} levels are not degraded. If each clock output is driving only one device, series termination is the optimal choice. If a clock trace must connect to multiple loads or receivers, series termination is not the best choice.

When a device is sending a voltage-level transition down the transmission line, the source driver will see only the input impedance of the load which should be a high value. A series resistor is always located directly in the tranmission path. When the driver sends out a logic high signal, a direct path to ground through a low impedance (e.g., a pull-down resistor) will not occur. For a logic low state, the source driver will not consume power from the voltage source as if a pull-up resistor was in the circuit.

When a series resistor is used, the impedance of the trace is changed as a function of frequency, described by Eq. (8.4) where ω is frequency (in radians), L is series induc-

tance, and C is capacitance of the trace. It is observed that when R exceeds ωL, characteristic impedance becomes inversely proportional to the square root of the frequency available. This occurs at low frequencies when the wavelength is long and the line is electrically short. As a result, transmission line models are not valid for this case, and characteristic impedance is not of much concern. However, at high frequencies, when ωL exceeds R, the characteristic impedance becomes constant.

$$Z_o(\omega) = \sqrt{\frac{R + j\omega L}{j\omega C}} \tag{8.4}$$

Effects of Edge Rate Degradation

When series termination is used, the rise time of the signal can be affected, especially if the value of the resistance is not correctly selected. At any point along the transmission line, looking back toward the source, we see a drive impedance, Z_o. When a capacitive load is provided, a response is observed which appears as a simple RC low-pass filter with a time constant of

$$\tau = RC = Z_o C \tag{8.5}$$

Using Eq. (8.4) for the 10–90% rise time of an RC filter, it is possible to determine the value of the rise time degradation as

$$t_{(10-90)} = 2.2 Z_o C \tag{8.6}$$

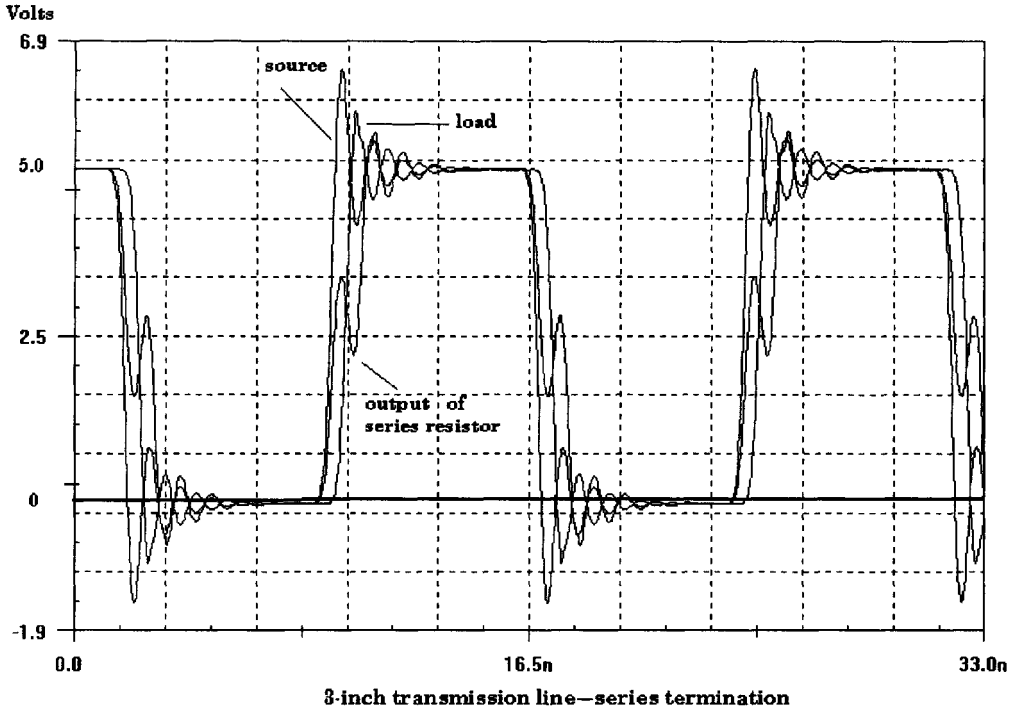
This rise time degradation is twice longer than the rise time of an end-terminated circuit. This condition occurs only if the transmission line impedance and load are the same.

Analysis of Series Termination

To better observe the effects of series termination and signal integrity, examine Fig. 8.6. This figure shows both the source and load voltages of a clock signal on a 3-inch and an 18-inch long trace. Both trace inductance and trace capacitance, in addition to load capacitance, play a role in these plots. The edge rate is 0.8 ns. The source is a clock skew driver with 66-MHz outputs. The 3-inch trace is electrically short, while the 18-inch trace is electrically long. One trace shows the signal directly at the output of the driver; the other trace is the output of the series resistor R_s; and the third trace is at the input of the load. Propagation delay at the load is described by $t_{pd} = 0.7\ (Z_o C_d)$, or the propagational delay equations detailed in Chapter 6 can be used if the values of $Z_o C_d$ are not known.

Interesting results are seen in Fig. 8.6. With an electrically short trace, a nearly perfect waveform is measured along the trace route for the 3-inch trace with typical ringing. The 1/2V at the output of the series resistor is easily observed. For the 18-inch trace, the waveform at the load is acceptable for signal integrity concerns, along with a noticeable 1/2V at the output of the series resistor. Both waveforms are nearly identical in appearance, except for the voltage level. A reduced voltage level at the output of the resistor does not affect the functionality of the signal. The item of interest is what is received at the load's input.

The same discussion regarding propagation delay of a transmission line detailed in the section "baseline" is applicable for series termination.



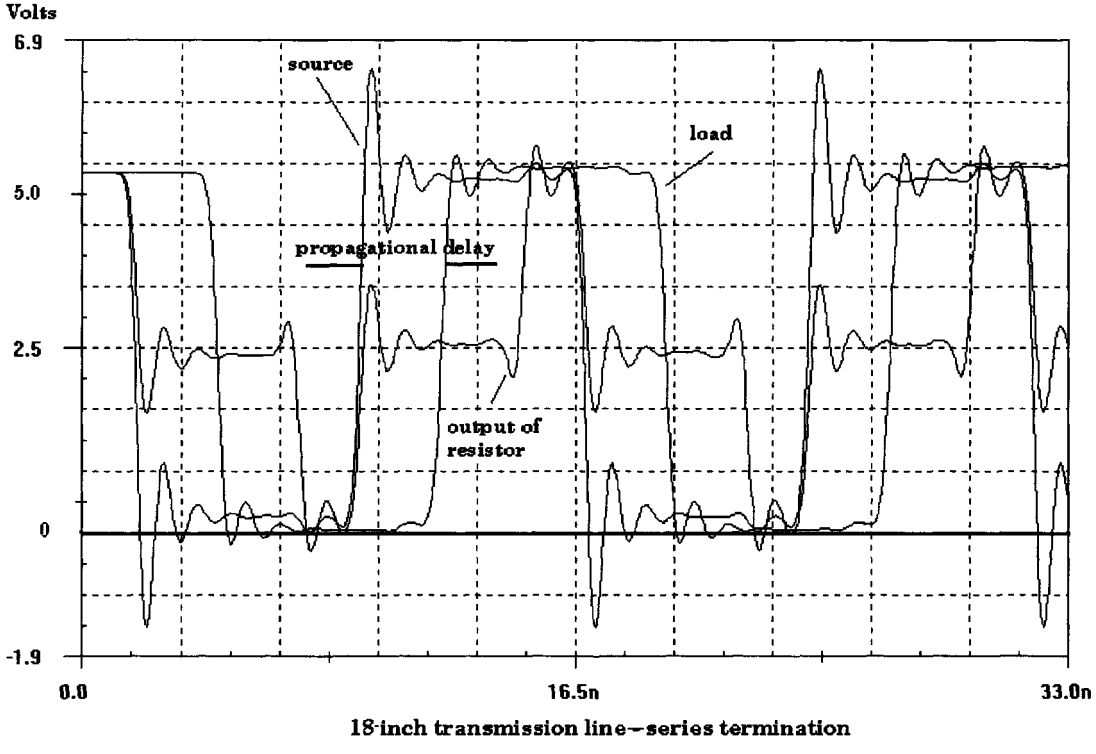


Figure 8.6 Series termination plots.

With a series termination resistor, minimal ringing is observed at the load compared to the unterminated trace shown in Fig. 8.4. This undistorted waveform is desired for signal functionality. An increase in propagation delay, however, is easily observed. The series resistor illustrates the masking of reflections. Both the 3-inch and 18-inch plots look nearly identical at the load because the circuit behaves identically when properly terminated, regardless of trace length. We can ignore the 6.6 V overshoot from the source.

Since $R_s + R_o = Z_o$, the voltage level at V_b (output of the series resistor) is one-half the voltage of V_a (source). The voltage waveform measured is divided evenly, with half of the voltage transmitted to the receiver. If the receiver had a very high-input impedance, the full waveform would have been observed at the load at t_{pd}, while the source would receive the reflected waveform at 2 * t_{pd} where t_{pd} is the one-way propagation delay.

When to Use Series Termination

Advantages of Series Termination

1. Series terminators can provide a slower rise time, which results in smaller residual reflections and less EMI.
2. Series resistors help reduce the spectral distribution of RF energy.
3. Series resistors reduce ground bounce.
4. Overshoot is reduced.
5. Signal quality/integrity is enhanced.
6. Minimal power dissipation occurs.
7. Distribution to multiple end-point loads from a common source (Fig. 8.7) is easily implemented.

Disadvantages of Series Termination

1. Series termination does not perform optimally when both TTL and CMOS devices are on the same net.
2. Series termination normally cannot be used when driving distributed loads because in the middle of the trace route, the voltage is only one-half the source voltage. Devices in the middle of a trace route will not get their proper voltage level until much later in the clock cycle.
3. Daisychain topologies are not appropriate with series termination, although a series resistor can be used with a parallel capacitor to slow down the edge time to extend beyond the propagation time of device interval reflections. All loads

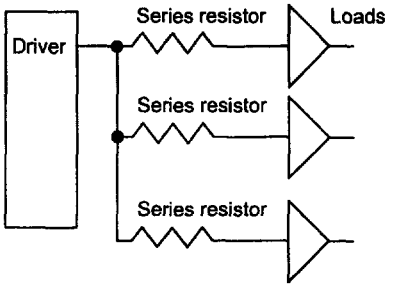


Figure 8.7 Distribution to multiple end-point load from a common source.

must be located at the end of the trace route. If a device is positioned somewhere between source and load, a distorted waveform will occur from improper voltage reference levels, along with possible reflections that may exist in the middle of the signal transmission path.

8.2.3 End Termination

End termination is used when multiple loads exist within a trace route. Multiple-source drivers may be connected to a bus structure or daisychained. The last device on a routed net is where the load termination must be positioned.

To summarize the discussion that follows.

1. The signal of interest travels down the transmission line at full voltage and current level without degradation.
2. The transmitted voltage level is observed at the load.
3. The termination will remove reflections by matching the line, thus damping out the overshoot and ringback.

There is a right way and a wrong way when placing end terminators on a PCB. This difference is shown in Fig. 8.8. Regardless of the method chosen, termination must occur at the "very end of the trace." For purposes of discussion, the RC method is shown in this figure.

Effects of Edge Rate Degradation

An interesting result occurs when termination is provided at the end of a trace route. This observation can describe the effects of edge rate degradation using a simple approach and the circuit of Fig. 8.9. This circuit is modeled as a Thevenin equivalent. The receiver appears as a capacitive load to the transmission line. For this simple circuit, the Thevenin equivalent of the impedance of the network is $Z_o/2$, assuming $R_s = R_L$, which is never the case in actual practice. The capacitor represents input shunt capacitance of the receiver.

When using end termination, the time constant or edge rate degradation is similar to Eq. (8.5) except the impedance of the circuit is $Z_o/2$, as shown in Eq. (8.7).

$$\tau = RC = Z_oC/2 \tag{8.7}$$

Also, similar to using Eq. (8.6) for the 10–90% rise time of an RC filter, the edge time degradation can determine the actual rise time degradation as

$$t_{(10\text{–}90)} = 2.2Z_oC/2 = 1.1\ Z_oC \tag{8.8}$$

For Eq. (8.8), the difference in edge rate degradation is assumed to be half that of series or source termination. This approximation is due to tolerances and variations within the network (transistors internal to the component plus discrete devices). For system critical nets where timing skew is important and synchronous operation must be assured, end termination may be a better choice.

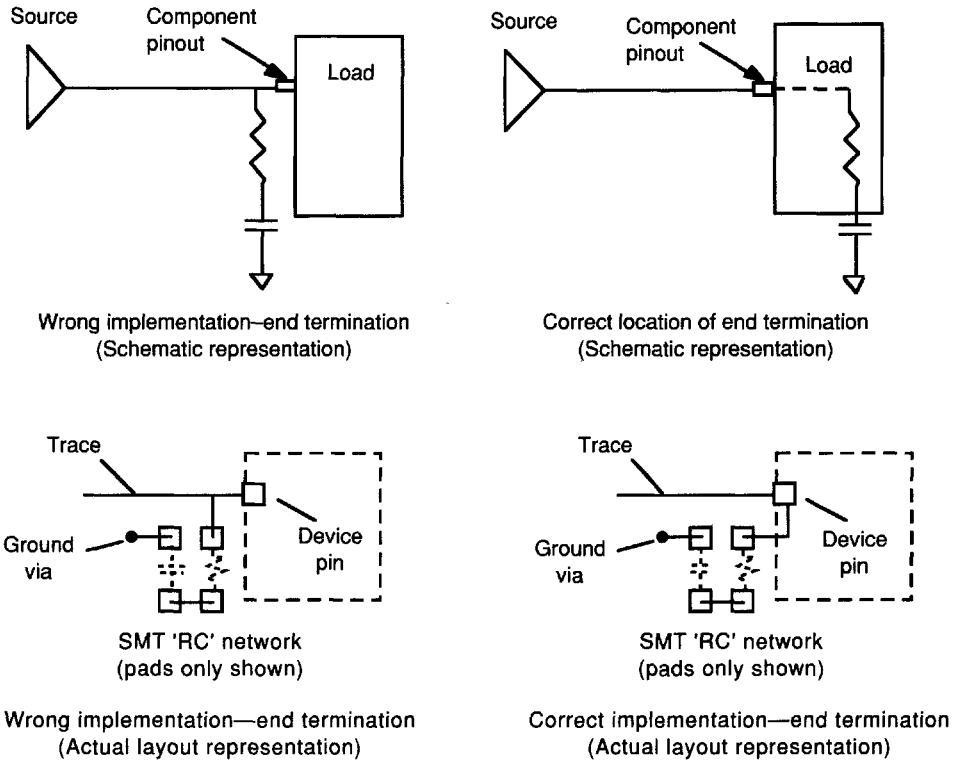


Figure 8.8 Locating end terminators on a PCB.

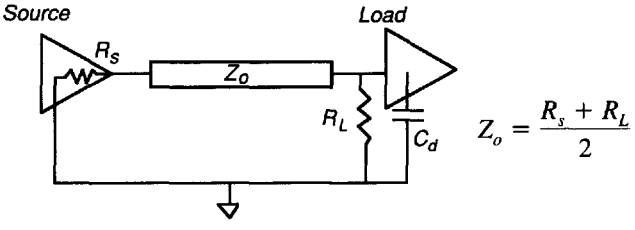


Figure 8.9 Equivalent circuit of end termination.

8.2.4 Parallel Termination

For simple parallel termination, a single resistor is provided at the end of the trace route (Fig. 8.10). This resistor, R, must have a value equal to the required impedance of the trace or transmission line. The other end of the resistor is tied to a reference source, generally ground. Parallel termination will add a small propagation delay to the signal due to the addition of the Z_oC time constant that is present in the network, described by Eq. (8.8). This equation includes the total impedance of the network. The termination resistor is only one component of the impedance equation. The total impedance, Z_o, is the result of the termination resistor, line impedance, and source output impedance. The C variable in the equation is the input shunt capacitance of the load.

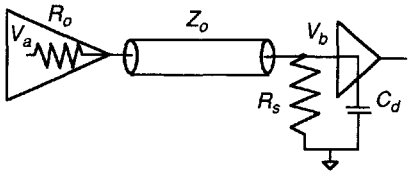


Figure 8.10 Parallel termination circuit.

A disadvantage of parallel termination is that this method consumes DC power, since the resistor is generally in the range of 50 to 150 Ω. In applications of critical device loading or where power consumption is critical, for example, battery-powered products (notebook computers), parallel termination is a poor choice. The driver must source current to the load. An increase in drive current will cause an increase in DC power consumption from the power supply, an undesirable feature in battery-operated products.

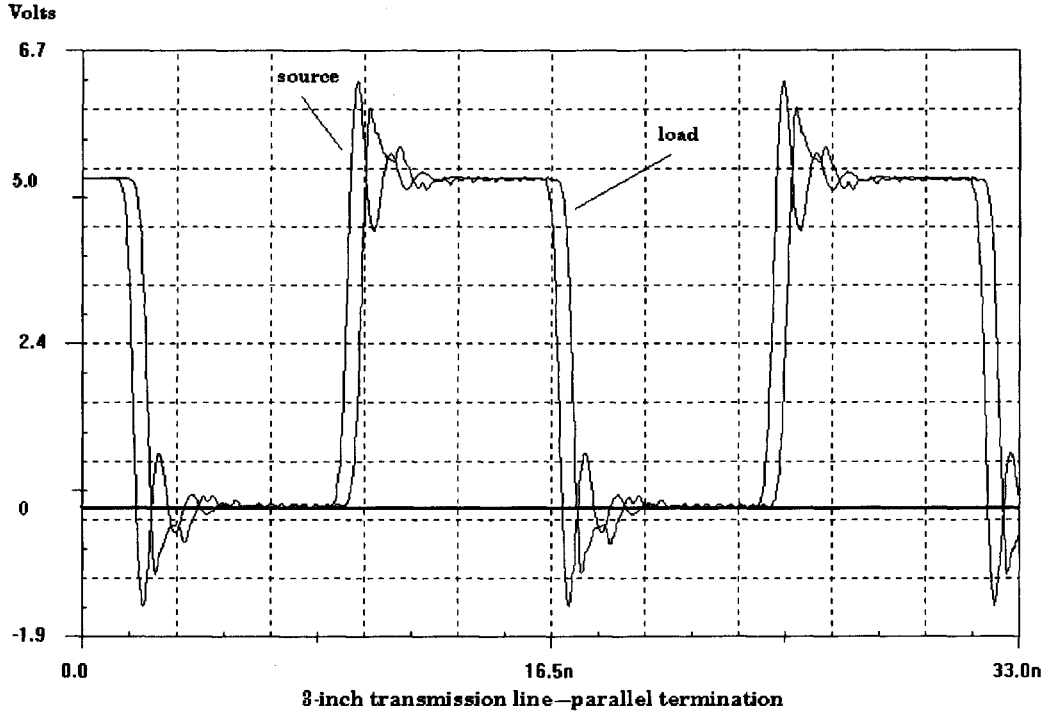
Simple parallel termination (resistive only) is rarely used in TTL or CMOS designs. This is because a large drive current is required in the HI logic state. When the source driver switches to V_{cc}, or logic HI, the driver must supply a current of V_{cc}/R to the termination resistor. When in the logic LOW state, no drive current exists. Assuming a 55 Ω transmission line, the current required for a 5V drive signal is 5V/55Ω = 91 mA. Very few drivers can source that much current! The drive requirements of TTL demand more current in the logic LOW state than logic HI. CMOS sources the same amount of current in both the LOW and HI logic states.

Since parallel termination creates a DC current path when the driver is in the HI state, excessive power dissipation and V_{OH} degradation (noise margin) occurs. A driver's output is always switching, thus DC current consumed by the termination resistor must exist. At higher frequencies, the AC switching current becomes the major component of the overall circuit. When using parallel termination, one should consider how much V_{OH} degradation is acceptable by the receivers.

When parallel termination is provided, the net result observed on an oscilloscope should be nearly identical to that of series, Thevenin or RC, since a properly terminated transmission line should respond the same regardless of the termination method used. This effect is observed in the various plots of termination methods provided in this chapter.

When using simple parallel termination, a single pull-down resistor is provided at the load. This allows fast circuit performance when driving distributed loads. This resistor has a Z_o value equal to the characteristic impedance of the trace and source driver. The other end of the resistor is tied to a reference point, usually ground. For ECL logic, the reference is power. The voltage level on the trace is described by Eq. (8.9). On PCB stackups that include Omega layers, parallel termination is commonly found. An Omega layer is a single layer within a multilayer stackup assignment that has resistors built into the copper plane using photo-resist material and laser etched for the desired resistance value. This termination method is extremely expensive and found in only high-technology products where component density is high and large pin-out devices physically leave no room for hundreds or even thousands of discrete termination resistors.

$$\Delta V_a = \Delta V_b \left(\frac{Z_o}{R_o + Z_o} \right) \tag{8.9}$$



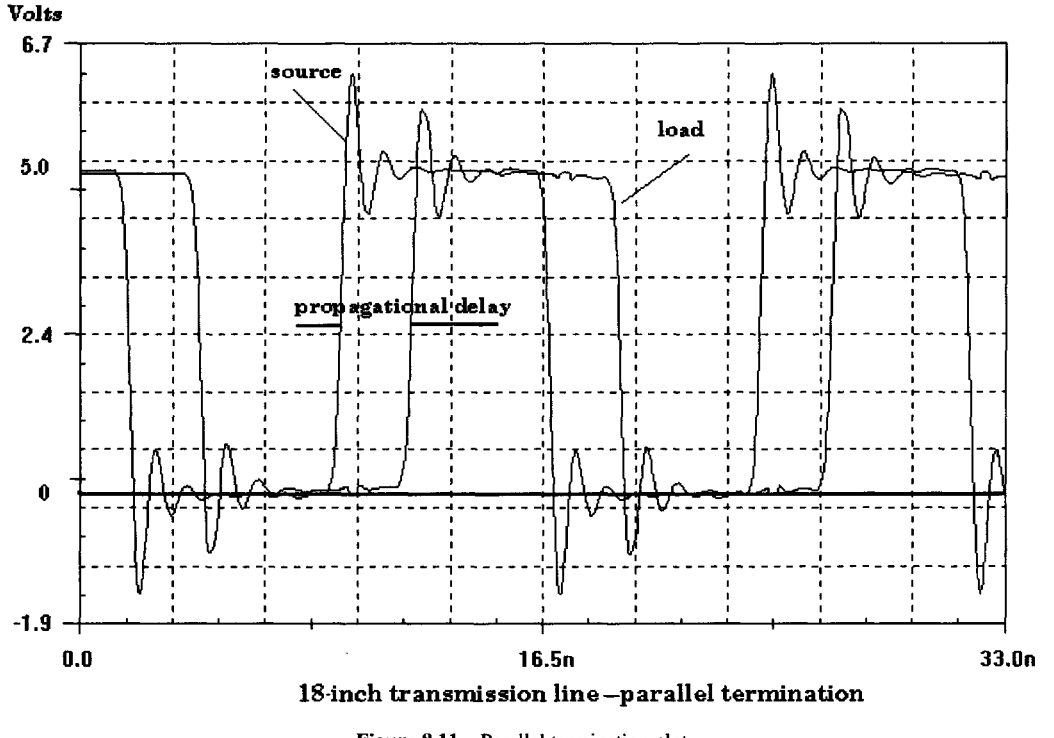


Figure 8.11 Parallel termination plot.

Loading a long trace with additional devices will affect the propagation delay of the source driver's signal, which was discussed in Chapter 7.

Analysis of Parallel Termination

A nearly undistorted waveform will be observed along the full length of the line using parallel termination, similar to that of a coax. If a routed net has multiple receivers and drivers, an increase in propagational delay will be observed owing to additional lumped capacitance provided by all devices connected into the net. If the input shunt capacitance is 5 pF, and six devices are provided on the routed net, a total of 30 pF is presented to the source driver. With the characteristic impedance of the trace and lumped capacitance, the signal will be delayed by the time constant $\tau = 1.1 * Z_o C$. We observe the signal directly at the output of the driver with expected overshoot, and ringing. The signal at the load is acceptable for system performance.

The same discussion regarding propagation delay of a transmission line in the section "baseline" for series termination is applicable. This propagation delay is easily observed in the 18-inch-long trace between source and load. Figure 8.11 shows what parallel termination looks like with both a 3-inch and 18-inch long trace. The results of a properly terminated transmission line will be identical, regardless of termination method chosen. The plot of Fig. 8.11 (18-inch trace) is nearly identical to that of Fig. 8.6 (18-inch trace). The same comments regarding propagational delay of a signal-routed microstrip also applies for parallel termination.

When to Use Parallel Termination

Advantages of Parallel Termination

1. Can be used with distributed loads.
2. Fully absorbs the transmitted wave to eliminate reflections.
3. Sets the line voltage level when nothing is driving the line.
4. Is excellent for busses when distributed loads are available at the end of the trace route.

Disadvantages of Parallel Termination

1. Increased power consumption.
2. Reduced noise margins unless the drivers can source high current circuits.

8.2.5 Thevenin Network

Thevenin termination has one advantage over parallel termination. Thevenin provides a connection that has one resistor to the power rail and the other resistor to ground (Fig. 8.12). Unlike parallel termination, Thevenin permits optimizing the voltage transition points between logic HI and logic LOW. When using Thevenin termination, an important consideration in choosing the resistor values is to avoid improper setting of the voltage reference level of the loads for both the HI and LOW logic transition points. The ratio of $R1/R2$ determines the relative proportions of logic HI and LOW drive current.

Designers commonly, but arbitrarily, use a 220/330 ohm ratio (132 Ohms parallel) for driving bus logic. Determining the resistor ratio value may be difficult to do if the switch point for logic families are different. This is especially true when both TTL and

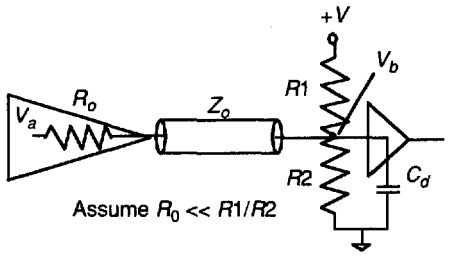


Figure 8.12 Thevenin termination circuit.

CMOS are used. A 1:1 resistor ratio (e.g., 110/110 ohms to create a 55-ohm termination value or characteristic Z_o of the trace) would limit the line voltage at 2.5V, thus allowing an invalid transition level for certain logic devices. Hence, Thevenin termination is optimal for TTL logic, not CMOS.

The Thevenin equivalent resistance must be equal to the characteristic impedance of the trace. Thevenin resistors will provide a voltage division for the signal on the trace. To determine the proper voltage reference desired, one should use Eq. (8.10).

$$V_{\text{ref}} = \frac{R2}{R1 + R2} V \tag{8.10}$$

where V_{ref} = desired voltage level to the input of the load
V = voltage source from the power rail
$R1$ = pull-up resistor
$R2$ = pull-down resistor

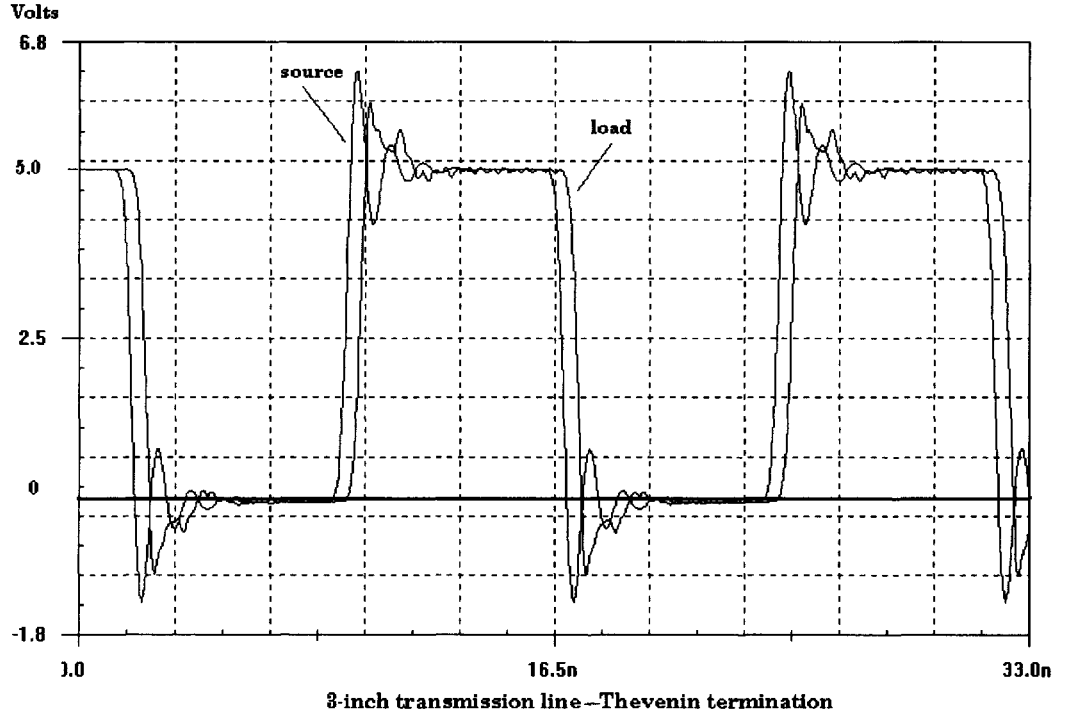
For the Thevenin termination circuit

$R1 = R2$: The drive requirements for both logic HI and LOW are identical. The setting may be unacceptable for certain logic families.
$R2 > R1$: The LOW current requirements are greater than HI. This setting will not work for TTL and CMOS devices.
$R1 > R2$: The HI current requirements are greater than LOW. This is a more appropriate selection for the majority of designs.

With these constraints, $I_{OH\text{max}}$ or $I_{OL\text{max}}$ must never be exceeded. This condition must exist, as TTL and CMOS sinks (positive) current in the LOW state. In the high state, TTL and CMOS sources (negative) current. Positive current refers to current that enters a device, while negative current is the current that leaves the component. ECL logic devices source (negative) current in both logic states.

With a properly chosen termination ratio for the resistors, an optimal DC voltage level will be present for both logic HI and LOW states. The advantage of using parallel termination over Thevenin is parallel's use of one less component. If we compare plots of the effects of parallel compared to Thevenin, we notice that both termination methods provide identical results. A terminated trace will always appear identical regardless of termination method chosen.

Thevenin termination is rarely used because of a large drive current required in the HI state. The results in Fig. 8.13 show a nearly perfect waveform, along with the expected delay of the signal at the load. Figure 8.13 shows the signal directly at the output of the



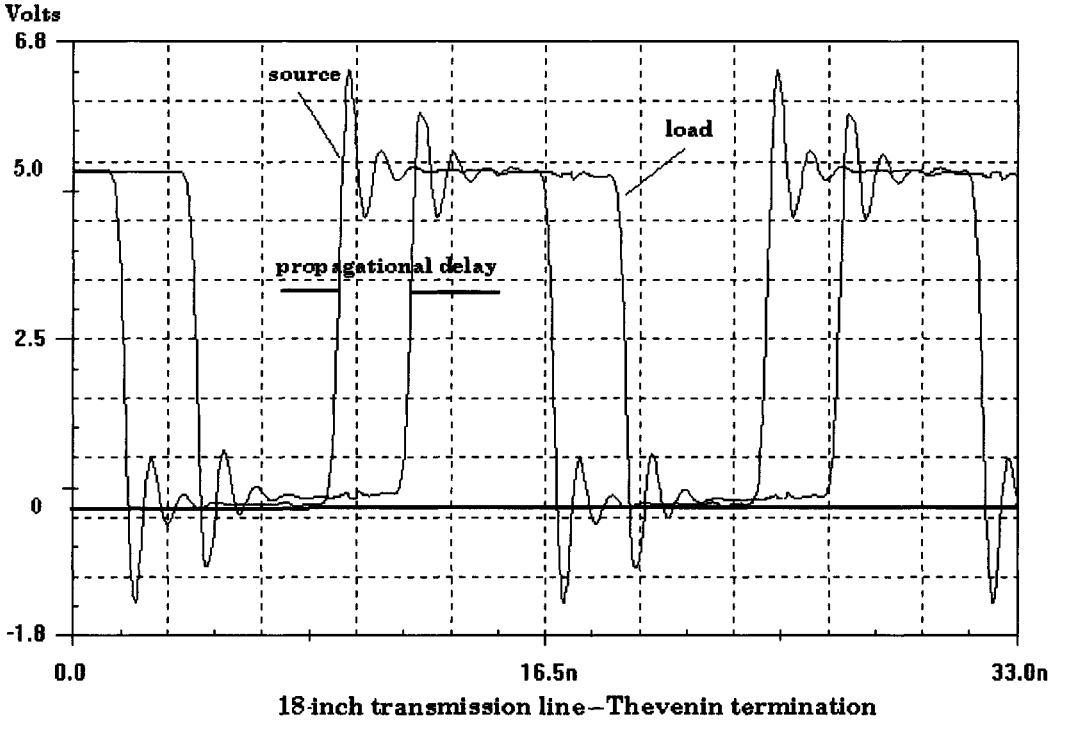


Figure 8.13 Thevenin termination plot.

driver with expected overshoot, and ringing, in addition to what the signal would look like at the load for both a 3-inch (electrically short) and 18-inch trace (electrically long).

Analysis of Thevenin Termination [2]

A nearly undistorted waveform will be observed along the full length of the line using Thevenin termination, similar to that of parallel termination. An increase in delay will also be observed on busses with multiple receivers and drivers on the net due to the additional lumped capacitance provided by all devices tied into the routed net. As with parallel termination, the characteristic impedance of the trace, along with the lumped capacitance, will cause the signal to be delayed by the time constant $\tau = 1.1 * Z_o C$. This delay is easily observed in the trace identified as load in Fig. 8.13. We also see what the signal profile looks like directly at the output of the driver along with typical ringing which always occurs. The signal at the load is acceptable for system performance.

Close examination of parallel termination, Fig. 8.11, and Thevenin, Fig. 8.13, indicates identical plots. This is what termination will do to a signal trace. To observe the difference, compare the waveform at the load to the unterminated trace in Figs. 8.4.

The results of a properly terminated transmission line will be identical, regardless of termination method chosen. The plot of Fig. 8.13 (18-inch trace) is nearly identical to those of Fig. 8.6 and 8.11 (18-inch trace). The same comments regarding propagational delay of a signal routed microstrip also apply for parallel termination.

When to Use Thevenin Termination

Advantages of Thevenin Termination

1. Can be used with distributed loads throughout a routed net.
2. Fully absorbs the transmitted wave to eliminate reflections.
3. Sets the line voltage level when nothing is driving the line.
4. Is excellent for busses.

Disadvantages of Thevenin Termination

1. Increases power consumption.
2. Reduces noise margins unless the drivers can source high current circuits.

When the driver is sourcing HI, say 5.0V, and the pull-down resistor is 330 Ω, the resistor must absorb 5.0/330 Ω = 15 mA of current. If the driver cannot source this much current, the HI value of the voltage, V_{OH}, will go down and the noise margin ($V_{IH} - V_{OH}$) will also go down. On busses terminated at both ends with 220/330 Ω resistors, the driver has to source double the current, 30 mA.

EXAMPLE: BACKPLANE IMPLEMENTATION

On a typical TTL-based backplane with traces on the outer layers (microstrip) (Fig. 8.14), the bus lines are terminated at both ends with a 220-Ω resistor to power and a 330-Ω resistor to ground. Both ends must be terminated since the source driver may be located anywhere on the bus. This 220/330 Ω combination provides 132-Ω termination, which is a typical value for PCB traces routed on a backplane assembly. With this termination methodology, the use of high-current bus drivers is required.

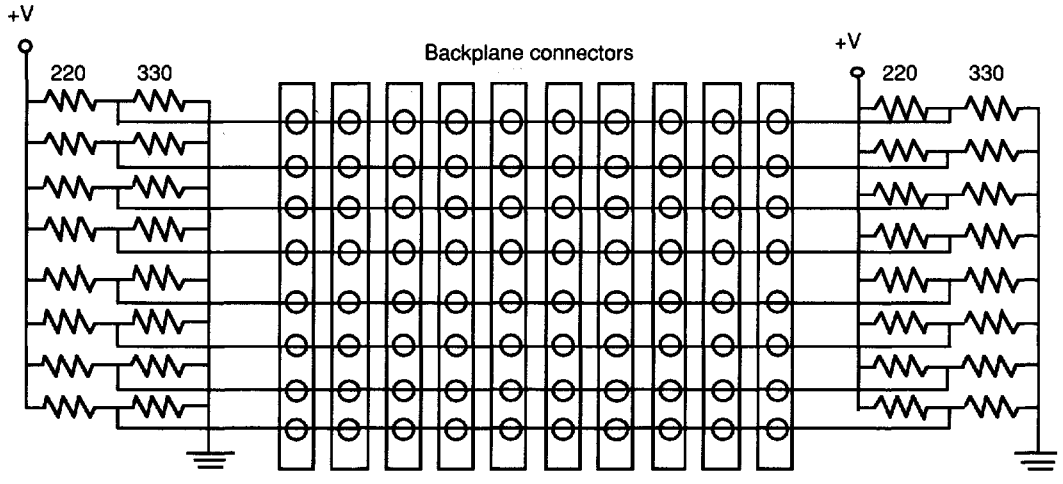


Figure 8.14 Backplane termination implementation.

8.2.6 RC Network

The RC (also known as AC) termination method works well in both TTL and CMOS systems. The resistor matches the characteristic impedance of the trace (identical to parallel). The capacitor holds the DC voltage level of the signal since the source driver does not have to provide current to drive an end terminator. As a result, AC current (RF energy) flows to ground during a switching state since a capacitor will allow RF energy (which is an AC wave, not the DC logic level of the signal) to pass through. Although a minor propagation delay is presented to the signal due to the RC time constant, less power dissipation exists than in parallel or Thevenin termination. From the viewpoint of the circuit, all three end termination methods are identical. The main difference lies in power dissipation, with RC consuming far less power than the other two.

The termination resistor must equal the Z_o of the trace, while the capacitor is generally very small (20–600 pF). The RC time constant must be greater than twice the loaded propagation delay (round trip travel time). This time constant is greater than twice the loaded propagation delay because a signal travels from source to load and returns. It takes one time constant each way for a total of two time constants. If we make the time constant slightly greater than the total propagation delay (x2), reflections will be minimized or eliminated. RC termination finds excellent use in buses containing similar layouts.

To determine the proper value of the resistor and capacitor, Eq. (8.11) provides this simple calculation which includes the round-trip propagation delay $2 * t'_{pd}$.

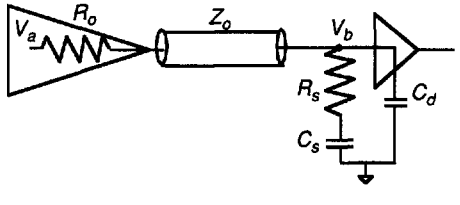


Figure 8.15 RC network circuit.

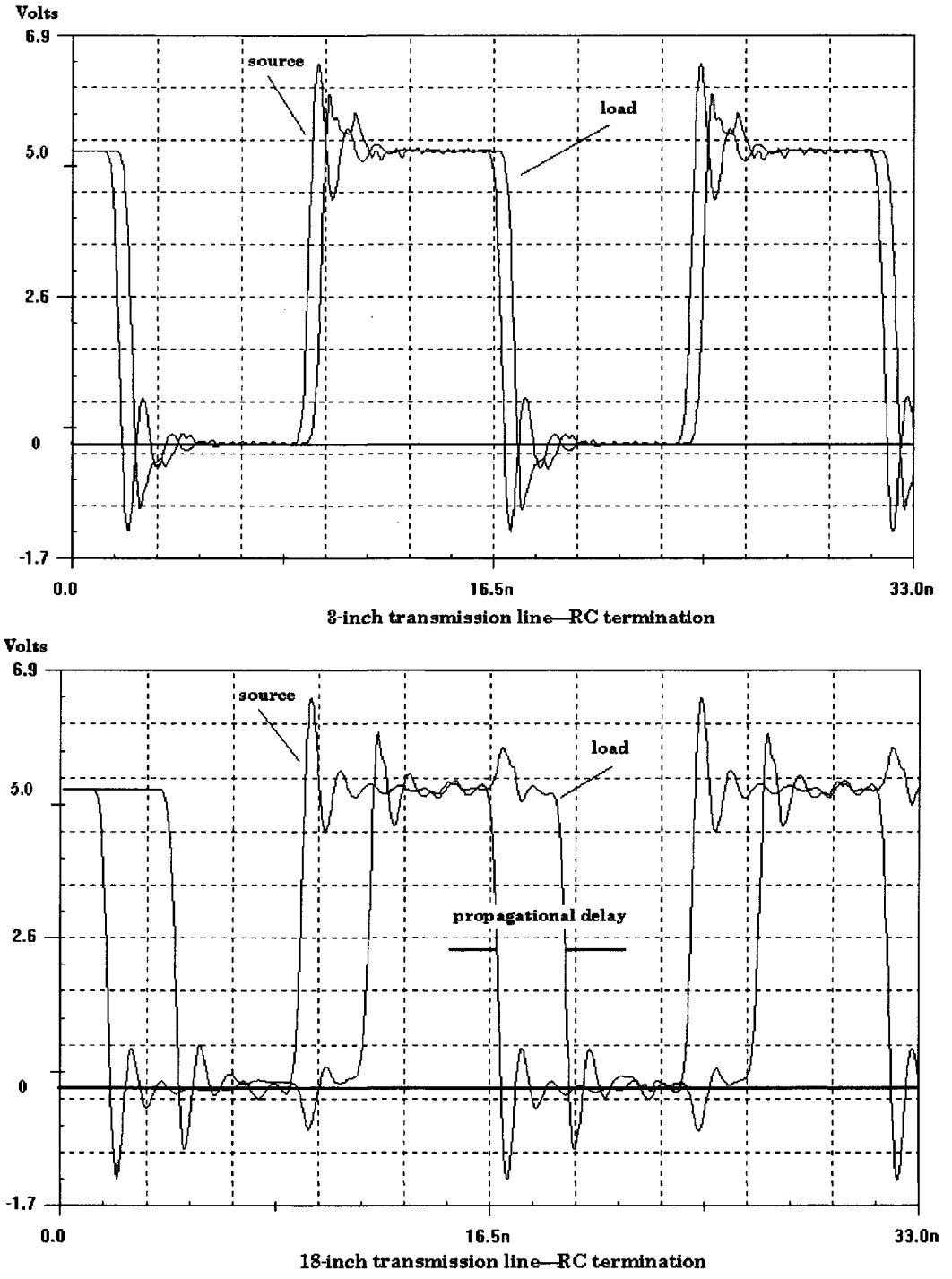


Figure 8.16 RC termination plot.

$$\tau = R_s C_s \quad \text{where } \tau > 2 * t'_{pd} \quad \text{for optimal performance} \tag{8.11}$$

Figure 8.16 shows the results of RC termination. The lumped capacitance (C_d plus C_s) affects the edge rate of the signal, causing a slower signal to be observed by the load.

If the round-trip propagation delay is 4 ns, RC must be > 8 ns. Calculate C_s using the known round-trip propagation delay. Propagation delay is discussed in Chapter 6 using the value of ε_r that is appropriate for the dielectric material provided and for the actual speed of propagation required.

Note: The self-resonant characteristic of the capacitor is critical during evaluation to avoid inserting equivalent series inductance (ESL) into the circuit.

Analysis of RC Network

Again, like parallel and Thevenin, a nearly undistorted waveform will be observed along the full length of the line. Optimal termination will provide a clean signal at the load regardless of which termination method is used.

The capacitor appears to the trace as an AC short to the RF component of the high-speed signal. The reflected wave is fully absorbed with no reflection since the resistor matches the trace impedance. The capacitor blocks the DC current so that no power consumption is traveling through the resistor to ground. The capacitor also prevents the DC noise margins from eroding, since there is no IR drop across the resistor. In addition, the RC network acts as a low-pass filter to remove glitches that may occur on the signal trace.

When to Use the RC Network

Advantages of RC Termination

1. Can be used with distributed loads and bus layouts.
2. Fully absorbs the transmitted wave to eliminate reflections.
3. Has low DC power consumption.

Disadvantages of RC Termination

1. May slow down very high-speed signals.
2. Can produce reflections due to the time constant of the RC network. This is definitely a concern for high-frequency, fast edge rate signals.

When differential paired signals exist, RC termination finds popular use. This termination method is shown in Fig. 8.17. Any termination method that is appropriate for this circuit may be used—RC, parallel, Thevenin, or series. For the example shown, the RC network requires only three components. The capacitor prevents power consumption in addition to maintaining the proper voltage reference to the signals of interest. The components should be close in tolerance to avoid mismatches and to assure equal values for each signal of the pair!

8.2.7 Diode Network

This termination method is commonly used for termination of differential or paired networks. A schematic representation is found in Fig. 8.20. Diodes are often used to limit overshoot on traces while providing low-power dissipation. The major disadvantage of

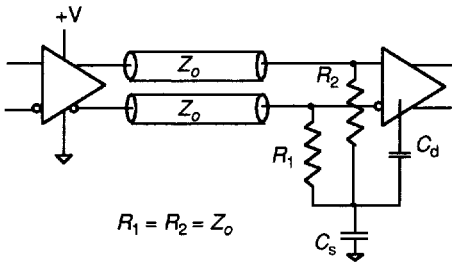


Figure 8.17 RC network of differential paired traces.

diode networks lies in their frequency response to high-speed signals. Although overshoots are prevented at the receiver's input, reflections will still exist in the trace as diodes do not affect trace impedance or absorb reflections. To gain the benefits of both techniques, diodes may be used in conjunction with the other methods discussed herein to minimize reflection problems. The main disadvantage lies in large current reflections that occurs with this termination network. One should be aware, however, that when a diode clamps a large impulse current, this current can be propagated in the ground plane, thus increasing EMI!

A summary of the various termination methods is provided at the end of this chapter, comparing advantages and disadvantages.

8.3 TERMINATOR NOISE AND CROSSTALK

Multiple terminators may be provided within a single package instead of being used as discrete components. These packages may be Single-In-Line Package (SIPs), Dual-In-Line Package (DIPs), or other configurations with a shared power and/or ground pin. This shared pin may contain undesired lead-length inductance, which may affect signal functionality when a logic transition occurs from high-to-low or low-to-high, in addition to allowing creation of RF currents to exist.

With an inductive effect present, described by $L = dI/dt$, a current surge will be observed by all terminators simultaneously due to this fixed inductance value. This current surge may cause a signal bounce to develop, similar to ground bounce on the power/ground planes. If the bounce is severe enough, functionality concerns exist. To minimize the bounce effect of multiple terminators within the same package, one should use only those package designs with separate power and ground pins and internal decoupling, if possible.

The difference in a typical termination package configuration is shown in Fig. 8.18. When a common ground pin is provided, a common current path will occur depending on the internal manufacturing process used. A common current path introduces a large amount of mutual inductance between the resistors in the package. This common current path will allow crosstalk to be generated internal to the terminator.

Designers should design and lay out a PCB to minimize creation of crosstalk between signal traces and to prevent mutual coupling of RF currents. With crosstalk concerns taking a major role in the layout of traces, one tends to forget that terminators may cause crosstalk.

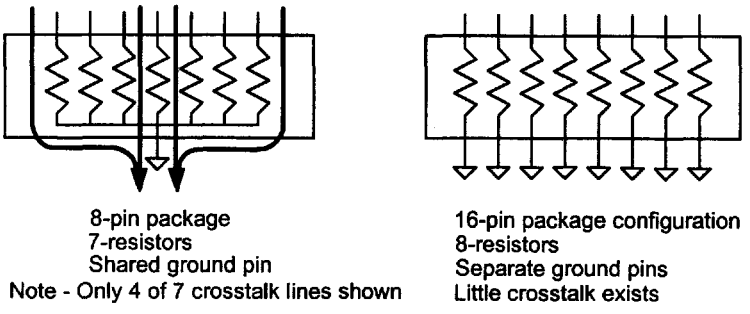


Figure 8.18 Shared pins within a terminator package.

Signal integrity and crosstalk are discussed in Chapter 7. Crosstalk occurs owing to the combination of capacitive and inductive coupling between traces, traces-to-planes, and traces to components. Capacitive and inductive coupling is additive to the overall amount of crosstalk that will exist.

To minimize crosstalk between traces, use of the *3-W* rule is required (discussed at the end of Chapter 7). How is implementation of the *3-W* rule with terminators accomplished? Figure 8.19 illustrates this common design oversight and how to fix it.

Terminators can cross-couple RF energy between circuit traces. This cross-coupling could be much worse than natural crosstalk present between two adjacent transmission lines. Crosstalk in terminations comes from both mutual inductive and capacitive coupling. Inductive coupling usually dominates. The total amount of coupling is the sum of both parts.

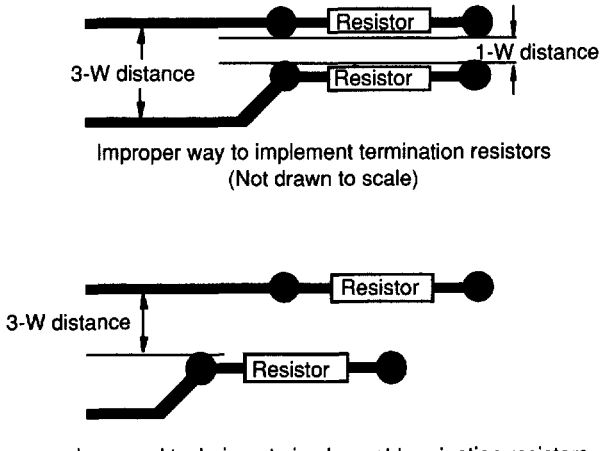


Figure 8.19 Crosstalk between termination resistors.

8.4 EFFECTS OF MULTIPLE TERMINATIONS

Multiple or dual terminations on a PCB trace can present functionality concerns. This is due to the additive effects that a dual termination presents to the circuit. During layout it is sometimes desirable to place component pads onto the PCB; this provides the ability to choose a termination method based on measurements from a prototype build. Although the layout can allow for choosing an optimal termination method, problems can and will occur if careful attention is not taken during installation of the components, or if rework is performed by a person who will install components on pads regardless of whether they are specified in the Bill of Materials. When multiple mounting locations are provided, the designer can use either series, parallel, Thevenin, or RC. An example of how a design engineer may specify optional termination methods for experimentation purposes is presented in Fig. 8.20.

Real-Life Situation—Using Dual Terminations (what can happen). Why would someone dual terminate a trace if poor performance were expected? Let's assume a product is being tested on a remote open field test site with only one attempt to make the product pass radiated emissions requirements. Mounting pads are provided for all possible termination methods. In the rework kit are 0 Ω resistors and a selection of various other resistors and capacitors. These components are used to rework the board (in the field), such as removing series termination or to convert an RC to parallel in order to better match trace impedance and enhance signal functionality. All these components are used in an attempt to make the product work as desired.

For example, component placement pads for a series terminator are provided on the top side of the PCB. During compliance testing, radiated emission is observed. The 0 Ω series resistor is replaced with 33 Ω. Also provided is end termination, which is located on the bottom side of the board unavailable for inspection and unknown to the test engineer. The test engineer may not know what kind of termination is provided, if any, or how terminations even work. The series resistor, 33 Ω, now allows for radiated emissions compliance. This rework is incorporated into the product and shipped without further investigation by signal integrity engineers since product revenue generally takes priority over functionality, especially if a project is behind a scheduled shipment date.

Many engineers will use only a spectrum analyzer when investigating an EMC event. If a sufficiently *high bandwidth oscilloscope* is used in conjunction with a spectrum

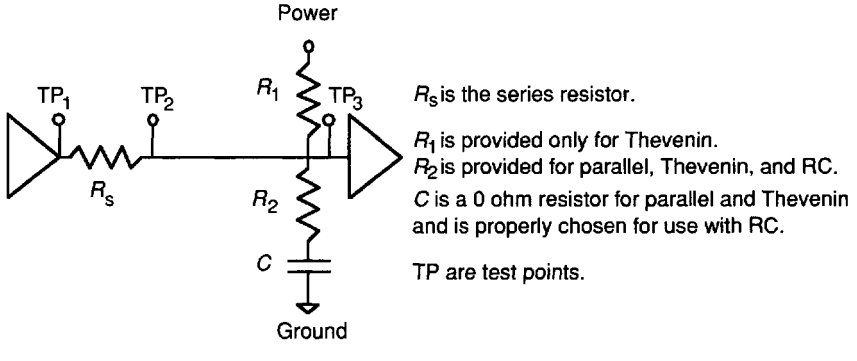
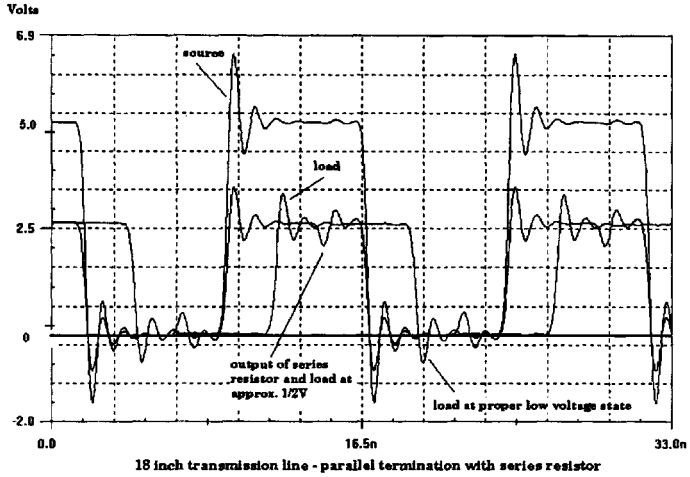
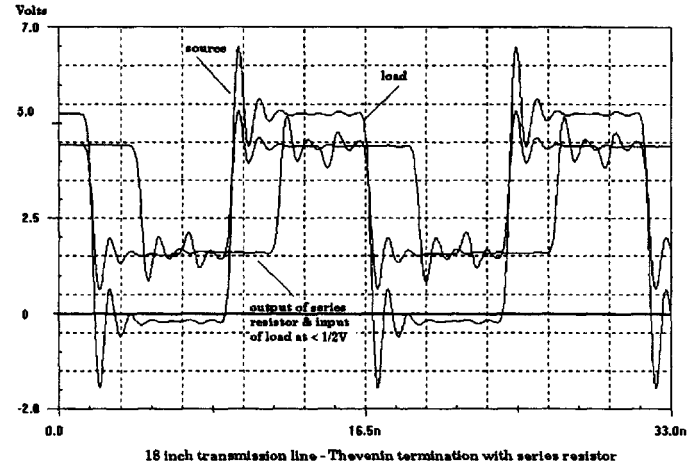


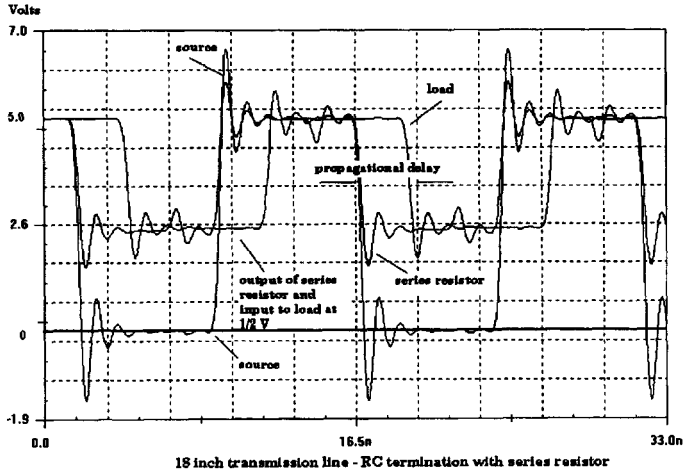
Figure 8.20 Providing for optional termination selection during PCB layout.



18 inch transmission line - parallel termination with series resistor



18 inch transmission line - Thevenin termination with series resistor



18 inch transmission line - RC termination with series resistor

Figure 8.21 Effects of dual terminations.

analyzer, signal integrity problems may be easily observed, with related concerns addressed. Most engineers will use either a spectrum analyzer or an oscilloscope, depending on their comfort level. Few engineers will consider both the time *and* frequency domain aspects of components, a network or circuit. When management demands that a product, which was to ship last week is behind schedule, additional engineering resources to investigate the effects of a termination change become unacceptable, for corporate revenue sometimes takes a higher priority than proper engineering analysis.

To illustrate actual results that can occur with dual terminations, an example is provided with multiple components daisychained on an 18-inch (45.7-cm) trace, 0.8-ns edge rate, with components dispersed through the trace route. Figure 8.20 illustrates a schematic drawing of this circuit. In Fig. 8.21, we observe the effects of dual terminations on the PCB using SPICE simulation. The trace is electrically long and requires termination per the definition provided in Chapter 6 for an electrically long trace.

For parallel and Thevenin, one will observe a 1/2V level, logic level state dependent. This 1/2V level is caused by the series resistor. The ringing that occurs at the load is minimal and is a nearly perfect signal at the load. However, an interesting situation is noted. For parallel termination with a series resistor, the voltage level observed at the load in the low-to-high transition state is at 1/2V. It becomes obvious that the circuit cannot work as designed, especially if mixed logic is provided on the net. The same results occur with Thevenin except in the high-to-low transition state.

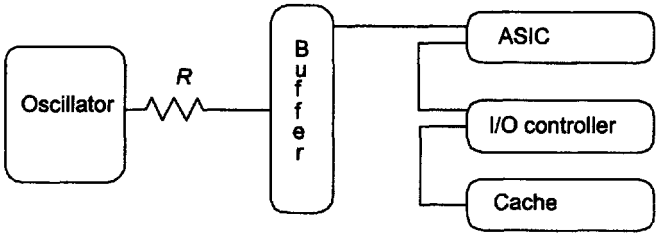
For RC networks, a more dramatic effect is observed. As a result of the terminator, the series resistor appears at the 1/2V level as expected. At this point, the output of the resistor looks identical with smooth rounding of the signal. This rounding occurs from $\tau = RC$ where τ is the rounding time constant, R is the termination resistance, and C is the total shunt capacitance of the network. The load receives a clean signal in the HI logic state but at the expense of a much slower edge rate. If the timing requirements of the load are not critical, rounding of the signal will enhance EMI performance significantly without affecting signal integrity. Since the capacitor holds the DC voltage level of the signal on the trace, the voltage degradation that was present when both parallel and Thevenin termination are dual terminated with a series resistor will not be seen.

As observed, providing dual termination can, and will, cause functionality concerns to exist. Dual termination must never be used in any design without a thorough understanding of what will happen to signal integrity along with creation of EMI.

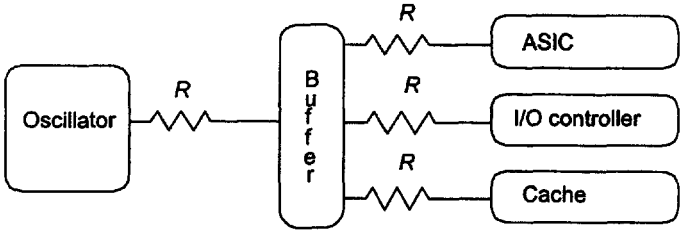
8.5 TRACE ROUTING

Engineers and designers will sometimes daisychain periodic signal and clock traces for ease of routing. Unless the distance is small between loads (with respect to propagation length of the signal rise time), reflections may occur from daisychained traces. Sometimes daisychaining impacts signal quality and EMI spectral energy distribution to the point of nonfunctionality or noncompliance. Therefore, radial connections for fast edge signals and clocks are preferred over daisychaining for nets with a single, common drive source. Each component should have its respective trace terminated in its characteristic impedance as shown in Fig. 8.22. Parallel and Thevenin termination at the end of the trace route is rarely feasible because the drivers usually cannot tolerate the total current sink of the terminated loads.

To prevent undesired effects of unmatched loads, termination may be required. Five common termination methods are available (discussed earlier in this chapter). Each



Poor trace routing for clock signals (Note daisychaining of clock signal)



Optimal trace routing for clock signals with series termination

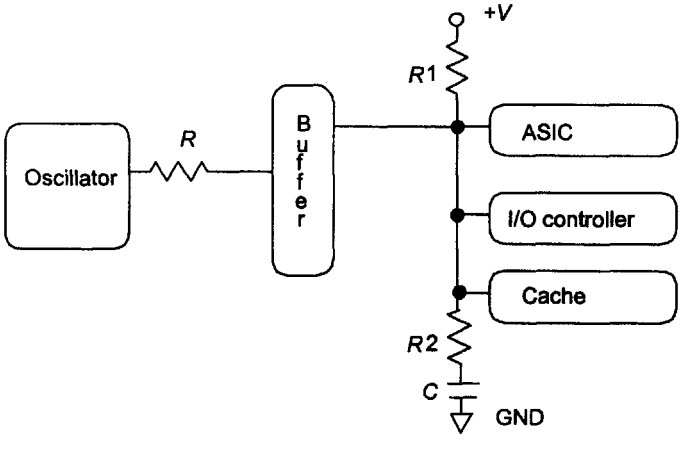


Figure 8.22 Termination of clock traces.

method is dependent on the complexities of layout geometry, component count, and power consumption. When a driver is overloaded, termination can degrade the trace if incorrectly specified or implemented.

If an electrically long signal trace route exists, this trace *must be correctly terminated!* Long lines generally require use of high-current driving components. One should calculate the terminating resistor value at the Thevenin equivalent or the characteristic impedance of the trace. Use of "T-stubs" or bifurcated lines is generally not allowed. If a

T-stub has to be used, the maximum permissible stub length cannot exceed $T = L_d^{tr/10}$, where L_d is the routed length of the trace. The length of each "T" from the center leg must be identical. In T-stub lines, the capacitance and load characteristics of the devices at the end of each T-arm should be exactly equal.

If a T-stub is required because of problems with layout or routing, it must be as short as possible. The measurement feature of the CAD system should be used to measure routing lengths. If necessary, one should serpentine route the shorter trace until it equals its counter trace length exactly.

A potential or fatal drawback of using T-stubs lies in future changes to the artwork. If a different design engineer or PCB designer makes a change to the layout or routing to implement rework or a redesign, knowledge of this T-stub implementation may not be known, and accidental changes to the trace may occur, posing potential EMI or functionality problems.

8.6 BIFURCATED LINES

Bifurcated lines is another term for T-stubs. This condition occurs when a trace is split into multiple trace routes from a driver. An example of a bifurcated topology is shown in Fig. 8.23, along with a recommended termination method.

The impedance of a bifurcated line is not constant throughout the trace route. Let us assume, for example, that the trace from point A to X is 50 ohms. The impedance of the bifurcated lines must be $2Z_o$ from point X to point B, or twice that of the desired impedance characteristics. This is because, for this example, the two traces are running in parallel, each with an impedance of 100 ohms. The parallel impedance of the two traces will be 50 ohms, the desired impedance of the network. Since the individual bifurcated traces are now 100 ohms, use of end termination of 100 ohms each is the only practicable termination methodology. To use parallel termination, the driver must be able to source sufficient current to multiple loads on the net.

If proper termination is provided, reflection and ringing that may occur will be prevented. If termination is not provided, the return current will see an impedance discontinuity at point X. This discontinuity will be observed as ringing at the source driver, point A. The termination must be provided at the end of the trace route as was shown in Fig. 8.8.

If bifurcated routing must occur, how can an optimal design be set up within a PCB when split traces must be $2Z_o$? The easy layout technique available to the PCB designer is to make the trace width smaller than the primary trace from point A to X. This becomes almost impossible for most applications, for the line widths of traces are already approaching a very small dimension. To increase trace impedance, it is necessary to make the traces even smaller, which in many situations is smaller than the manufacturing process a PCB fabricator is capable of performing.

Another problem with bifurcated lines lies with RF loop currents created within the network. If one of the bifurcated signal traces is routed on a different routing plane than the other bifurcated trace, RF return current will try to reference both traces to different 0V return planes. When this occurs, a potentially large loop area is created, with a corresponding increase in radiated emissions.

To summarize, use of bifurcated lines, or T-stubs is not desirable for both signal integrity and EMI compliance reasons.

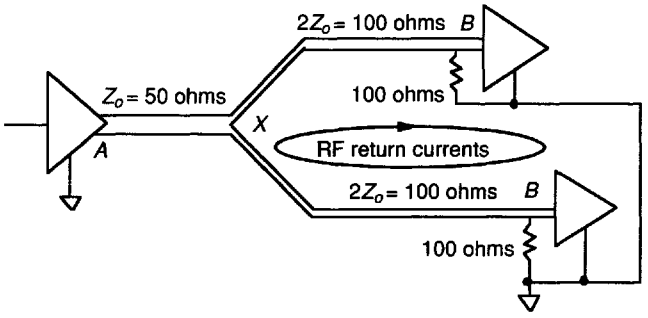


Figure 8.23 Example of bifurcated lines.

8.7 SUMMARY—TERMINATION METHODS

Different termination methods are available, each for a specific application along with advantages and disadvantages. The termination method that provides optimal performance for most designs (CMOS or TTL) is dependent on what the circuit designer requires. The following is a brief summary of termination methods presented earlier in this chapter.

1. Series is excellent for point-to-point trace routes (one load on the net). In addition, series termination works well for those traces that are electrically short (small propagation time from source-to-load and return from load-to-source) with respect to the clock frequency (t_{pd}). Series termination may also be used to slow down edge times so that the effect of propagation discontinuities in the signal path is minimized. In addition, it becomes a simple process to allow for the fanout of multiple load radials from a common source to occur using separate transmission lines that do not corrupt other circuits in the network.
2. Parallel is preferred for busses and point-to-point nets with fast clock/pulses (frequencies).
3. Thevenin networks are difficult to implement owing to the reduced voltage level that exists in both the HI and LOW state if a combination of both CMOS and TTL exists on the same net.
4. The RC network provides good signal quality but at the expense of added components. Drawbacks exist at high frequencies and for long trace lengths owing to limited damping that occurs with poor impedance matching and edge rate degradation.
5. Dual terminations degrade signal functionality and should not be used without fully understanding the consequences.

What happens when a trace on a PCB cannot be terminated?

1. There may be 100% positive signal reflection, resulting in signal doubling in amplitude at the source driver. This may cause destruction of the component owing to excessive voltage levels.
2. The signal may become 70–80% negative at the source driver, which will erode signal functional and noise margin levels of the circuit.

3. Loads located at a distance from the driver may be triggered by false signal transitions, resulting from ringing that will occur at trigger threshold levels.
4. Load-sensitive components should be located at the end of a routed net to minimize reflections between these sensitive components and to prevent false edge triggering.
5. Edge-sensitive signals should be prevented. Voltage-level sensitive components should be used with a sufficiently long setup time to guarantee proper triggering.

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