*EMC and the Printed Circuit Board: Design, Theory, and Layout Made Simple.* Mark I. Montrose
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# 3

# Components and EMC

It is a well-known fact that RF energy spectra is created as a result of switching current within a PCB. These currents are created as a byproduct of digital components. Each logic state transition produces a transient surge within the power distribution system. Most of the time, these logic transitions do not produce enough ground-noise voltage to be of any functional concern. It is when the edge rate (rise and fall time) of a component becomes extremely fast that RF energy is produced.

Transient spikes placed on a power distribution system creates ground-noise voltage. This ground-noise voltage is first observed as differential-mode (DM) noise. Differential-mode noise is then converted to common-mode (CM) currents. Common-mode currents are the main cause of radiated RF energy. By minimizing production of DM noise in the power distribution network, less CM current results.

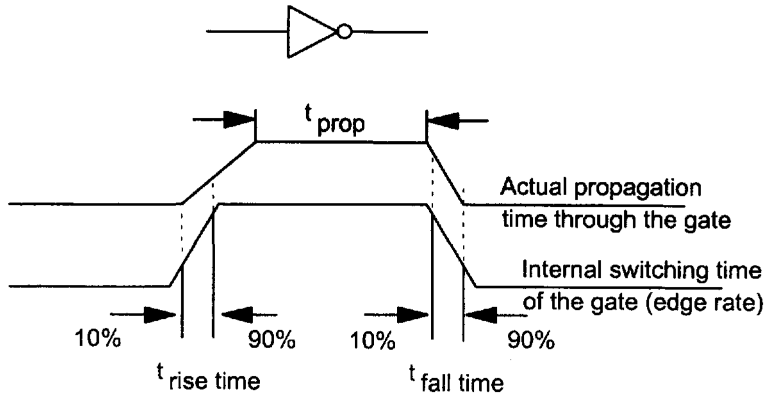
This chapter investigates active components (digital logic) along with their relationship to the creation of DM noise. Passive components were discussed in Chapter 2. In addition to the parameters and behaviors that are present within digital logic related to emissions, susceptibility and self-compatibility concerns exist.

## 3.1 EDGE RATE

When choosing digital components for a particular application, design engineers are generally interested only in functionality and operating speed, basing their selection on the propagation delay of the internal logic gates as published by the manufacturer, not necessarily the actual edge rate of input and output signals.

As the speed of components accelerates (faster internal propagation time), increases in DM currents, crosstalk, and ringing potentially can occur. There is an inverse relationship between operating speed and EMI. Many components have internal logic gates that operate at a faster edge rate than the propagation delay required for functionality. As a re-

sult, slower logic families (internal gates) are preferred for EMI since propagation delay is the primary function of the circuit. Figure 3.1 illustrates the relationship between the internal switching speed of a basic inverter gate compared to propagation delay.




t prop is the propagation delay of the device.

*Note:* Manufacturer may claim a rise/fall time at 2 ns max. In reality, this value may be well into sub-nanosecond values.

**Figure 3.1** Output switching time versus propagation delay.

Speed is important only when the edge rate of a signal (rise or fall time) is fast enough that the desired signal changes logic state in the same or less time than it takes to allow the signal to travel the length of the trace or wire. The actual clock frequency is a secondary concern for EMC compliance, whereas the actual edge rate is the primary concern.

Various logic families are available with different design features. These features vary between CMOS, TTL, and ECL and include input power, package outline, speed-power combinations, voltage swing levels, and edge rates. Certain logic devices are now available with clock skew circuitry to slow down the internal edges of the internal logic gates while maintaining accurate propagation delay.

One extremely important device parameter (for EMC) usually not specified by device manufacturers is *power peak inrush surge current into the power pins*. These peak power currents are the result of logic crossover currents, device capacitive overheads, and capacitance caused by surge currents from trace capacitance and loading device junctions. These surge currents may exhibit levels that are many multiples of the actual signal currents that are injected into a transmission line (trace).

Selection of the slowest logic family possible while maintaining adequate timing margins minimizes EMI effects and enhances signal quality. We should note here that use of standard and low-power Schottky TTL logic, (e.g., 74LS series) is becoming less common in today's marketplace. Moreover, specialized design techniques during layout are usually not required when using slower speed logic families. However, today's high-speed, high-technology products require use of extremely fast-edge logic in the 1.5–5 ns range, for example, 74ACT and 74F series. Use of a 74HCT could be provisionally adequate for replacement of a 74ACT for most applications, with the added benefit of less RF emissions generated. As a general consideration, *do not use faster devices than the functional timing diagram or what the circuit actually demands.*

If timing requires fast logic families, the designer must address individually the issues of decoupling, routing, and handling of clock traces. (See Table 3.1 for details on the EMI characteristics of different logic families.)

Fast switching times (edges) cause proportional increases in problems related to return currents, crosstalk, ringing, and reflections, and only increased attention to meticulous design can alleviate these problems. These problems are independent of device propagation delay. This is because logic families have edge rates that are faster than the propagation delay inherent in the device. No two logic families are the same. Even the same components from different manufacturers may differ in construction and edge rates. Edge rate is defined as the rate of voltage or current change per unit time (volt/ns or amperes/ns).

When selecting a logic family, manufacturers will specify in their data book the *maximum* or *typical* edge rate $t_{max}$ or $t_{typ}$ of the clocks and I/O pins. This specification is usually 2–5 ns maximum. It is observed that the *minimum* edge rate $t_{min}$ may not be published. A device with a 2 ns maximum edge rate specification may in reality be 0.5 to 1.0 ns. The significant contributor to the creation of RF energy is the edge rate, *not* actual operating frequency. A 5 MHz oscillator driving a 74F04 driver (with a 1-ns edge) will generate larger amounts of RF spectral energy over the frequency spectrum than a 100-MHz oscillator driving a 74ALS04 (with a 4-ns edge). ***This one component specification is the most frequently overlooked and forgotten parameter in printed circuit board design. However, this is the most critical aspect of which design engineers must be con-***

**TABLE 3.1** Chart of Logic Families

| Logic Family | Published Rise/Fall Time (Approx. $T_r/T_f$ | Principal Harmonic Content/ $F = (1/\pi t_r)$ | Typical Frequencies Observed as EMI ($10^{th}$ harmonic) $F_{max} = 10*F$ |
|---|---|---|---|
| 74L xxx | 31–35 ns | 10 MHz | 100 MHz |
| 74C xxx | 25–60 ns | 13 MHz | 130 MHz |
| 74HC xxx | 13–15 ns | 24 MHz | 240 MHz |
| 74 xxx | 10–12 ns | 32 MHz | 320 MHz |
| (flip-flop) | 15–22 ns | 21 Mhz | 210 MHz |
| 74LS xxx | 9.5 ns | 34 MHz | 340 MHz |
| (flip-flop) | 13–15 ns | 24 MHz | 240 MHz |
| 74H xxx | 4–6 ns | 80 MHz | 800 MHz |
| 74S xxx | 3–4 ns | 106 MHz | 1.1 GHz |
| 74HCT xxx | 5–15 ns | 64 MHz | 640 MHz |
| 74ALS xxx | 2–10 ns | 160 MHz | 1.6 GHz |
| 74ACT xxx | 2–5 ns | 160 MHz | 1.6 GHz |
| 74F xxx | 1.5–1.6 ns | 212 MHz | 2.1 GHz |
| ECL 10K | 1.5 ns | 212 MHz | 2.1 GHz |
| ECL 100K | 0.75 ns | 424 MHz | 4.2 GHz |
| BTL | 1.0* | 318 MHz | 3.2 GHz |
| LVDS | 0.3* | 1.1 GHz | 11 GHz |
| GaAs | 0.3* | 1.1 GHz | 11 GHz |
| GTL + (Pentium Pro) | 0.3* | 1.1 GHz | 11 GHz |

*These are minimum edge rate values.

TABLE 3.2 Selected Characteristics of Logic Families

| Logic Family | Voltage Swing (V) | Input Capacitance (pF) | DC Noises Margin (V) | Typical Output Resistance $R_o$ Low/High) Ω |
|---|---|---|---|---|
| CMOS, 5V | 5 | 5 | 1.2 | 300/300 |
| CMOS, 12V | 12 | 5 | 3 | 300/300 |
| TTL | 3.3 | 5 | 0.4 | 30/150 |
| TTL-LS | 3.3 | 5.5 | 0.4 | 30/160 |
| HCMOS | 5 | 4 | 0.7 | 160/160 |
| S-TTL | 3.3 | 4 | 0.3 | 15/50 |
| FAST & AS-TTL | 3.3 | 4.5 | 0.3 | 15/40 |
| ECL, 10k | 0.8 | 3 | 0.1 | 7/7 |
| GaAs | 1 | ≈ 1 | 0.1 | — |

***cerned with to ensure an EMI-compliant product.*** The frequently heard statement, "Use the slowest logic family possible," is a result of the minimum edge rate parameter ***not being specified or published*** by a component manufacturer in their data books. Edge rates of digital devices are the source of most RF energy created within a PCB.

The reason to use the slowest logic family stems from the relationship between time domain and frequency domain. Fourier analysis of signal edges in the time domain shows that as the slope (edge rate) of the signal becomes faster, a greater amount of spectral bandwidth of RF energy is created. A detailed discussion of Fourier transforms and analysis is presented in Appendix B.

Table 3.1 provides information on the harmonic spectrum of digital logic families. This chart can be used as a reference in determining an optimal logic family to use for minimizing EMI emissions while allowing for proper functionality of the design. In examining Table 3.1, the spectral distribution (bandwidth) is shown as $1/\pi t_r$, with $t_r$ being the edge rate. For bipolar technologies, the rise and fall times are generally different, with $t_f$ the faster of the two. The equivalent bandwidth presented in Table 3.1 is calculated on the shorter (or faster) edge rate, either $t_r$ or $t_f$ (fall time or high-low transition). Rise and fall time is commonly referred to as the "edge rate" and is dependent on the device loading (output) pin. Table 3.1 considers capacitive loading at approximately 20–40 pF to represent reasonably fast conditions and typical board layout.

Table 3.2 shows selected characteristics of several logic families. Here it is observed that the output resistance, $R_o$, of the logic gate is the current limiting parameter. This defines how much drive current is possible under a heavy capacitive load, or the equivalence of a shorted trace at a specific resonant frequency. Even a shorted gate output (time of transition) cannot deliver a current greater than $V/R_o$.

## 3.2 INPUT POWER CONSUMPTION

Power supply transition currents to a gate's input is a major contributor to noise generation on the board by either the power plane (or trace) or ground plane/ground trace (0V reference). The 0V reference refers to the source that is at ground potential relative to the

power source. It is common to refer to 0V reference as being either the power return plane, image plane, or ground plane. Transition currents are the main source of differential-mode currents and, hence, RF energy.

1. Examining Table 3.1, we notice that the shorter the transition time, or the faster edge rate, a larger EMI spectral profile exists. EMI increases in severity with frequency, $f$ (for conducted EMI and crosstalk) and often $f^2$ (for radiated EMI).
2. The power supply transition current demands during component switching can be quite large. These currents have no relationship with the quiescent current required to establish a "1" or "0" signal state in digital logic. For TTL and some CMOS technologies, inrush of surge current is created owing to partial conduction overlap of the output drive transistors. During the time that the crossover between logic high and logic low occurs, the power bus is virtually shorted to ground through two partially saturated transistors, as well as a current limiting resistor. This resistor is designed to keep the inrush of surge current to a level that prevents damage to the drive circuitry.
3. To avoid crossover conduction currents, manufacturers are providing Schottky barrier diodes to prevent the output transistors from going into excessive saturation. Other design techniques used within the fabrication of the component include "output edge rate control." This is accomplished by replacing one large-output transistor with several smaller ones. The peak current surge is still significant, along with potential on-chip problems related to functionality if the component has a large number of output drivers.
4. RF voltages and capacitive crosstalk can exist during the voltage swing between logic low and logic high.
5. The current that is required to change logic state from low to high or high to low is also larger than the quiescent current. This load current is calculated to be

$$I_t = C\frac{dV}{dt} \tag{3.1}$$

where $C$ is the sum of the distributed capacitance of the load, *plus* the trace capacitance to ground. For single-sided boards, $C$ is 0.1 to 0.3 pF/cm. For multilayer, $C$ is 0.3 to 2 pF/cm, and input capacitance is as shown in Table 3.2.

For example, if we have a 3.5-V, 2-ns edge rate signal, with a 7-cm-long trace on a single-layer board, with a fanout of 5 gates, the transient output current is

$$I_t = (7\text{ cm} * 0.3 \times 10^{-12} F / \text{cm} + 5 * 5 \times 10^{-12} F / \text{gate})\frac{3.5\text{ V}}{2\text{ ns}} = 47\text{ mA} \tag{3.2}$$

The peak current in this equation combines nonsymmetrical current usage with the power supply transition current. For low-to-high transitions, this current is added to the quiescent current. For high-to-low transition, the current is subtracted from the quiescent current, since the gate is *sunk* to ground and the capacitive charge from the load must discharge into the output driver's gate, which appears as a short to ground.

For products that are sensitive to input current draw, such as portable electronic devices powered by a battery with a limited time of operation, consideration must be made for all components specified in the Bill of Materials. This includes all second-source com-

ponents where alternative manufacturers provide a device for a particular function. Different manufacturing processes allow one device to consume more input current than another, either during quiescent operation or logic switching. The measurement, or calculation of the transient output current should be made with all device pins switching simultaneously under maximum capacitive load. This determines the worst case conditions that may exist. Consideration must also be made for usage at elevated temperatures where input current draw may be greater than that specified in its respective data sheet.

Another concern related to radiated EMI emissions is due to the difference between manufacturers of active digital components. Although a digital device may be form, fit, and function compatible, differences exist in the manufacturing process (and design). Not every manufacturer designs its components in the same way; hence, design engineers should not assume identical results from similar components related to functionality or EMC compliance, especially if behavioral models are used for simulation purposes.

## 3.3 CLOCK SKEW

With increasing performance requirements in high-technology products, greater emphasis on the design of low clock skew circuits is required. Clock skew, the difference in time between simultaneous clock transitions within a network at various points of arrival, is a major component constraint that forms the upper bounds of the system clock frequency. Reduction in system clock skew improves operational performance without having to resort to a higher speed logic device such as ECL or GaAs.

System designers want to utilize as much of the clock cycle as possible without adding unnecessary timing guard bands. Propagation delays of peripheral logic do not scale with frequency. As a result, when the clock period decreases, the designer has less time to perform a specific function with more logic devices to trigger. This is often a difficult task to achieve. A viable option is to use a special clock source that minimizes clock uncertainty.

To illustrate this situation, a 33-MHz component has a clock cycle of $T_{cycle} = 30$ ns. A 74FCT240, for example, has a high–low uncertainty ($t_{plh}$ to $t_{phl}$) of approximately 3.3 ns. If a pin-to-pin skew of 1.7 ns exists on the part, along with the propagational delay within the trace, we may have only 25 ns of the clock period available instead of 30 ns. Taking this example to a new level, we see that a 50-MHz system has a penalty of 25%. This allows for a maximum of 10% of the period permitted for clock distribution.

If use of multilevel clock drivers is required, additional clock skew may be added to the circuit. This is exactly what we *want to avoid.* Use of "multi-output," not "multilevel," clock skew buffers is being provided to address this problem. The drawback of these devices is that, although they meet timing requirements in the time domain, a large amount of radiated RF energy will emanate from the device package when observed in the frequency domain. Even with the best design techniques implemented for suppressing of RF energy on a PCB, reducing radiated noise from a component is difficult, if not impossible to eliminate, except through containment and use of a metal case, a grounded heatsink, or overall system shielding.

An important consideration when designing with a clock driver circuit is that the specifications provided are for a fixed, lumped capacitive load. With various devices on the net, the capacitance of the transmission line may be altered from optimal conditions,

hence exacerbating the creation of common-mode currents and increasing ground bounce. With this situation, various loads distributed over several inches of a PCB trace can contribute additional delay. The system designer must use caution to minimize total system skew. In other words, changing a clock driver to a low-skew device may not solve all timing problems. In fact, an increase in RF emissions usually occurs.

Skew is divided into three parts: duty cycle skew, output-to-output skew, and part-to-part skew. Depending on the specific application, each component can be of equal or overriding importance.

### 3.3.1 Duty Cycle Skew

Duty cycle skew is the difference between $t_{plh}$ and $t_{phl}$ related to propagation delay between components. This is illustrated in Fig. 3.2. Because of the difference in $t_{plh}$ and $t_{phl}$, pulse width distortion of the duty cycle is identified as pulse skew. This skew is critical in applications when both edges, or when the duty cycle of the clock signal, is important. This is generally observed in microprocessor designs [8].

### 3.3.2 Output-to-Output Skew

Output-to-output skew is the difference between the propagation delay of all outputs of a clock driver. This skew is dependent on the design of the component's output transistors being identical. If the skew between all edges is a critical parameter, we need to add this time parameter to the duty cycle skew to acquire total system skew. Generally, output-to-output skew is smaller than duty cycle skew for TTL and CMOS devices. Because of the near zero-duty cycle skew of differential drivers, (e.g., ECL or LVDS), a single device driver provides a clock signal to a load, or when multiple load devices on the net must be clocked at exactly the same time with respect to each other. This situation is caused by the design of the wafer (die) internal to the component package. Because of the manufacturing process used, this skew will be significantly less than the propagation delay that is specified in the device's data sheet. Figure 3.3 illustrates output-to-output skew [8].

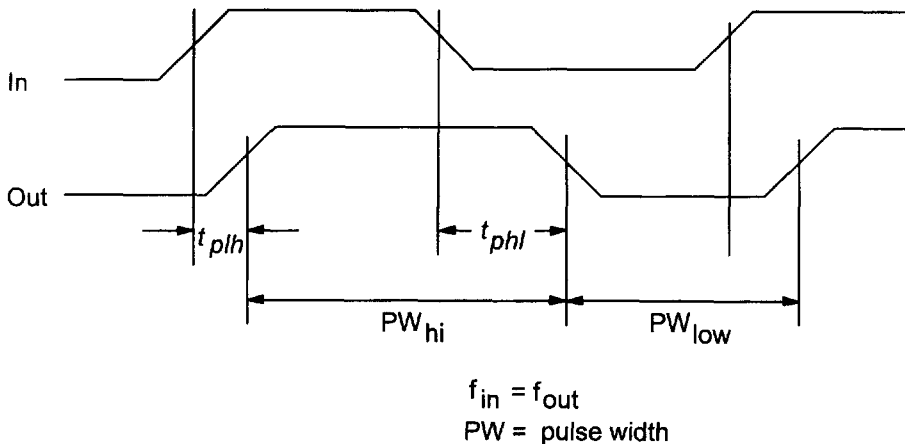



**Figure 3.2** Duty cycle skew.

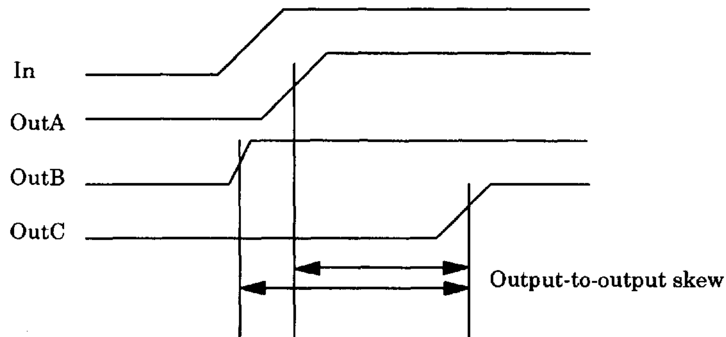



**Figure 3.3** Output-to-output skew

### 3.3.3 Part-to-Part Skew

The part-to-part skew specification is by far the most difficult performance aspect of a device to minimize, owing to the environment in which a device is located in and the manufacturing process being used to manufacture the clock driver. This skew is significantly greater than duty cycle or output-to-output skew and is based on nonvarying environmental conditions. It is advisable to study carefully the data sheet on devices used to ascertain the conditions in which the part is guaranteed to function. If the part-to-part skew specified is different from the propagation delay window for the device, we can assume that constraints must exist for the device's part-to-part skew specification [8].

## 3.4 COMPONENT PACKAGING

Consideration must always be given to placement of components on a PCB along with their interconnect traces, bus structures, and decoupling capacitors. A design parameter that is generally *not* considered by design engineers (and always overlooked because "that's the way it is") is how digital components are packaged (silicon substrate in its protective case, either plastic or ceramic). Design engineers generally agree that a device is a device and must be used in a design based on desired functionality and cost. The case packaging is a parameter that is generally outside the control of the design engineer. With this situation, why worry about component packaging? Speed is the only important parameter in high-technology designs according to the marketing document or engineering functionality specification. In reality, component packaging plays a major role in the development or suppression of RF currents.

The inductance of individual leads within a component package creates several problems, the greatest concern being that of *lead-length inductance*. This inductance allows several abnormal operating conditions to exist. These concerns are ground bounce and creation of a small loop antenna that may radiate RF currents based on the physical dimensions that exist between source and load. Ground bounce causes glitches to occur in logic input circuitry whenever the device's output switches from one logic state to another. Ground bounce is discussed later in this chapter.

Although it may seem minuscule, the loop area of the die, its bonding wires to a pad, and the component leads to the PCB can become significant contributors to the creation of EMI. This is especially true with very-large-scale integrated (VLSI) components and heavily populated PCBs with high-speed (edge rate) parameters. With multilayer PCB stackups, the trace radiating loops are so small that IC leads can become a large radiating antenna relative to loop area and the frequency generated within the component.

A detailed discussion on how differential-mode currents produce radiated emissions is found in Chapter 2. Differential-mode currents are set up by the existence of a loop between components and a plane on a multi-layer board. For inductance to exist, a loop must be present. To minimize inductance, the loop area must decrease in size. This inductance includes the length of the bond wires internal to components, internal bond leads for capacitors, resistors, and other passive components. A review using Fig. 3.4 examines how loops create radiated emissions.

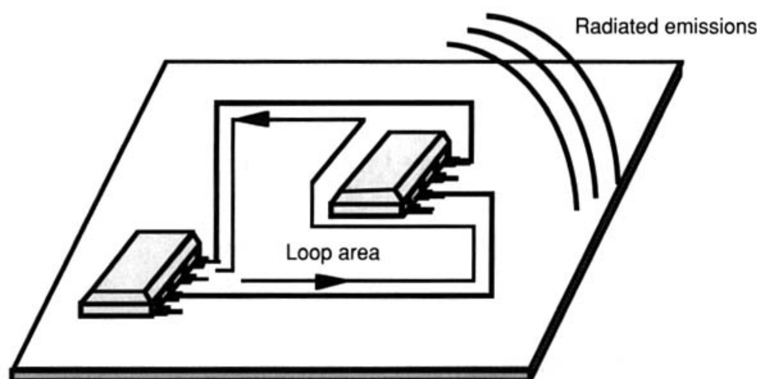



**Figure 3.4** Loop area between components.

With lead-length inductance in mind, the worst type of component packaging is the standard TTL Dual-In-Line Package (DIP) where the power and ground pins are at opposite corners. This arrangement is illustrated in Fig. 3.5.

In most PCBs, primary emission sources are established from currents flowing between components. Radiated emissions can be modeled as a small-loop antenna carrying interference current shown in Fig. 3.4. A small loop is one whose dimensions are smaller than a quarter wavelength ($\lambda/4$) at a particular frequency of interest. For most PCBs, loops exist with small dimensions for frequencies up to several hundred MHz. When a dimension approaches $\lambda/4$, RF currents within the loop will appear out of phase at a distance such that the effect causes the field strength to be reduced at any given point.

Common-mode current is more difficult to control and normally determines the overall emissions performance. Common mode is generally observed from cables affixed to the unit. RF energy is determined by the common-mode potential (usually ground-noise voltage) and is not the same as differential-mode radiated energy. Common-mode current may be modeled as a monotonic antenna driven by ground-noise voltage. For a short monopole antenna of length $L$ over a ground plane, the magnitude of the electric field strength can be measured at a distance $r$ in the far field.

To predict the maximum electric field strength from a loop over a ground plane, Eq. (3.3) is used [4]. Differential-mode radiated emissions is best controlled in the design and layout of the PCB or product.

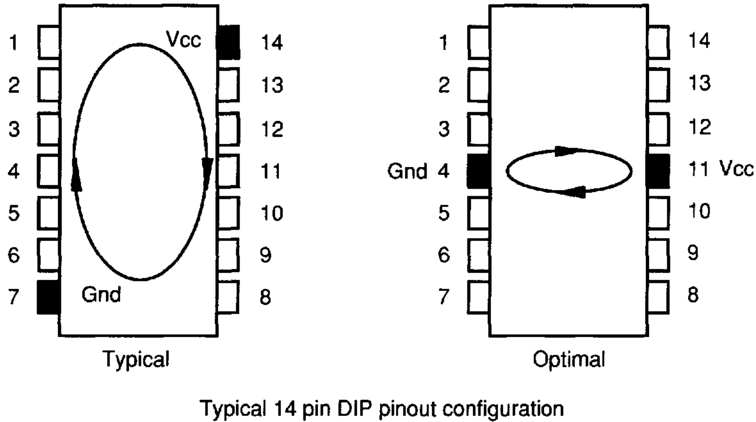



**Figure 3. 5** Component packaging related to RF loops—DIP configuration.

$$E = 263 * 10^{-16} (f^2 * A * I_s)\left(\frac{1}{r}\right) \text{ volts per meter} \quad \text{(differential-mode)}$$

$$E = 4\pi * 10^{-7} (I_s * f * l)\left(\frac{1}{r}\right) \text{ volts per meter} \quad \text{(common-mode)} \tag{3.3}$$

where $E$ = effective radiated field (V/m)
$A$ = loop area ($cm^2$)
$f$ = frequency (MHz)
$I_s$ = the source current (mA)
$l$ = length of the trace or cable (meters)
$r$ = distance from the radiating element to the receiving antenna (meters)

The maximum loop area that will not result in E-field levels to exceed a specific specification level is described by Eq. (3.4).

$$A = \frac{380\, Er}{f^2 I_s} \tag{3.4}$$

In free space (typically described as a minimum distance from the radiating source as wavelength, $\lambda$, divided by $2\pi$), radiated energy decreases with inverse proportion to distance between source and antenna. The loop area on the PCB must be known, which is the total area of the circuit between the trace and RF current return path. A convoluted shape may be present, which is at times difficult to determine for a single frequency of interest using Eq. (3.3). The equation must be solved for *each and every loop* (different loop-size areas) and for each frequency of interest if the full profile is to be understood.

Using Eq. (3.3), we can determine if a particular routing topology needs to have special attention as it relates to radiated emissions. This special attention may involve some or all of the following: re-routing the trace stripline, changing routing topology, locating source and load components closer to each other, or providing external shielding of the assembly (containment).

To help minimize loop area, we can select logic components (to the extent possible), with power and ground pins located in the center of the package (not on opposite corners) or physically adjacent to each other. Power pins in the center provide for optimal placement of decoupling capacitors (when these capacitors are placed on the bottom side of the PCB). This configuration also minimizes trace length connections between the device and decoupling capacitor, in addition to minimizing trace length inductance from the power and ground pins *internal* to the silicon wafer (die) of the package. Since a via is required to bring both power and ground to the device (when both power and ground planes are provided in a multilayer PCB stackup assignment), these same vias can also be used for the local decoupling capacitor.

Surface-mount technology (SMT) components have an advantage over through-hole devices by virtue of a smaller loop area related to creation of RF currents. In Fig. 3.5, we notice that a reduction in loop area exists when the power and 0V reference pins are located in the center of the device instead of opposite corners. A similar reduction in loop area also occurs on larger packaged components where the power and ground pins are provided adjacent to each other, as illustrated in Fig. 3.6. Adjacent power and 0V reference interconnect bond wires minimize loop areas for RF currents that may be developed and allow for enhanced flux cancellation (or minimization) between power and ground. If RF currents exist on power input pins due to differential-mode switching currents created by simultaneously switching all pins under maximum capacitive load, a more stable 0V reference system must be available. RF flux will see this alternate return path (0V reference), thus canceling out internally generated RF currents by minimizing differential-mode ground-noise voltage.

With this consideration in mind, use of surface-mount technology (SMT) components is preferred to through-hole in minimizing RF emissions. This characteristic difference is due to shorter lead-length inductance from the die of the component to the circuit trace on the PCB. SMTs by virtue of package size have smaller loop areas. Internal lead-

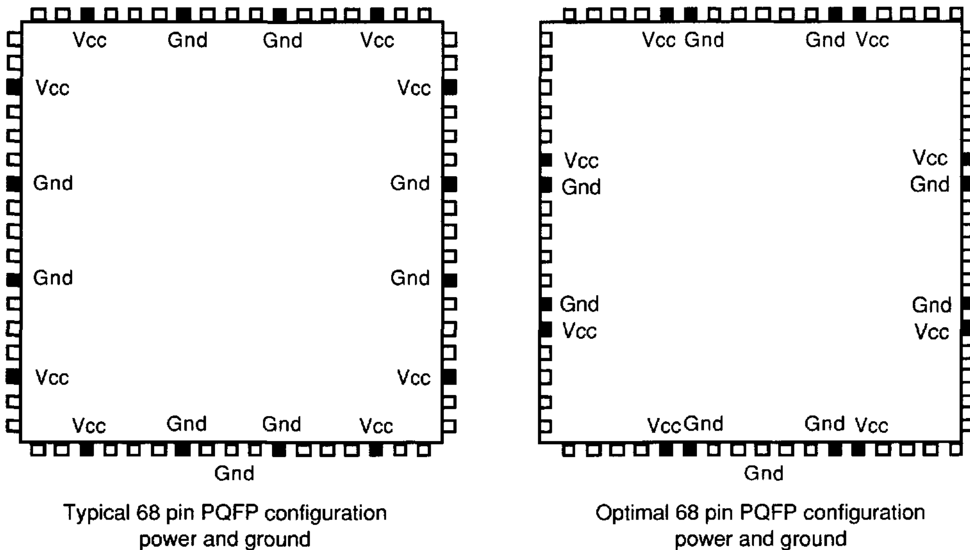



**Figure 3.6** Pinout location of larger components.

length inductance also exists. Inductance is a component that generates RF currents. RF currents cause RF emissions, in addition to possibly causing signal integrity problems. Sometimes through-hole devices are installed on sockets. Sockets add greater lead-length inductance and hence create greater amounts of EMI since the loop area is increased.

Another design feature built into components that either promote or demote creation of RF currents is the manner in which IC package leads are bonded to the PCB. An example of two different lead bond configurations is shown in Fig. 3.7.

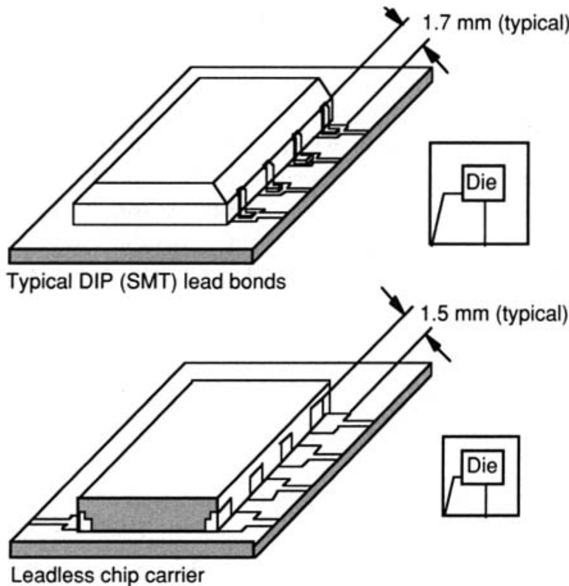



**Figure 3.7** Lead bonding to the PCB.

Although the loop area appears to be extremely small, bonding wires internal to the package, along with the external interconnect leads, allow for significant RF paths to be developed. Multilayer boards minimize RF currents because the loop area for the traces are small compared to the overall inductive lead-length internal to the device. In other words, bond wires can become significant antennas, especially at high frequencies or with logic devices that operate in the sub-nanosecond range. Issues with bond wires are becoming more common in today's high-technology products. With this situation, the use of DIP packaging provides for the greatest amount of RF field development, especially if a through-hole socket is provided. Table 3.3 presents values of lead-length inductance of various logic packages [2].

SMTs also provide superior performance over DIP components as there is approximately a 40% reduction in package size. This translates to a 64 percent reduction in the lead length inductance in the radiating loop between the die and the mounting pad. In addition, SMTs use less board space with corresponding less trace lengths between components (smaller board size). With the use of SMT components, the decoupling capacitor loop area is also reduced (see Chapter 5).

A variety of packaging configurations exist. Almost all packages when used at high speeds suffer from problems associated with lead-length inductance, lead capacitance, and heat dissipation. The inductance of individual leads within a device package creates a problem identified as *ground bounce*. Ground bounce causes glitches in logic inputs dur-

**TABLE 3.3** Lead-Length Inductance of Various Logic Packages

| Package Size and Type | Lead-Length Inductance |
|---|---|
| 14 pin DIP | 2.0 – 10.2 nH |
| 20 pin DIP | 3.4 – 13.7 nH |
| 40 pin DIP | 4.4 – 21.7 nH |
| 20 pin PLCC | 3.5 – 6.3 nH |
| 28 pin PLCC | 3.7 – 7.8 nH |
| 44 pin PLCC | 4.3 – 6.1 nH |
| 68 pin PLCC | 5.3 – 8.9 nH |
| 14 pin SOIC | 2.6 – 3.6 nH |
| 20 pin SOIC | 4.9 – 8.5 nH |
| 40 pin TAB | 1.2 – 2.5 nH |
| 624 pin CBGA | 0.5 – 4.7 nH |
| Wire bonded to hybrid substrate | 1 nH |

ing a state transition from a driving source. We will now examine the magnitude of these glitches and their effects.

## 3.5 GROUND BOUNCE

A major concern associated with the development of RF emissions from a digital device is ground bounce. Ground bounce causes RF noise (differential-mode) to be produced by the simultaneous switching of drivers within an IC package. By examining details within the component, we gain a better understanding of what happens within the PCB. Differential-mode voltages ultimately result in radiated emissions because common-mode currents are accordingly established. To better understand this phenomenon, we will examine a component using a micromodel analysis.

A qualitative relationship exists between ground bounce and emissions at the system level. Designers tend to limit the noise threshold below 500mV for zero-to-peak amplitude of ground bounce glitches. When a ground bounce glitch exceeds a threshold level, emissions increase, along with false triggering of components on the routed net (poor signal quality). Ground bounce is difficult to solve especially when emissions from a product exceed regulatory requirements. Sometimes the unit ceases to function properly. When diagnosing a signal integrity problem, EMI concerns may be eliminated or reduced when the signal integrity problem is solved.

In addition, ground bounce presents a situation in which the ground reference system is not at a constant 0V reference value. Transistors within a component package will not sense an active signal properly if the ground reference subsystem is not stable or is constantly changing.

*Ground bounce develops a common-mode potential between the device die and the parent (PCB) image plane (0V return path) and in this mode will couple this potential to all device signals by superimposition. This superimposition can occur on both the power and ground structure. Ground bounce is directly related to the large instantaneous current flow through*

*the power supply inductance and is not due to the output capacitance or inductance of the transmission line being driven. Ground bounce is also dependent on the physical location of the device driver as well as the number of outputs that switch at the same time with respect to a power and ground pad on the die. Bounce is directly related to the dI/dt of the output driver gate (switching speed of the pre-driver within the die circuitry).*

Figure 3.8 illustrates an idealized logic circuit internal to a semiconductor. We assume four leads: $V_{in}$, $V_{out}$, $V_{cc}$, and $V_{gnd}$. The device shown is a totem-pole configuration. In reality, all logic device families exhibit similar ground bounce problems at high speeds of operation. When Switch 2 closes, the load capacitor $C$ is shorted to ground. As the voltage across $C$ falls to 0V, the stored charge flows back to ground, causing a massive current surge within the ground return circuit. This current is identified as $I_{\text{discharge}}$.

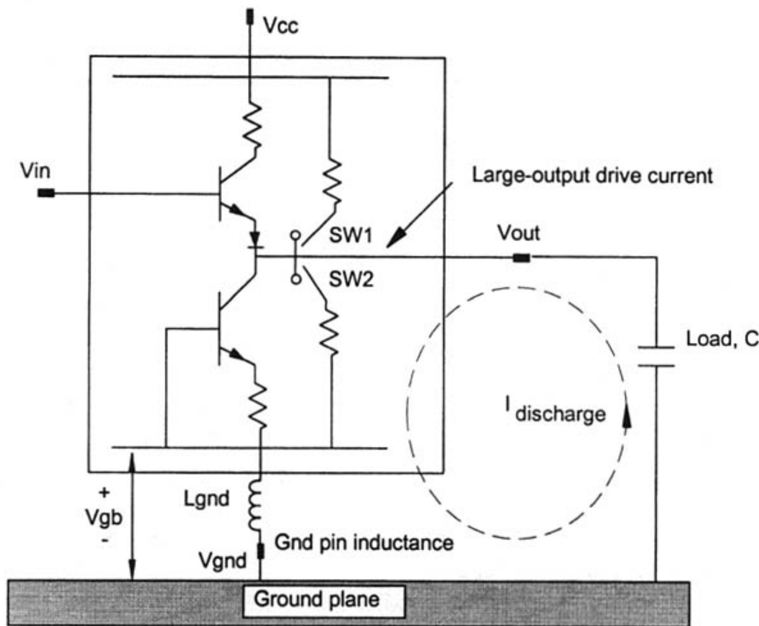



**Figure 3.8** Lead inductance within a component.

As the capacitor's current is replenished with voltage and then discharged again, working against the inductance in the ground return pin, $L_{gnd}$, a voltage $V_{gb}$ is induced between the system ground plane underneath the device and the ground reference internal to the device. The magnitude of this voltage is shown in Eq. (3.5). We identify $V_{gb}$ as the ground bounce voltage.

$$V_{\text{gb}} = L_{\text{gnd}} \frac{dI_{\text{discharge}}}{dt} \tag{3.5}$$

Another explanation of how ground bounce is created has to do with when a gate switches from one logic state to another. Both n and p transistors of the gate are on, and current is sunk between the power and ground planes of the PCB. This current places an additional requirement on the power distribution network which may be insufficient for

optimal performance. This explanation of the switching of the two transistors in the gate being in conduction is not the most acceptable one, since the resistance between the power rail ($V_{cc}$) to the top transistor and from the bottom transistor to ground (Gnd) limits the current from $V_{cc}$ to Gnd significantly. Thus, the primary source of the ground bounce, in the totem-pole configuration of TTL circuits, is the load capacitance discharge to ground through the gate.

Switching elements demand an almost instantaneous change in drive current. The inductance in the lead bonds of the component, trace inductance, and other parasitic inductance causes this instantaneous drive current to occur. The power supply assembly cannot absorb an instantaneous change of current. As a result, a voltage difference is created between the ground and power pins of the component and the lead bond connections. Ground bounce will appear as noise in both the component's power and ground structure. Under this condition, reduced noise margin is observed which may permit false triggering of a voltage-level sensitive trace. From a functional perspective, the noise margin is usually smaller for the low-logic state than for the high-logic state. It is the low-logic state that is of greater concern for system-level functionality.

Usually, the measured ground bounce voltage, $V_{gb}$, is small compared with the full-swing output signal voltage. Ground bounce does not often affect the transmitted signal. It does, however, interfere with reception of the signal by the load. This is because the receiver compares its input voltage against the internal, local 0V reference. This difference appears as a (+) input connected to a (-) input. Since the internal ground carries the $V_{gb}$ pulse, the actual differential voltage observed at the receiver's input is: $V_{in} - V_{gb}$. This condition is representative of TTL circuits. CMOS compares its input against a weighted average of both power ($V_{cc}$) and ground. ECL components compare their input against $V_{cc}$. Although the topology is different between logic families, the concept of ground bounce is the same. If we simultaneously switch N outputs from a component into N corresponding capacitive loads, we have N times as much ground current and pulse $V_{gb}$ grows N times larger.

Fundamentally, information is processed within a digital device by variations of voltages between logic states. Figure 3.9 illustrates a CMOS gate and associated parasitic impedance. In the high-to-low transition state, the load capacitance, $C_L$, is assumed to be 50 pF. A 5V potential across $C_L$ equates to 250 pCoulombs *($Q = CV$)* within the capacitor. This charge must be transferred through the device in order to bring the load to the low state (0V potential). During this high-to-low transition, the charge stored in the capacitor will flow from the load through the ground pin of the device. When this happens, the rate of change of current ($dI/dt$) develops a voltage drop across the inductance of the ground reference pin. This internal lead and ground return inductance can cause overshoot, undershoot, and even ringing in high-speed logic families.

When ground bounce occurs, the waveform depicted in Fig. 3.10 is observed. The charge that is impressed across the PCB trace results in a common-mode voltage. It is this common-mode voltage that causes RF emissions. Because we are unable to eliminate the transfer of charge between logic state transitions, we must limit the magnitude of the RF current peaks. This is best accomplished by having a very low-impedance path across the power and ground structure of the PCB.

Ground bounce gets worse under the following conditions, as a result of increased current drawn from the power distribution network.

- Capacitive loading is increased.
- Load resistance is decreased.

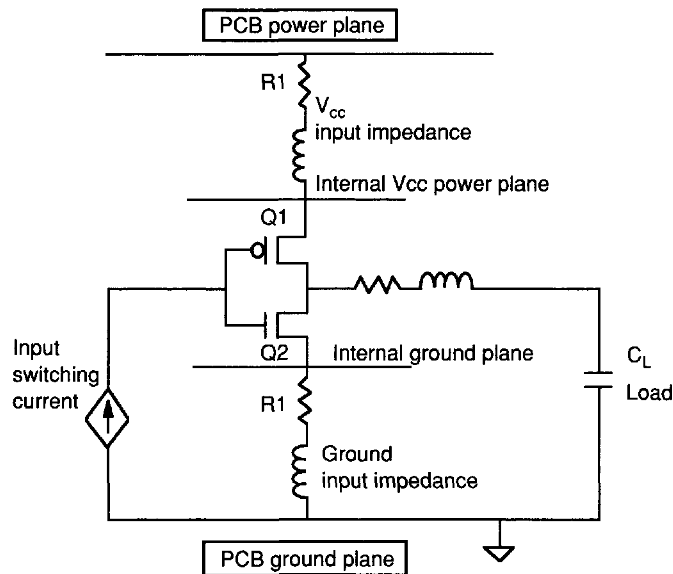



**Figure 3.9** Typical CMOS output.

- Lead and trace inductance is increased.
- Multiple gates (devices) switch simultaneously.

To remove ground bounce, several techniques are commonly used. Slowing down the output switching time is the preferred method. Certain components are now being provided with clock skew circuitry to slow down the edge rate, in addition to providing a series resistor internal to the silicon die.

Other manufacturers use multiple ground wire bond leads internal to the device package. This is acceptable if the wires are evenly spaced throughout the device as lead-length inductance is decreased. Spreading the ground connections throughout the components is better than lumping the pins together.

When designing a PCB layout, a separate ground connection should be provided for each ground pin directly to the ground plane. Connecting two ground terminals together and running them through a single trace to a common grounding point (via) defeats the purpose of having independent ground leads.

Other methods to minimize ground bounce include

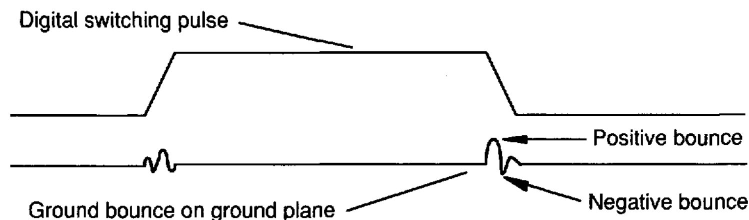



**Figure 3.10** Typical ground bounce waveform

1. *Load control*—lower the capacitance and increase resistance.
2. *Layout*—minimize the inductance during layout of the PCB for power and ground, not just the output signal traces.
3. *Component packaging*—use devices with a ground reference pin in the center of the device (4 nH) instead of the corners (15 nH). Surface-mount devices are preferred to through-hole components for this reason.

The design enhancements that a component manufacturer may use to minimize ground bounce for their product include the following list.

1. Decrease trace inductance for both the power/ground pins.
2. Use double bonding wires from the die to the securement pads.
3. Use wider mounting pads as opposed to narrow ones.
4. Decrease the lengths of bond wires within the package.
5. Shorten the height of the pins or lower the profile of the package plastic quad flat pack (PQFPs have less lead-length inductance than pin grid array [PGA] packaging).
6. Provide a high ratio of ground pads to signal pads.
7. Provide an extra ground plane inside the component's package.
8. Provide buried substrate capacitance for application-specific integrated circuits (ASICs).
9. Provide for an on-chip decoupling capacitor internal to the package (built-in power and ground plane between the die and package using the securement glue as the dielectric material).
10. Locate power and ground pins adjacent to each other, preferably in the center of the device so that inductance can cancel magnetic flux lines and minimize development common-mode currents.
11. Provide Low Inductance Capacitor Array (LICA) capacitors internal to Multi-Chip-Module (MCM) packaging.
12. Use low-inductance flip chip packaging.

## 3.6 LEAD-TO-LEAD CAPACITANCE

A factor that affects the RF emission profile of a component, in addition to lead-length inductance, is stray capacitance between adjacent pins internal to a device. Noise voltages can couple between pins and cause functionality concerns to exist. What really occurs in this situation is crosstalk. If a high RF spectral profile signal is created within a component, and capacitive coupling occurs on an adjacent pin (lead) or trace, it becomes extremely difficult to isolate and implement design enhancements for both signal integrity or regulatory compliance issues. An illustration of capacitive coupling that occurs between component leads is shown in Fig. 3.11.

The percentage of crosstalk that exists between two pins is described by Eq. (3.6). Capacitive crosstalk becomes more pronounced as the rise times become shorter (faster

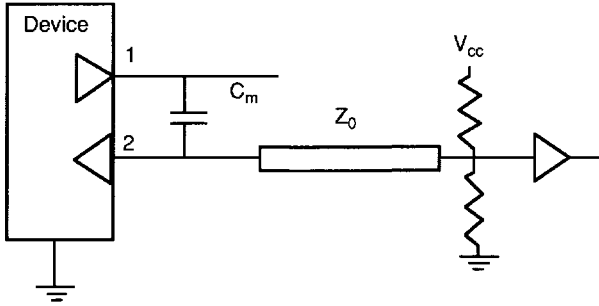



**Figure 3.11** Capacitive coupling between component pins.

edge rate). Crosstalk is also made worse when high-impedance transmission lines are provided to the circuit. A high-impedance transmission line adds more capacitance, which contributes to the overall performance of the device. A detailed discussion of crosstalk is presented in Chapter 7, which gives us a better understanding of this equation.

$$\text{Crosstalk} = \frac{ZC_m}{T_{10-90}} \tag{3.6}$$

where $C_m$ = mutual capacitance between lines 1 and 2
$Z$ = the parallel impedance of the trace and terminator $(Z_o \| R_t)$
$T_{10-90}$ = the 10–90% edge rate of the signal on the output pin

## 3.7 GROUNDED HEATSINKS

Grounded heatsinks, a new concept in PCB suppression, finds use in specific applications and for certain components. Grounded heatsinks are sometimes required when using VLSI processors with internal clocks in the 75-MHz range and above. These CPU and VLSI components require more extensive high-frequency decoupling and grounding than do most other parts of a PCB.

New technology in wafer fabrication easily allows component densities to exceed 1 million transistors per die. As a result, some components consume 15 watts or more of DC power. Certain components which exceed 15 watts of power and require separate cooling provided by a fan built into their heatsink or by location of the device adjacent to a fan or cooling device. Since these high-power, high-speed processors are being implemented in more designs, special design techniques are now required for EMI suppression and heat removal at the component level.

When we examine the function of a heatsink in the thermodynamic domain, we see that removal of heat generated internal to the processor must occur. Components that dissipate large amounts of heat are usually encapsulated in a ceramic case since ceramic packaging will dissipate more heat than a plastic package. Ceramic cases also cost more. Certain components, due to large junction temperatures between internal gates, generate more heat than the ceramic package can dissipate; hence, a heatsink is required for thermal cooling.

Having briefly discussed the function of heatsinks in the thermodynamic domain, we now examine the metal heatsink in the RF domain. For proper thermal implementation

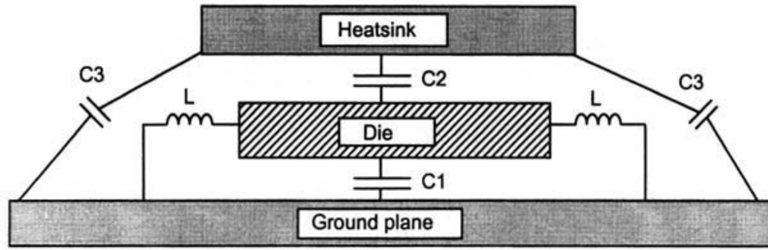
and use of heatsinks, a thermal conductor (silicon compound or mica insulation) is provided. This compound is generally electrically nonconductive. This conductor contains excellent thermal properties for transferring heat from the component to the heatsink. Examining metal heatsinks in the RF domain, we observe the following characteristics, illustrated in Fig. 3.12 and Fig. 3.13.

- Wafer dies operating at high clock speeds generally 75 MHz and higher generate large amounts of common-mode RF current internal within the package.
- Decoupling capacitors remove differential-mode RF current that exists between the power and ground planes and signal pins.
- Certain ceramic packages contain solder pads on top of the package case to provide additional differential-mode power filtering required by the large power consumption in addition to high-frequency decoupling. Decoupling capacitors minimize ground bounce and ground-noise voltage created by the simultaneous switching of all component pins under maximum capacitive load.
- The wafer (or die) internal to the package (Fig. 3.13) is located closer to the top of the case (dimension "X") than the bottom of the package (dimension "Y"). Therefore, height separation from the die to an image plane internal to the PCB is greater than the height of the die to the top of the package case and heatsink. Common-mode RF currents generated internal within the wafer have no place to couple to 0V reference; hence, RF energy is radiated into free space. Differential-mode decoupling capacitors will not remove common-mode noise created within the component.
- Placing a metal heatsink on top of the component provides a 0V reference (image plane) closer to the wafer than the image plane on the PCB. Tighter *common-mode* RF coupling occurs between the die and heatsink than between the die and the first image plane of the PCB.
- Common-mode coupling that occurs to the heatsink now causes this thermodynamically required part to become a *monotonic antenna,* perfect for radiating RF energy into free space.

The net result of using a metal heatsink is the same as placing a monotonic antenna inside the product to radiate clock harmonics throughout the entire frequency spectrum. To deenergize this antenna, the heatsink must be grounded. Although this concept is very simple to understand, it is virtually ignored within the field of PCB design for RF energy suppression.

A VLSI component can be an effective radiator of RF energy. Adding a heatsink adds yet one more design parameter when considered in the frequency domain and not just within the thermodynamic domain. In general, as the size of the heatsink increases, radiation efficiency increases. The maximum amount of radiation will occur at different frequencies depending on the geometry of the heatsink and self-resonant frequency of the assembly if the heatsink is a metallic structure.

Heatsinks must be grounded to the ground planes (or 0V reference) of the PCB by a metal connection on all four sides. Use of a fence (similar to a vertical bus bar) from the PCB to the heatsink will encapsulate the processor. This fence will create a Faraday shield around the processor, thus preventing common-mode noise RF energy internal to the package from radiating into free space or coupling onto nearby components, cables,




Typical self-resonant frequency of VLSI processors is approximately 400 to 800 MHz with heatsink.

**Figure 3.12** Grounded heatsink theory of operation.

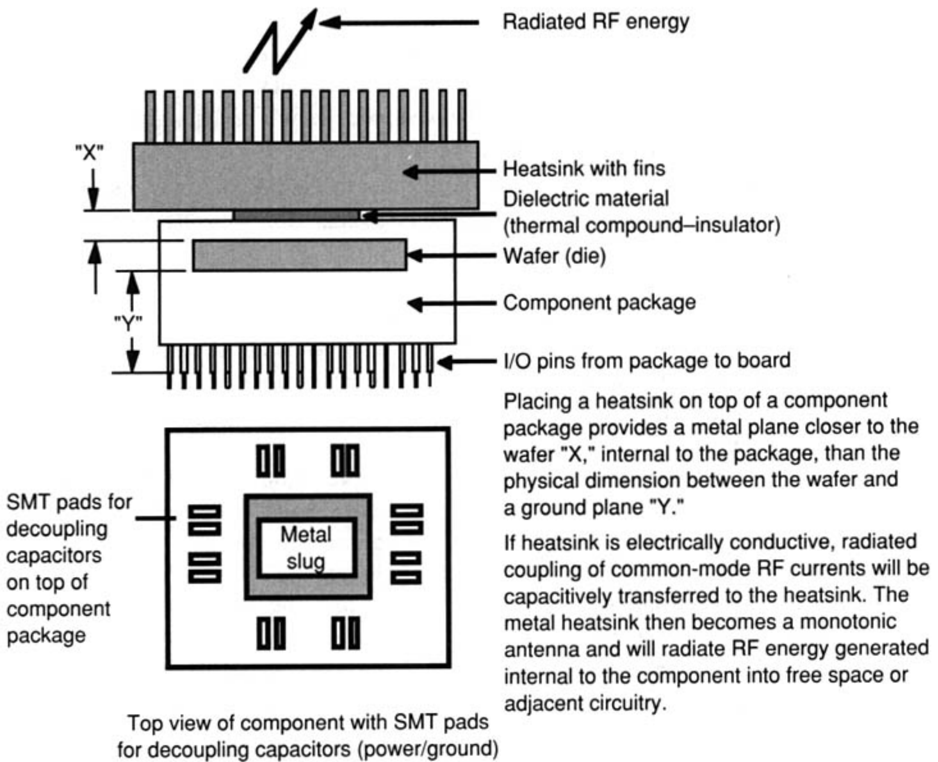



**Figure 3.13** Grounded heatsink implementation.

peripherals, or into aperture slots. A technique for providing grounding of the heatsink is shown in Fig. 3.14.

Reduced Instruction Set Computing (RISC) processors or VLSI components generally have a high self-resonant frequency that is a combination of the manufacturing process and internal clock speed, in addition to the impedance present in the power planes during maximum power consumption. As a result, VLSI components radiate RF energy more than many other components if RF suppression techniques were not incorporated by the component manufacturer. Any attempt to remove this self-resonant RF frequency using standard design suppression techniques is almost impossible except through use of the heatsink as a *common-mode decoupling capacitor.*

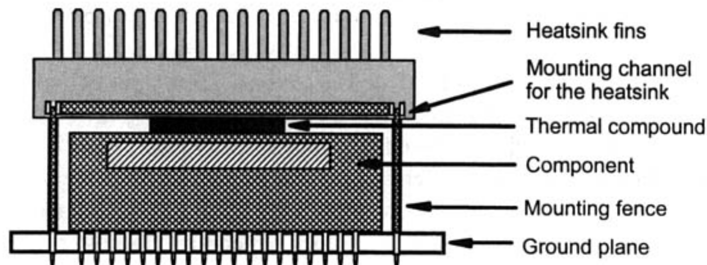



**Figure 3.14** Grounding the heatsink.

This heatsink is generally used in conjunction with both differential-mode capacitors located on the top of the components' ceramic package, if provided, in addition to the standard differential-mode capacitors located under the component directly on the PCB. A differential-mode decoupling capacitor connects directly between the power and ground planes to remove switching noise from these planes. A common-mode decoupling capacitor provides an AC shunt to remove CM noise generated internally from the die to the ground reference system.

A grounded heatsink must always be at *ground potential.* The active component is always at *RF voltage potential.* The thermal compound is a dielectric insulator between two large plates. The definition of a capacitor is fulfilled. Thus, a grounded heatsink works as one large *common-mode decoupling capacitor,* while optional discrete capacitors located on top of the device package or directly on the PCB are used for *differential-mode* decoupling. This common-mode capacitor shunts RF currents generated within the processor to ground.

Using a grounded heatsink creates

1. A thermal device to remove heat generated internal to the package.
2. A Faraday shield to prevent RF energy created from the clock circuitry internal to the processor from radiating into free space or corrupting adjacent circuitry.
3. A "common-mode" decoupling capacitor that removes common-mode RF currents generated directly from the die, or the wafer, inside the package, by AC coupling RF energy from the die to ground.

If a grounded heatsink is implemented, the grounding fingers of the fence (spring fingers or other PCB mounting method employed) must be connected to all ground planes, or the 0V reference structure in the PCB on at least 1/4 inch (0.125 cm) centers

around the processor. At each and every ground connection, install two sets of parallel decoupling capacitors, alternating between each ground pin of the fence with 0.1 μf in parallel with 0.001 μf, and 0.01 μf in parallel with 100 pF. RF spectral distribution from RISC processors and similar components generally exceed 1-GHz bandwidth. RISC or VLSI processors also require more extensive multipoint grounding around all four sides of the processor than most other types of components. These capacitive values complement the approximate λ/4 mechanical size of typical heatsinks, making them efficient suppressors of EMI spectra.

## 3.8 POWER FILTERING FOR CLOCK SOURCES

Oscillators are one source of radiated emissions. The output of their periodic waveform is transmitted down a PCB trace to a load. Depending on the layout of the PCB, component placement, trace routing, decoupling, impedance control, and other items related to flux cancellation or minimization, emissions will either exist or be a nonissue related to EMC compliance. In addition, signal integrity concerns must be considered.

In some situations, oscillators (clock generation circuits) will inject RF currents on to a PCB trace. This is in addition to ground bounce that occurs as a result of poor decoupling or power supply immunity. If the oscillator is located within a noisy environment, additional power supply filtering will be required. The amount of this filtering is dependent on how much reduction in jitter must be achieved. Jitter is a small, rapid variation in the waveform owing to mechanical vibrations, fluctuation in supply voltages, and control-system instability. Basically, clock jitter refers to any deviation of a clock's output transition from their ideal operating condition. Trying to determine a precise value for jitter reduction is nearly impossible for the following reasons.

1. Different manufacturers of oscillators have different power requirements, along with a difference in actual edge rates. Although the oscillators may have the same frequency, not all oscillators have the same AC or DC characteristics.
2. Jitter performance is generally not provided in their respective data sheets or application notes. Each manufacturer of oscillators will have a different jitter requirement.
3. RF noise in a system changes when different brands of integrated circuits are used.

To minimize ground bounce and enhance power supply noise reduction, use of a filter circuit is required (see Fig. 3.15). These circuits will achieve a reduction of up to 20 dB in the frequency range above 20 MHz. Use of a two-stage filter will double the attenuation.

It is mandatory to physically locate the filter circuit as close as possible to the power input pin of the oscillator circuit to minimize RF loop currents. Depending on the frequency of the oscillator, a current loop could be present causing radiated emissions. Use of surface-mount devices is preferred over through-hole devices due to less lead-length inductance in the component package.

Two methods can be used to provide power filtering for clock sources. One involves use of an RLC circuit, the other a ferrite bead and capacitor combination, discussed below.

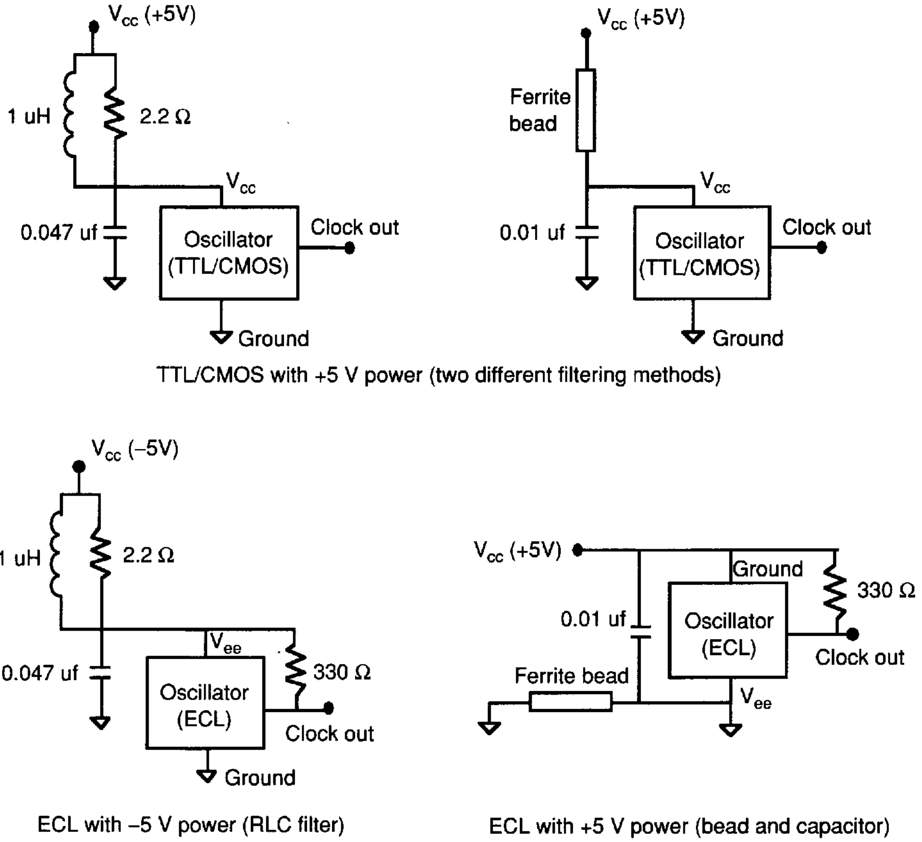



**Figure 3.15** Sample filter circuits for oscillators.

A large inductor or capacitor value will enhance the filter's attenuation at lower frequencies if this filter method is used. For any combination of $L$ and $C$, to achieve 20 dB of attenuation, Eq. (3.7) is used.

$$f_{20dB} = \frac{3.2}{\sqrt{LC}} \tag{3.7}$$

where $f$ is frequency in hertz.

If a resonance occurs in this LC circuit, reduction of the Q of the circuit may be required. This is best accomplished by use of a resistor. This resistor prevents a particular resonance from occurring and is calculated by Eq. (3.8).

$$R = \frac{1}{2}\sqrt{\frac{L}{C}} \text{ (ohms)} \tag{3.8}$$

With either filter, the oscillator is forced to draw transient current from the local decoupling capacitor. The regular decoupling and bulk capacitors located throughout the PCB would be unable to provide the fast-transient current required by the oscillator due to inductance in the power path. This local filter would keep the current loop (power and ground) from the power input circuit small, thus preventing this localized circuit from infecting the

rest of the board. The path for the transient current surges would only be from the local filter capacitor to the IC's power pin and out the IC's ground pin back to the negative side of the capacitor, a relatively small loop. This small-current loop description is applicable not only for oscillators, but also for all components that require this type of filtering.

If a ferrite bead-on-lead is provided in place of the inductor, we can eliminate the resistor. This is because the bead-on-lead at DC provides low inductance. Since the oscillator or clock generation circuitry is usually above 10 MHz in today's products, high-frequency RF energy will be prevented from entering the system's main power distribution network and corrupting other functional circuits. The local capacitor provides only decoupling to recharge the power rail for the localized oscillator circuitry. This filter combination minimizes power consumption surges and prevents the possibility of infecting the entire power distribution circuit with RF energy created by the oscillator package.

*Caution*: Use of some ferrites in power or ground can interact with the output signal's return image in the plane and alter signal quality.

## 3.9 RADIATED DESIGN CONCERNS FOR INTEGRATED CIRCUITS

Recent advances in integrated circuit (IC) components such as microprocessors, digital signal processors, and application-specific integrated circuits (ASICs) have become significant sources of electromagnetic noise. In recent years, clock rates have increased from 25 and 33 MHz to 200 through 500 MHz. Along with the increase in clock rates, there is a corresponding increase in dynamic power dissipation due to switching currents that exceed 10 watts on a typical VLSI device. Individual circuits, when isolated by themselves, generally do not radiate enough RF energy to exceed mandated regulatory limits. The RF energy that is created is frequently coupled into structures within a product assembly, which will then cause EMI problems to be observed.

These structures and assemblies include cavities created by metallic enclosures, apertures, connected cables, and the like which enhances lower-frequency emissions. Heatsinks are a prime source of radiated RF energy, discussed earlier.

The reason why some, not all, manufacturers of components do not place a high priority on EMC or radiated noise coupling (requiring the end user to accept the responsibility of solving emissions along with ground noise or ground bounce) is based on the following wish-list. These noncompliant, wish-list components are designed for

1. "Infinitely" fast rise times (zero rise times).
2. Unlimited fanout drive (unlimited power output).

With these two items, it becomes even more important to recognize that these conditions exist. Not all manufacturers produce the same product, although they may be form, fit, and function compatible. Noncompliant components must be handled with care using the following techniques.

1. Keeping short lead-lengths (lower the output loop area).
2. Keeping clock signals away from I/O circuitry and lines (prevents coupling).

3. Raising the output resistance of a clock trace with a series impedance (resistor or ferrite bead).

To address these problems of noncompliant components, EMC engineers must advance state-of-the-art principles by implementing EMI suppression techniques for ICs. These techniques must keep up with higher speed designs. Design and cost margins play an important part in determining how a solution will be implemented. Engineers must be able to predict radiated emissions using specialized tools and simulation programs. The main problem that exists with simulation analysis is finding appropriate tools, including the development of behavioral models that reflect IC parameters (actual and parasitic) along with proper voltage and current impulse (surge) characteristics.

Various studies have been performed to determine the difference in characteristic radiated emissions between ICs. These differences include packaging, layout, logic families, and different vendors for the same device. Recorded measurements show differences of up to 10 dB between different versions of the same device. An example of this difference is seen in Table 3.4 [3].

Various efforts by numerous companies involved in simulation and modeling are underway to calculate radiated emissions from components. These emissions are generally common-mode which makes it difficult to model. In contrast, differential-mode currents are easy to simulate and model. Efforts are in process to determine efficient methods of measurement techniques. Until research is available, calculating radiated emissions from ICs will remain a subject for adventurous engineers.

Radiated emissions from components can be reduced through use of the following design techniques:

- Reduction of package size; antenna efficiency (lowers the effective area of radiation).
- Reduction of high-frequency energy created within the die structure.
- Isolation of RF noise produced from the die to any IC pins that connect to external circuitry.

Selected combinations of these techniques must be used in order to reduce radiated emissions. This includes designing the component to have interconnect pads on the substrate adjacent to each other for power and ground to minimize ground bounce. Edge rate control must be implemented on periodic clock signals (series resistance or equivalent technique) to reduce high-frequency RF coupling onto adjacent traces or other metallic structures. Lower impedance bond wires must also be provided.

To minimize radiated emissions from components, see Table 3.5.

**TABLE 3.4** Radiated Emissions Between Vendors

| Radiated electric field strength (dBμV/m) at 3 m | | |
|---|---|---|
| Frequency | Vendor A | Vendor B |
| 30 MHz | 32.8 | 42.8 |
| 40 MHz | 27.5 | 33.0 |
| 50 MHz | 23.0 | 28.0 |

**TABLE 3.5** Design Concerns to Reduce Radiated Emissions from Components

| Reduce Radiation Efficiency | Reduce Coupling and Crosstalk | Reduce High-Frequency Switching Energy |
|---|---|---|
| Use a smaller package size | Use more ground pins placed strategically around the device | Use drivers with the slowest edge rate acceptable for proper operation |
| Use a ground plane inside the package | Use small distributed clock drivers instead of a single driver | Isolate areas on the die where necessary which contain clock logic |
| Use additional ground/power leads near the clock source | Use drivers with the lowest drive voltage possible | Use split power-ground structures to isolate clock noise |
| Use a shielded package | Use the slowest clock rate possible | Separate areas on the die where isolation is required |
| Group signals and power leads together | Use current limiting resistors | Isolate signal leads with ground wires |
| Use low-inductance bond wires in the package | Reduce die trace capacitance<br>Use differential clock drivers | Separate I/O ports from clock pins |

## 3.11 SUMMARY FOR RADIATED EMISSION CONTROL—COMPONENT LEVEL

The following recommendations will help minimize the amount of RF energy that is created from use of certain logic devices, especially digital logic.

- Select devices that consume less input current during logic transition states. Of concern here is the maximum inrush current of all component pins switching simultaneously under maximum capacitive load, not the average or quiescent value.
- Use the slowest logic possible for the function required. Although slower speed devices are becoming more difficult to procure, a best attempt effort is required to prevent use of sub-nanosecond devices for common logic functions.
- Select logic devices with power and ground pins located in the center of the package, with both power and ground pins adjacent to each other.
- Use devices with metal enclosed packaging (oscillators). Ground the metal case or package to the 0V reference with as many low-impedance via connections as possible.
- For devices that contain ceramic packaging and a metal slug on top, provide for a grounded heatsink. Conceptually, this can be incorporated in certain products; however, it may be difficult, if not impossible, to implement.

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