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5

Bypassing and Decoupling

Bypassing and decoupling refers to preventing energy transference from one circuit to another in addition to enhancing the quality of the power distribution system. Three circuit areas are of primary concern: power and ground planes, components, and internal power connections.

Decoupling is a means of overcoming physical and time constraints caused by digital circuitry switching logic states. Digital logic usually involves two possible states, "0" or "1." Some conceptual devices may not be binary but ternary. The setting and detection of these two states is achieved with switches internal to the component that determines whether the device is to be at logic LOW or logic HIGH. There is a finite time period for the device to make this determination. Within this window, a margin of protection is provided to guarantee against false triggering. Moving the logic state near the trigger level creates a degree of uncertainty. If we add high-frequency noise, the degree of uncertainty increases and false triggering may occur.

Decoupling is also required to provide sufficient dynamic voltage and current for proper operation of components during clock or data transitions when all component signal pins switch simultaneously under maximum capacitive load. Decoupling is accomplished by ensuring a low-impedance power source is present in both circuit traces and power planes. Because decoupling capacitors have an increasingly low impedance at high frequencies up to the point of self-resonance, high-frequency noise is effectively diverted from the signal trace, while low-frequency RF energy remains relatively unaffected. Optimal implementation is achieved by using bulk, bypass, and decoupling capacitors. All capacitor values must be calculated for a specific function. In addition, we must properly select the dielectric material of the capacitor and not leave it to random choice from past usage or experience.

Three common uses of capacitors follow. Of course, a capacitor may also be used in other applications such as timing, wave shaping, integration, and filtering.

Decoupling. Removes RF energy injected into the power distribution network from high-frequency components consuming power at the speed the device is switching at. Decoupling capacitors also provides a localized source of DC power for devices and components, and is particularly useful in reducing peak current surges propagated across the board.

Bypassing. Diverts unwanted common-mode RF energy from components or cables. This is essential in creating an AC shunt to remove undesired energy from entering susceptible areas in addition to providing other functions of filtering (bandwidth limiting).

Bulk. Used to maintain constant DC voltage and current to components when all signal pins switch simultaneously under maximum capacitive load. It also prevents power dropout due to *dI/dt* current surges generated by components.

An ideal capacitor has no losses in its conductive plates and dielectric. Current is always present between the two parallel plates. Because of this current, an element of inductance is associated with the parallel plate configuration. Because one plate is charging while its adjacent counterpart is discharging, a mutual coupling factor is added to the overall inductance of the capacitor.

5.1 REVIEW OF RESONANCE

All capacitors consist of an *LCR* circuit where L = inductance related to lead length, R = resistance in the leads, and C = capacitance. A schematic representation of a capacitor is shown in Fig. 5.1. At a calculable frequency, the series combination of L and C becomes resonant, providing very low impedance and effective RF shunting at resonance. At frequencies above self-resonance, the impedance of the capacitor becomes increasingly inductive and bypassing or decoupling becomes less effective. Hence, bypassing and decoupling are affected by the lead-length inductance of the capacitor (including surface mount, radial, or axial styles), the trace length between the capacitor and a components, feed-through pads, and so forth.

Before discussing bypassing and decoupling of circuits on a PCB, a review of resonance is provided. Resonance occurs in a circuit when the reactive value difference between the inductive and capacitive vector is zero. This is equivalent to saying that the circuit is purely resistive in its response to AC voltage. Three types of resonance are common:

- Series resonance
- Parallel resonance
- Parallel C—series RL resonance

Resonant circuits are frequency selective since they pass more or less RF current at certain frequencies than at others. A series *LCR* circuit will pass the selected frequency (as measured across C) if R is high and the source resistance is low. If R is low and the source resistance is high, the circuit will reject the chosen frequency. A parallel resonant circuit placed in series with the load will reject the chosen frequency.

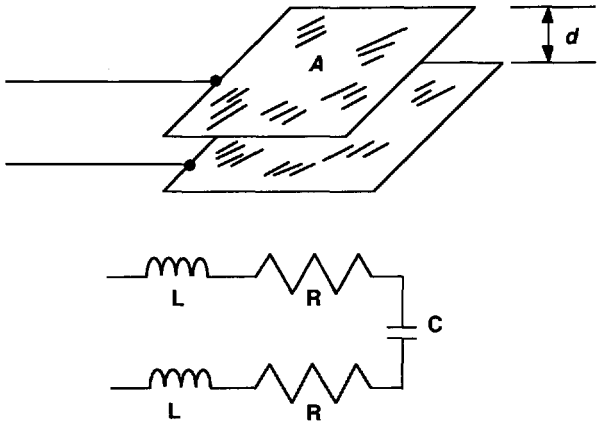


Figure 5.1 Physical characteristics of a capacitor with leads.

5.1.1 Series Resonance

The overall impedance of a series RLC circuit is $Z = \sqrt{R^2 + (X_L - X_c)^2}$. If an RLC circuit is to behave resistively, the value can be calculated as shown in Fig. 5.2 where ω $(2\pi f)$ is known as the *resonant-angular frequency*.

With a series RLC circuit at resonance,

- Impedance is at minimum.
- Impedance equals resistance.
- The phase angle difference is zero.
- Current is at maximum.
- Power transfer (IV) is at maximum.

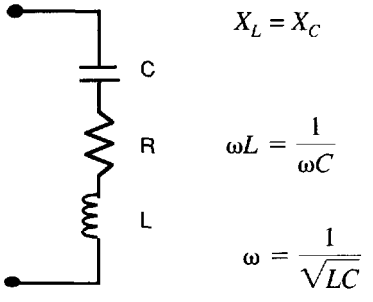


Figure 5.2 Series resonance.

$$\omega = \frac{1}{\sqrt{LC}}$$

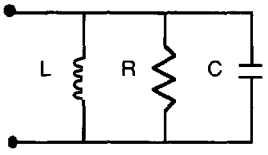


Figure 5.3 Parallel resonance.

5.1.2 Parallel Resonance

A parallel RLC circuit behaves as shown in Fig. 5.3. The resonant frequency is the same as for a series RLC circuit.

With a parallel RLC circuit at resonance,

- Impedance is at maximum.
- Impedance equals resistance.
- The phase angle difference is zero.
- Current is at minimum.
- Power transfer (IV) is at minimum.

5.1.3 Parallel C—Series RL Resonance (Antiresonant Circuit)

Practical resonant circuits generally consist of an inductor and variable capacitor in parallel. Since the inductor will possess some resistance, the equivalent circuit is shown in Fig. 5.4. The resistance in the inductive branch may be a discrete element or the internal resistance of a nonideal inductor.

At resonance, the capacitor and inductor trade the same stored energy on alternate half cycles. When the capacitor discharges, the inductor charges, and vice versa. At the antiresonant frequency, the tank circuit presents a high impedance to the primary circuit current, even though the current within the tank is high. Power is dissipated only in the resistive portion of the network.

The antiresonant circuit is equivalent to a parallel RLC circuit whose resistance is Q^2R.

$$w = \sqrt{\frac{1}{LC} - \left(\frac{R}{L}\right)^2} \approx \frac{1}{\sqrt{LC}} \quad [R << \omega_o L]$$

$$Q = \frac{1}{\omega_o CR} = \frac{X_C}{R} = \frac{X_L}{R}$$

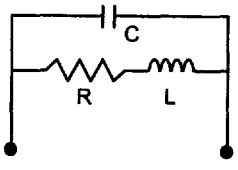


Figure 5.4 Parallel C—series RL resonance.

5.2 PHYSICAL CHARACTERISTICS

5.2.1 Impedance

The equivalent circuit of a capacitor was shown in Fig. 5.1. The impedance of this capacitor is expressed by

$$|Z| = \sqrt{R_s^2 + \left(2\pi fL - \frac{1}{2\pi fC}\right)^2} \tag{5.1}$$

where Z = impedance *(Ω)*
R_s = Equivalent Series Resistance—ESR *(Ω)*
L = Equivalent Series Inductance—ESL *(H)*
C = capacitance *(F)*
f = frequency *(Hz)*

From this equation, $|Z|$ exhibits its minimum value at a resonant frequency f_o such that

$$f_o = \frac{1}{2\pi\sqrt{LC}} \tag{5.2}$$

In reality, the impedance equation (Eq. 5.1) reflects hidden parasitics that are present when we take into account ESL and ESR.

Equivalent Series Resistance (ESR) is a term referring to resistive losses in a capacitor. This loss consists of the distributed plate resistance of the metal electrodes, the contact resistance between internal electrodes, and the external termination points. Note that skin effect at high frequencies increases this resistive value in the leads of the component. Thus, the high-frequency "ESR" is higher in equivalence than DC "ESR."

Equivalent Series Inductance (ESL) is the loss element that must be overcome as current flow is constricted within a device package. The tighter the restriction, the higher the current density and the higher the ESL. The ratio of width to length must be taken into consideration to minimize this parasitic element.

Examining Eq. (5.1), we have a variation of the same equation with ESR and ESL, shown in Eq. (5.3).

$$|Z| = \sqrt{(ESR)^2 + (X_{ESL} - X_C)^2}$$

where $X_{ESL} = 2\pi f\,(\text{ESL})$ (5.3)

$$X_C = \frac{1}{2\pi fC}$$

For certain types of capacitors with regard to dielectric material, the capacitance value varies with temperature and DC bias. Equivalent Series Resistance varies with temperature, DC bias, and frequency, while Equivalent Series Inductance remains fairly unchanged.

For an ideal planar capacitor where current uniformly enters from one side and exits from another side, inductance will be practically zero. For those cases, Z will approach R_s at high frequencies and will not exhibit an inherent resonance, which is exactly what a power and ground plane structure within a PCB does. This is best illustrated by Fig. 5.5.

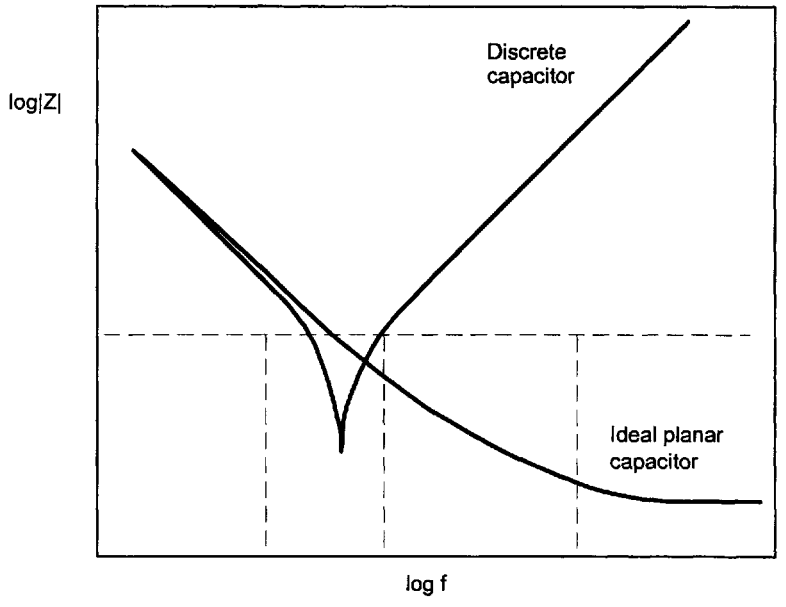


Figure 5.5 Theoretical impedance frequency response of ideal planar capacitors.

The impedance of an "ideal" capacitor decreases with frequency at a rate of −20 dB/decade. Because a capacitor has inductance in its leads, this inductance prevents the capacitor from behaving as desired, described by Eq. (5.2).

> It should be noted that long power traces in two-sided boards that are not laid out for idealized flux cancellation are in effect, extensions of the lead lengths of the capacitor, and this fact seriously alters the self-resonance of the power distribution system.

Above self-resonance, the impedance of the capacitor becomes inductive and increases at +20 dB/decade as detailed in Fig. 5.6. Above the self-resonant frequency, the capacitor ceases to function as a capacitor. The magnitude of ESR is extremely small and, as such, does not significantly affect the self-resonant frequency of the capacitor.

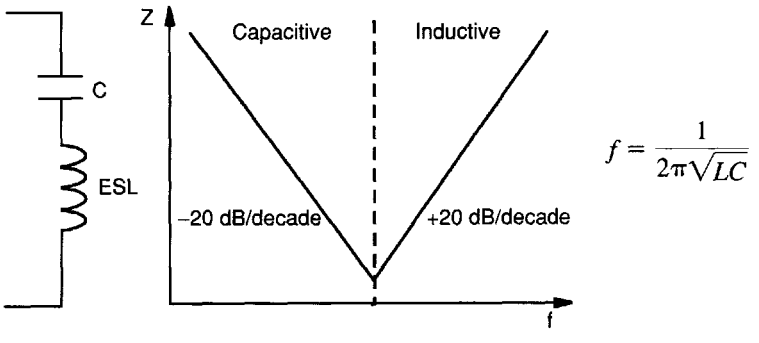


Figure 5.6 Effects of lead-length inductance within a capacitor.

The effectiveness of a capacitor in reducing power distribution noise at a particular frequency of interest is illustrated by Eq. (5.4)

$$\Delta V(f) = |Z(f)| \cdot \Delta I(f) \tag{5.4}$$

where ΔV is the allowed power supply sag; ΔI is the current supplied to the device; and f is the frequency of interest. To optimize the power distribution system by ensuring that noise does not exceed a desired tolerance limit, $|Z|$ must be less than $\Delta V/\Delta I$ for the required current supply. The maximum $|Z|$ should be estimated from the maximum ΔI required. If $\Delta I = 1A$, and $\Delta V = 3.3V$, the impedance of the capacitor must be less than 0.3 Ω.

In order for an ideal capacitor to work as desired, the device should have a high C in order to provide a low impedance at a desired frequency and a low L so that the impedance will not increase at higher frequencies. In addition, the capacitor must have a low R_s to obtain the least possible impedance. For this reason, power and ground planes structures are optimal in providing low-impedance decoupling within a PCB over discrete components.

5.2.2 Energy Storage

Decoupling capacitors ideally should be able to supply all the current necessary during a state transition of a logic device. This is described by Eq. (5.5). Use of decoupling capacitors on two-layer boards also reduces power supply ripple.

$$C = \frac{\Delta I}{\Delta V/\Delta t}$$

$$\text{that is, } \frac{20\ ma}{100\ mv/5\ ns} = 0.001\ \mu f \quad \text{or} \quad 1000\ pf \tag{5.5}$$

where ΔI = current transient
ΔV = allowable power supply voltage change (ripple)
Δt = switching time

Note that for ΔV, EMI requirements are usually more demanding than chip supply needs.

The response of a decoupling capacitor is based on a sudden change in demand for current. It is useful to interpret the frequency domain impedance response in terms of the capacitor's ability to supply current. This charge transfer ability is also for the time domain function that the capacitor is generally selected for. The low-frequency impedance between the power and ground planes indicates how much voltage on the board will change when experiencing a relatively slow transient. This response is an indication of the time-average voltage swing experienced during a faster transient. With low impedance, more current is available to the components under a sudden change in voltage. High-frequency impedance is an indication of how much current the board can initially supply in response to a fast transient. Boards with the lowest impedance above 100 MHz can supply the greatest amount of current (for a given voltage change) during the first few nanoseconds of a sudden transient.

5.2.3 Resonance

When selecting bypass and decoupling capacitors, calculate the charge and discharge frequency of the capacitor based on logic family and clock speed used (self-resonant frequency). One must select a capacitance value based on the reactance that the capacitor presents to the circuit. A capacitor is capacitive up to its self-resonant frequency. Above self-resonance, the capacitor becomes inductive, which minimizes RF decoupling. Table 5.1 illustrates the self-resonant frequency of two types of ceramic capacitors, one with standard 0.25-inch leads and the other surface mount. The self-resonant frequency of SMT capacitors is always higher, although this benefit can be obviated by connection inductance. This higher self-resonant frequency is due to lower lead-length inductance provided by the smaller case package size and lack of long radial or axial lead lengths.

In performing SPICE testing or analysis on various package-size SMT capacitors, all with the same capacitive value, the self-resonant frequency changed by only a few MHz between package sizes, while keeping all other measurement constants unchanged. SMT package sizes of 1210, 0805, and 0603 are common in today's products using various types of dielectric material. Only the lead inductance is different between packaging with capacitance valve remaining constant. The dielectric material did not play a significant part in changing the self-resonant frequency of the capacitor. The change in self-resonant frequency observed between different package sizes, based on lead-length inductance in SMT packaging, was negligible and varied by ± 2–5 MHz.

When actual testing was performed in a laboratory environment on a large sample of capacitors, an interesting phenomenon was observed. The capacitors were self-resonant at the frequency analyzed, as expected. Based on a large sample size, the self-resonant frequency varied considerably. (There were too many plots to detail in this chapter or place within a table.) The self-resonant frequency varied because of the tolerance rating of the capacitor. Because of the manufacturing process, capacitors are provided with a tolerance rating of generally ±10%. More expensive capacitors are in the ± 2–5% range. Since the physical size of the capacitor is fixed, due to the manufacturing process used, the value of capacitance can change owing to the thickness and variation of the dielectric material and other parameters. With manufacturing tolerance for the capacitance part of the component, the actual self-resonant frequency will change based on the tolerance rating of the device. If a design requires an exact value of decoupling, the use of an expensive precision capacitor is required. The resonance equation easily illustrates this tolerance change.

TABLE 5.1 Approximate Self-resonant Frequencies of Capacitors (lead-length dependent)

Capacitor Value	Through-Hole* 0.25″ leads	Surface Mount** (0805)
1.0 μf	2.6 MHz	5 MHz
0.1 μf	8.2 MHz	16 MHz
0.01 μf	26 MHz	50 MHz
1000 pF	82 MHz	159 MHz
500 pF	116 MHz	225 MHz
100 pF	260 MHz	503 MHz
10 pF	821 MHz	1.6 GHz

*For through-hole, L = 3.75 nH (15 nH per/inch).

**For surface mount, L = 1 nH.

Leaded capacitors are nothing more than surface-mount devices with leads attached. A typical leaded capacitor has on the average approximately 2.5 nH of inductance for every 0.10 inch of lead length above the surface of the board. Surface-mount capacitors average 1 nH lead-length inductance.

An inductor does not change resonant response like a capacitor. Instead, the magnitude of impedance changes as the frequency changes. Parasitic capacitance around an inductor can, however, cause parallel resonance and alter response. The higher the frequency of the circuit, the greater the impedance. RF current traveling through an impedance causes an RF voltage. As a result, RF current is created in the device as related to Ohm's law, $V_{rf} = I_{rf} * Z_{rf}$. As examined above, one of the most important design concerns when using capacitors for decoupling lies in lead length inductance. SMT capacitors perform better at higher frequencies than radial or axial capacitors because of lower internal lead inductance. Table 5.2 shows the magnitude of impedance of a 15-nH inductor versus frequency. This inductance value is caused by the lead lengths of the capacitor and the method of placement of the capacitor on a typical PCB.

Figure 5.7 shows the self-resonant frequency of various capacitor values along with different logic families. It is observed that capacitors are capacitive until they approach self-resonance (null point) before going inductive. Above the point where capacitors go inductive, they proportionally cease to function for RF decoupling; however, they may still be the best source of charge for the device, even at frequencies where they are inductive. This is because the internal bond wire from the capacitor's plates to its mounting pad (or pin) must be taken into consideration. Inductance is what causes capacitors to become less useful at frequencies above self-resonance for decoupling purposes.

Certain logic families generate a greater spectrum of RF energy. This energy is generally higher in frequency than the self-resonant frequency range which a decoupling capacitor presents to the circuit. For example, a 0.1 μF capacitor will usually not decouple RF currents for an "ACT or F" logic device, whereas a 0.001 μF capacitor is a more appropriate choice due to the faster edge rate (0.8–2.0 ns minimum) typical of these higher-speed components.

TABLE 5.2 Magnitude of Impedance of a 15-nH Inductor versus Frequency

Frequency (MHz)	Z (ohms)
0.1	0.01
0.5	0.05
1.0	0.10
10.0	1.0
20.0	1.9
30.0	2.8
40.0	3.8
50.0	4.7
60.0	5.7
70.0	6.6
80.0	7.5
90.0	8.5
100.0	9.4

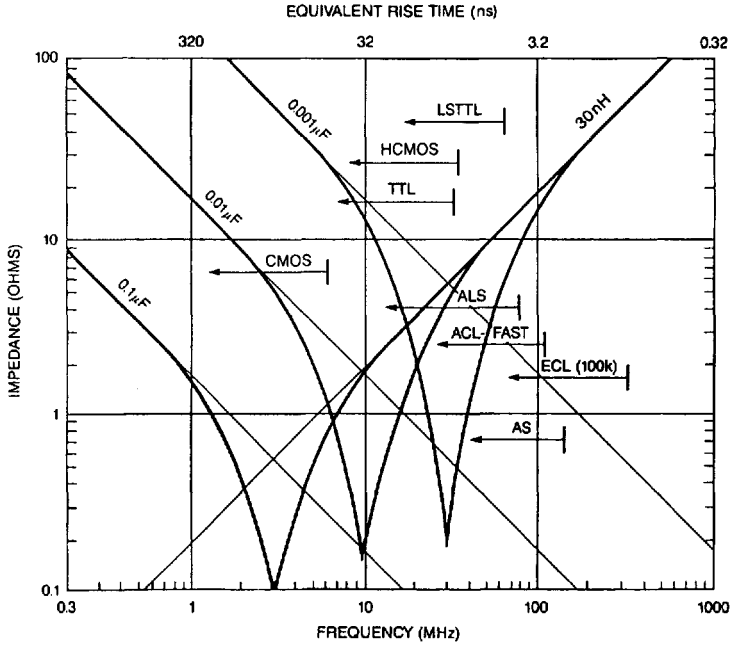


Figure 5.7 Self-resonant frequency of capacitors versus logic families. Capacitors provided with 30-nH series inductance (trace plus lead length). (Source: H. Ott, *Noise Reduction Techniques in Electronic Systems*. Copyright © 1988 John Wiley & Sons, reprinted with permission)

We now compare the difference between through-hole and surface-mount capacitors (SMT). Since SMT devices have much less lead-length inductance, the self-resonant frequency is higher than through-hole. Figure 5.8 illustrates a plot of the self-resonant frequency of various values of ceramic capacitors. All capacitors in the figure have the same lead-length inductance for comparison purposes.

Effective capacitive decoupling is achieved when capacitors are properly placed on the PCB. Random placement or excessive use of capacitors is a waste of material. Sometimes fewer capacitors strategically placed perform best for decoupling. In certain applications, two capacitors in parallel are required to provide greater spectral bandwidth of RF suppression. These parallel capacitors must differ by two orders of magnitude or value (e.g., 0.1 and 0.001 μF) or 100x for optimal performance. Use of parallel capacitors are discussed later in this chapter.

5.2.4 Benefits of Power and Ground Planes

A benefit of using multilayer PCBs is the placement of the power and ground planes adjacent to each other. The physical relationship of these two planes creates one large decoupling capacitor. This capacitor usually provides adequate decoupling for low-speed (slow edge rate) designs; however, additional layers add significant cost to the PCB. If components have signal edges (t_r or t_f) slower than 10 ns (e.g., standard TTL logic), use of high-

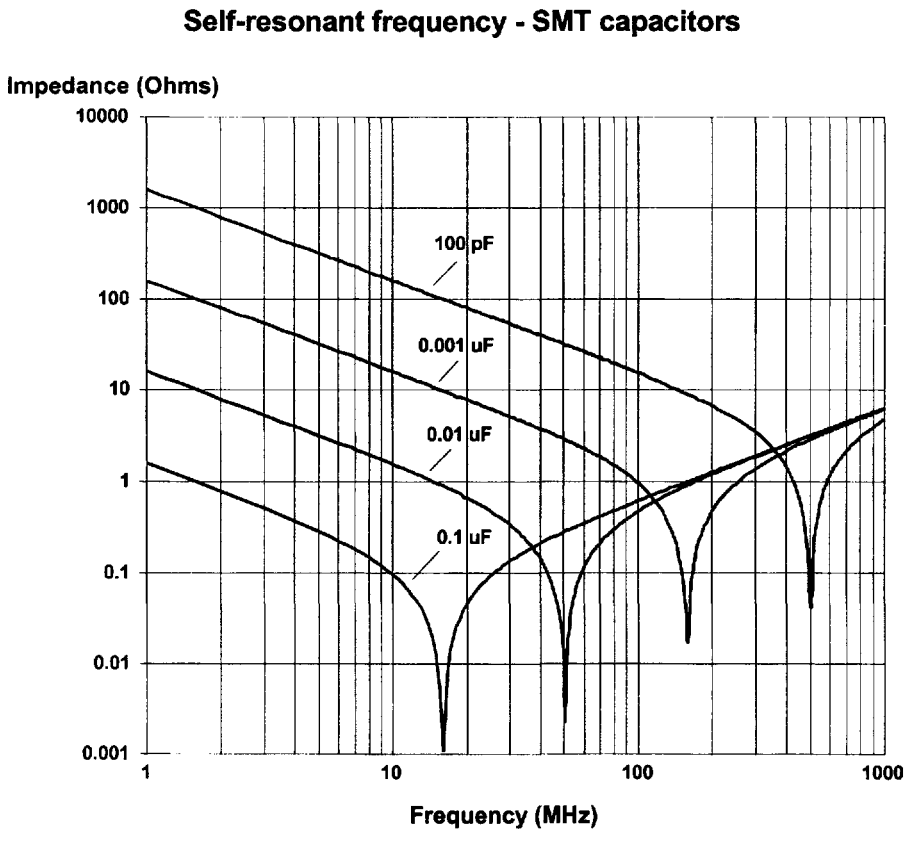


Figure 5.8 Self-resonant frequency of SMT capacitors. (ESL = 1nH)

performance, high self-resonant frequency decoupling capacitors is generally not required. Bulk capacitors are still needed, however, to maintain proper voltage levels. For performance reasons values such as 0.1 μF to 10 μF are appropriate for device power pins.

Another factor to consider when using power and ground planes as a primary decoupling capacitor is the self-resonant frequency of this built-in capacitor. If the self-resonant frequency of the power and ground planes is the same as the self-resonant frequency of the lumped total of the decoupling capacitors installed on the board, there will be a sharp resonance where these two frequencies meet. No longer will there be a wide spectral distribution of decoupling. If a clock harmonic is at the same frequency as this sharp resonance, the board will act as if little decoupling exists. When this situation occurs, the PCB may become an unintentional radiator with possible noncompliance with EMI requirements. Should this occur, additional decoupling capacitors (with a different self-resonant frequency) will be required to shift the resonance of the PCB's power and ground planes.

One simple method to change the self-resonant frequency of the power and ground planes is to change the distance spacing between these planes. Increasing or decreasing

the height separation or relocation within the layer stackup will change the capacitance value of the assembly. Equations (5.7) and (5.8) provide this calculation. One disadvantage of using this technique is that the impedance of the signal routing layers may also change, which is a performance concern. Many multilayer PCBs generally have a self-resonant frequency between 200 and 400 MHz.

In the past, slower speed logic devices fell well below the spectrum of the self-resonant frequency of the PCB's power and ground planes. Logic devices used in newer, high-technology designs approach or exceed this critical resonant frequency. When both the impedance of the power planes and the decoupling capacitors approach the same resonant frequency, severe performance deterioration occurs. This degraded high-frequency impedance will result in serious EMI problems. Basically, the assembled PCB becomes an unintentional transmitter. The PCB is not really the transmitter; rather, the highly repetitive circuits or clocks are the cause of RF energy. Decoupling will not solve this type of problem (due to the resonance of the decoupling), requiring system-level containment measures to be employed.

5.3 CAPACITORS IN PARALLEL

It is common practice during a product design to make provisions for parallel decoupling of capacitors with the intent of providing greater spectral distribution of performance and minimizing ground bounce. Ground bounce is one cause of EMI created within a PCB. When parallel decoupling is provided, one must not forget that a third capacitor exists—the power and ground plane structure.

When DC power is consumed by components switching, a momentary surge occurs in the power distribution network. Decoupling provides a localized point source charge since a finite inductance exists within the power supply network. By keeping the voltage level at a stable reference point, false logic switching is prevented. Decoupling capacitors also minimize radiated emissions by providing a very small loop area for creating high spectral content switching currents instead of having a larger loop area created between the component and a remote power source.

Research on the effectiveness of multiple decoupling capacitors shows that parallel decoupling may not be significantly effective and that at high frequencies, only a 6-dB improvement may occur over the use of a single large-value capacitor.[1] Although 6-dB appears to be a small number for suppression of RF current, it may be all that is required to bring a noncompliant product into compliance with international EMI specifications. According to Paul,

> Above the self-resonant frequency of the larger value capacitor where its impedance increases with frequency (inductive), the impedance of the smaller capacitor is decreasing (capacitive). At some point, the impedance of the smaller value capacitor will be smaller than that of the larger value capacitor and will dominate thereby giving a smaller net impedance than that of the larger value capacitor alone.

[1]Clayton, Paul, "Effectiveness of Multiple Decoupling Capacitors," *IEEE Transactions on Electromagnetic Compatibility*, May 1992, vol. EMC-34, pp. 130–133.

This 6-dB improvement is basically the result of lower lead and device-body inductance provided by the capacitors in parallel. There are now two sets of parallel leads from the internal plates of the capacitors. These two sets provide greater trace width than would be available if only one set of leads were provided. With a wider trace width, there is less lead-length inductance. This reduced lead-length inductance is a significant reason why parallel decoupling capacitors work as well as they do.

Figure 5.9 shows a plot of two bypass capacitors, 0.01 μF and 100 pF, both individually and in parallel. The 0.01 μF capacitor has a self-resonant frequency at 14.85 MHz. The 100 pF capacitor has its self-resonant frequency at 148.5 MHz. At 110 MHz, there is a large increase in impedance due to the parallel combination. The 0.01 μF capacitor is inductive, while the 100 pF capacitor is still capacitive. We have both L and C in resonance—hence, an antiresonant frequency point, which is exactly what we do not want in a PCB if compliance to EMI requirements is mandatory.

> Between the self-resonant frequency of the larger value capacitor, 0.01 μF, and the self-resonant frequency of the smaller value capacitor, 100 pF, the impedance of the larger value capacitor is essentially inductive, whereas the impedance of the smaller value capacitor is capacitive. In this frequency range there exists a parallel resonant LC circuit and we should therefore expect to find an infinite impedance of the parallel combination. Around this resonant point, the impedance of the parallel combination is actually larger than the impedance of either isolated capacitor! [4, p.132]

In Fig. 5.9, observe that at 500 MHz, the impedances of the individual capacitors are virtually identical. The parallel impedance is only 6-dB lower. This 6-dB improvement is only valid over a limited frequency range from about 120 to 160 MHz.

To further examine what occurs when two capacitors are used in parallel, we look at a Bode plot of the impedance presented by two capacitors in parallel (see Fig. 5.10).

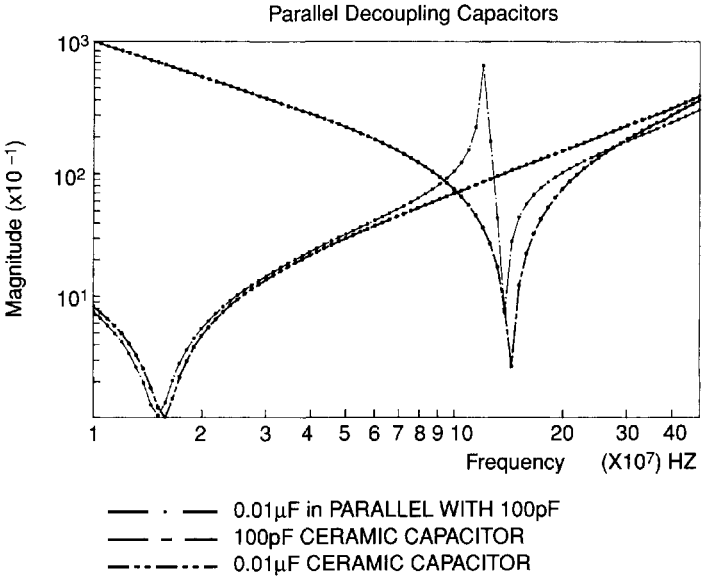


Figure 5.9 Resonance of parallel capacitors.

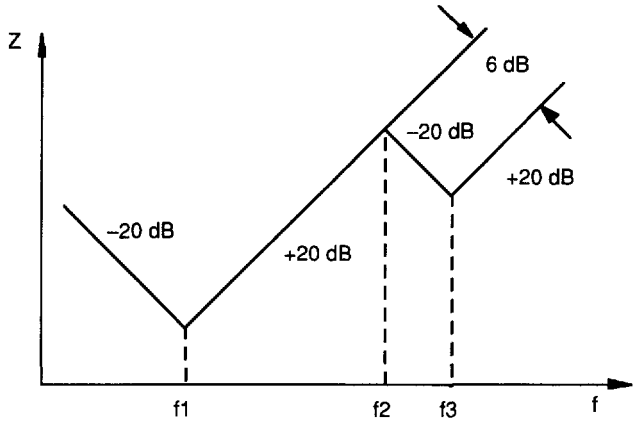


Figure 5.10 Bode plot of parallel capacitors.

For the bode plot of Fig. 5.10, the frequency responses of the magnitude at the various break frequencies are [4]

$$f_1 = \frac{1}{2\pi\sqrt{LC_1}} < f_2 = \frac{1}{2\pi\sqrt{LC_2}} < f_3 = \frac{1}{2\pi\sqrt{LC_3}} = 2f_2 \tag{5.6}$$

By shortening the lead-lengths of the larger value capacitor (0.01 μF), we can obtain the same results by a factor of 2. For this reason a single capacitor may be more optimal in a specific design than two, especially if minimal lead-length inductance exists.

To remove RF current generated by components switching all signal pins simultaneously (and it is desired to parallel decouple), it is common practice to place two capacitors in parallel (e.g., 0.1 μF and 0.001 μF) immediately adjacent to each power pin. If parallel decoupling is used within a PCB layout, one must be aware that the capacitance values should differ by two orders of magnitude, or 100x. The total capacitance of parallel capacitors is not important. Parallel reactance provided by the parallel capacitors (due to self-resonant frequency) is the important item. (See Tables 5.1 and 5.2.)

To optimize the effects of parallel bypassing and to allow use of only one capacitor, reduction in capacitor lead length inductance is required. A finite amount of lead length inductance will always exist when installing the capacitor on the PCB. Note that the lead length must also include the length of the via connecting the capacitor to the planes. The shorter the lead length from either single or parallel decoupling, the greater the performance. In addition, some manufacturers provide capacitors with significantly reduced "body" inductance internal to the capacitor.

5.4 POWER AND GROUND PLANE CAPACITANCE

The effects of the internal power and ground planes inside the PCB are not considered in Fig. 5.9. However, multiple bypassing effects are illustrated in Fig. 5.11. Power and ground planes have very little lead-length inductance equivalence and no ESR (Equiva-

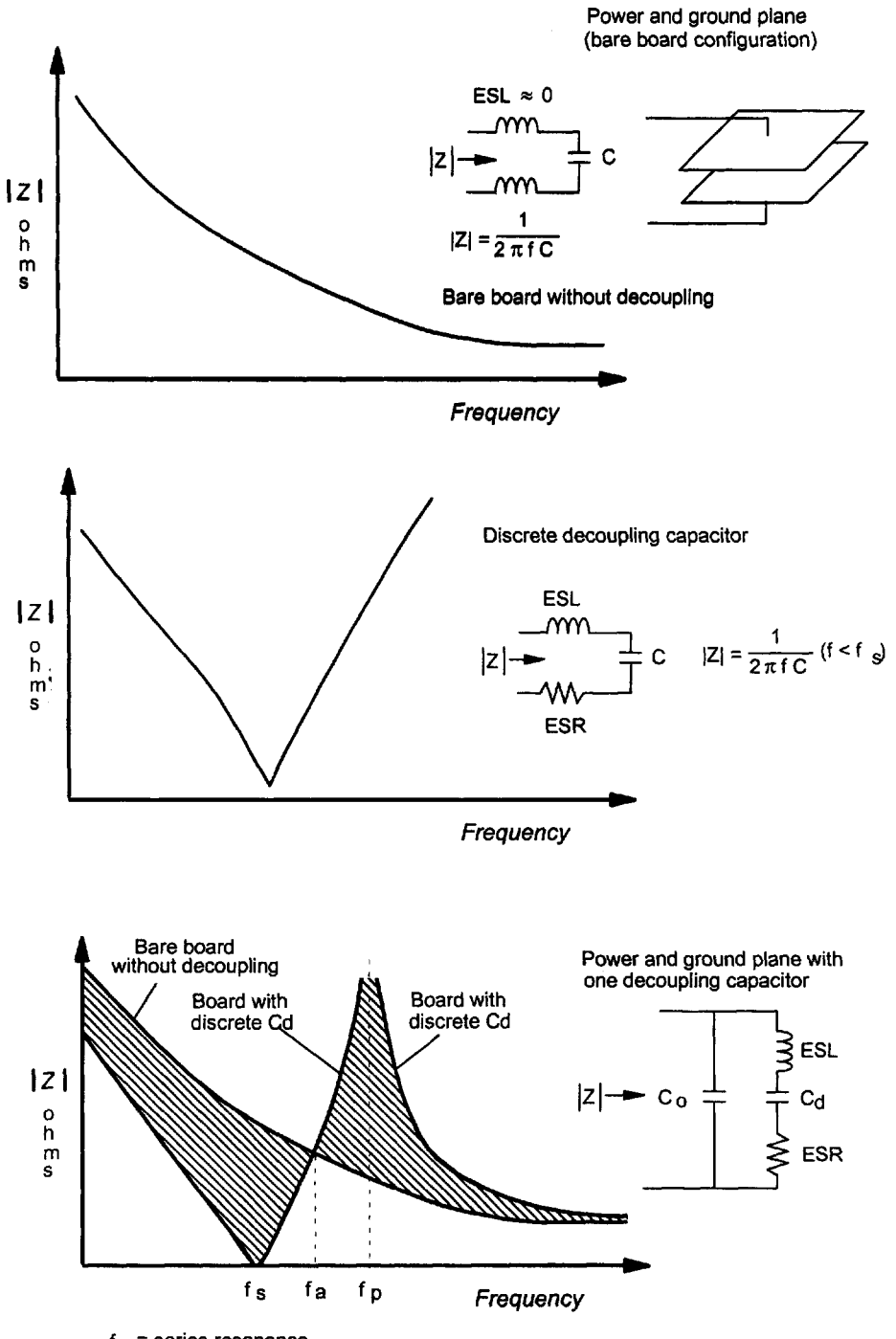


Figure 5.11 Decoupling effects of power and ground planes with discrete capacitors.

lent Series Resistance). Use of power planes as a decoupling capacitor reduces RF energy at frequencies generally in the higher frequency ranges.

On most multilayer boards, the maximum inductance of the planes between two components is significantly less than 1 nH. Conversely, lead-length inductance (e.g., the inductance associated with the traces connecting a component to its respective via plus the via themselves) is typically 2.5–10 nH or greater [8].

Capacitance will always be present between a voltage and ground plane pair. Depending on thickness of the core, the dielectric constant, and the placement of the planes within the board stackup, various values of internal capacitance can exist. Network analysis, mathematical calculations or modeling will reveal the actual capacitance of the power planes. This is in addition to determining the impedance of all circuit planes and the self-resonant frequency of the total assembly as potential RF radiators. This value of capacitance is easily estimated by Eqs. (5.7) and (5.8). This approximation may be used just to *estimate* the capacitance between planes since planes are finite, have multiple holes, vias, and the like. Actual capacitance is generally less than the calculated value.

$$C = \frac{\varepsilon_o \varepsilon_r A}{d} = \frac{\varepsilon A}{d} \tag{5.7}$$

where ε = permittivity of the medium between capacitor plates *(F/m)*
A = area of the parallel plates *(m^2)*
d = separation of the plates *(m)*
C = capacitance between the power and ground plane*s (pF)*

Introducing relative permittivity ε_r of the dielectric material, and the value of the permittivity of free space, ε_o, we obtain the capacitance of the parallel-plate capacitor, namely, the power and ground plane combination.

$$C = 8.85 \frac{A\,\varepsilon_r}{d}\,(pF) \tag{5.8}$$

where ε_r = is the relative permittivity of the medium between the plates, typically ≈ 4.5 (varies for linear material, usually between 1 and 10)
and ε_o = permittivity of free space, $1/36\pi * 10^{-9}$ F/m = $8.85 * 10^{-12}$ F/m = 8.85 pF/m

Equations (5.7) and (5.8) show that the power and ground planes, when separated by 0.01 inch of FR-4 material, will have a capacitance of 100 pF/in^2.

Because discrete decoupling capacitors are common in multilayer PCBs, we must question the value of these capacitors when low-frequency, slow edge rate components are provided, generally in the frequency range below 25 MHz. Research into the effects of power and ground planes along with discrete capacitors reveals interesting results [6].

In Fig. 5.11, the impedance of the "bare board" closely approximates the ideal decoupling impedance that would result if only pure capacitance free of interconnect inductance and resistance could be added. This ideal impedance is given by $Z_c = 1/j\omega C_o$. The discrete capacitor becomes zero at the series resonant frequency, f_s, and infinite at the parallel resonance frequency, f_p, where n = number of discrete capacitors provided, C_d is the discrete capacitor, and C_o is the capacitance of the power and ground plane structure, conditioned by the source impedance of the power supply [6].

$$f_s = \frac{1}{2\pi\sqrt{LC}} \qquad f_p = f_s\sqrt{1 + \frac{nC_d}{C_o}} \tag{5.9}$$

For frequencies below the series resonance frequency, discrete decoupling capacitors behave as capacitors with an impedance of $Z = 1/j\omega C$. For frequencies near the series resonance frequency, the impedance of the loaded PCB is actually less than that of the ideal PCB. However, at frequencies above f_s, the decoupling capacitors begin to exhibit inductive behavior as a result of their associated interconnect inductance. Thus, the discrete decoupling capacitors function as inductors at frequencies above their series resonance frequency. The frequency at which the magnitude of the board impedance is the same with or without the decoupling capacitors (where the unloaded PCB intersects that of the loaded, nonideal PCB) is [6]

$$f_a = f_s\sqrt{1 + (nC_d / 2C_o)} \tag{5.10}$$

For frequencies above f_a, the additional number of "n" decoupling capacitors provides no additional benefit (as long as the switching frequencies of the components are within the decoupling range of the power and ground plane structure) since the bare board impedance remains far below that of the board that is loaded with discrete capacitors. At frequencies near the loaded board pole (parallel resonant) frequency, the magnitude of the loaded board impedance is extremely high, and the decoupling performance of the loaded board is far worse than that of the unloaded board (without additional decoupling capacitor). The analysis clearly indicates that minimizing the series inductance of the decoupling capacitor connection is crucial to achieving ideal capacitor behavior over the widest possible frequency range, which in the time domain corresponds to the ability to supply charge rapidly. Lowering the interconnect inductance increases the series and parallel-resonance frequency, thereby extending the range of ideal capacitor behavior [6].

Parallel resonances correspond to poles in the board impedance expression. Series resonances are null points. When multiple capacitors are provided, the poles and zeros will alternate so that there will be exactly one parallel resonance between each pair of series resonances. A parallel resonance will always exist between two series resonances.

Although good distributive capacitance exists when using a power and ground plane structure, adjacent close stacking of these two planes plays a critical part in the overall PCB assembly. If two sets of power and ground planes exist, for example, +5V/ground and +3.3V/ground, both with different dielectric spacing between the two planes, it is possible to have multiple decoupling capacitors built internal to the board. With proper selection of layer stackup, both high-frequency and low-frequency decoupling can be achieved without use of any discrete capacitors. To expand on this concept, a technology known as buried capacitance is finding use in extremely high-technology products that require high-frequency decoupling.

5.4.1 Buried Capacitance

Buried capacitance™ is a patented manufacturing process in which the power and ground planes are separated by a 0.001 inch (0.25 mm) dielectric.[2] With this small dielectric spacing, decoupling is effective up to 200–300 MHz. Above this frequency range, use

[2]Buried capacitance is a registered trademark of HADCO Corporation (which purchased Zycon Corporation, developers of this technology).

of discrete capacitors is required to decouple components that operate above the cutoff frequency of the buried capacitance. The important item to remember is that the closer the distance spacing is between the power and ground planes, the better the decoupling performance. It is to be remembered that, although buried capacitors may eliminate the employment and cost of discrete components, use of this technology may far exceed the cost of all discrete components that were removed.

To better understand the concept of buried capacitance, we should consider the power and ground planes as pure capacitance at low frequencies with very little inductance. These planes can be considered to be an equal-potential surface with no voltage gradient except for a small DC voltage drop. This capacitance is calculated simply as area divided by thickness times permittivity. For a 10-inch square board, with 2 mil FR-4 dielectric between the power and ground planes, we have 45 nF (0.045 μF).

At some frequency, a full wave will be observed between the power and ground planes along the edge length of the PCB. Assuming velocity of propagation to be 6 in/ns (15.24 cm/ns), we observe that the frequency will be 600 MHz for a 10 × 10 inch board. At this frequency, the planes are not at equal potential, for the voltage measured between two points can differ greatly as we move the test probe around the board. A reasonable transition frequency is one-tenth of 600 MHz or 60 MHz. Below this frequency, the planes can be considered as pure capacitance.

Knowing the velocity of propagation and capacitance per square area, we can calculate the plane inductance. For a 2-mil-thick dielectric, capacitance is 0.45 nF/inch^2, velocity of propagation = 6 inch/ns, and inductance is 0.062 nH/square. This inductance is a spreading inductance, similar in interpretation to spreading resistance, and is a very small number. This small number is the primary reason why power planes are mainly pure capacitance.

With inductance and capacitance, we calculate the impedance as $Z_o = \sqrt{L/C}$, which is 0.372 ohms-inch. A plane wave traveling down a long length of a 10-inch-wide board will see 0.372/10 = 0.0372 ohms impedance, again, a small number.

Decoupling capacitance is increased because the distance spacing between the planes *(d)* is in the denominator. Inductance is decreased because the velocity of propagation must remain constant and the total impedance is also decreased. The power and ground planes are the means of distributing power. Reducing the dielectric thickness is effective at increasing high-frequency decoupling capacitance and transporting high-frequency power through a lower impedance distribution system.

5.4.2 Calculating Power and Ground Plane Capacitance

Capacitance between a power and ground plane is described by

$$C_{pp} = k\frac{\varepsilon_r A}{d} \tag{5.11}$$

where C_{pp} = capacitance of parallel plates (pF)
ε_r = relative dielectric constant of the board material (vacuum = 1, FR4 material = 4.1 to 4.7)
A = common area between the parallel plates (square inches or cm)
d = distance spacing between the plates (inches or cm)
k = conversion constant (0.2249 for inches, 0.884 for cm)

One caveat in implementing this technology is that the inductance caused by the antipads (holes for through-vias) in the power and ground planes can minimize the theoretical effectiveness of this technique.

Because of the efficiency of the power planes as a decoupling capacitor, the use of high self-resonant frequency decoupling capacitors may not be required for standard TTL or slow-speed logic. This optimum efficiency exists, however, only when the power planes are closely spaced—less than 0.01 inch with 0.005 inch preferred for high-speed applications. If additional decoupling capacitors are not properly chosen, the power planes will go inductive below the lower cut-in range of the higher self-resonant frequency decoupling capacitor. With this gap in resonance, a pole is generated, causing undesirable effects on RF suppression. At this point, RF suppression techniques on the PCB become ineffective, and containment measures must be used at a much greater expense.

5.5 LEAD-LENGTH INDUCTANCE

All capacitors have lead and device body inductance. Vias also add to this inductance value. Lead inductance must be minimized at all times. When a signal trace plus lead-length inductance is combined, a higher impedance mismatch will be present between the component's ground pin and the system ground plane. With trace impedance mismatch, a voltage gradient is created between these two sources, creating RF currents. RF fields cause RF emissions on PCBs; hence, decoupling capacitors must be designed for minimum inductive lead length, including via and pin escapes (or pad connections from the component pin to the point where the device pin connects to a via).

In a capacitor, the dielectric material determines the magnitude of the zero for the self-resonant frequency of operation. All dielectric material is temperature sensitive. The capacitance value of the capacitor will change in relation to the ambient temperature provided to its case package. At certain temperatures, the capacitance may change substantially and may result in improper performance, or no performance at all when used as a bypass or decoupling element. The more temperature stable the dielectric material, the better performance of the capacitor.

In addition to the sensitivity of the dielectric material to temperature, the equivalent series inductance (ESL) and the equivalent series resistance (ESR) must be low at the desired frequency of operation. ESL acts like a parasitic inductor, whereas ESR acts like a parasitic resistor, both in series with the capacitor. ESL is not a major factor in today's small SMT capacitors. Radial and axial lead devices will always have large ESL values. Together, ESL and ESR degrade a capacitor's effectiveness as a bypass element. When selecting a capacitor, one should choose a capacitor family that publishes actual ESL and ESR values in their data sheet. Random selection of a standard capacitor may result in improper performance if ESL and ESR are too high. Most vendors of capacitors do not publish ESL and ESR values, so it is best to be aware of this selection parameter when choosing capacitors used in high-speed, high-technology PCBs.

Because surface-mount capacitors have essentially little ESL and ESR, their use is preferred over radial or axial types. Typically, ESL is <1.0 nH, and ESR should be 0.5 ohms or less. For decoupling capacitors, capacitance tolerance is not as important as the temperature stability, dielectric constant, ESL, ESR, and self-resonant frequency [1].

5.6 PLACEMENT

5.6.1 Power Planes

Multilayer PCBs generally contain one or more pairs of voltage and ground planes. Power planes function as a low-inductance capacitor that constrains RF currents generated from components and traces. Multiple chassis ground stitch connections to all ground planes minimizes voltage gradients between board and chassis and between/among board layers. These gradients also are a major source of common-mode RF fields. This is in addition to sourcing RF currents to chassis ground. In many cases, multiple ground stitch connections are not always possible, especially in card cage designs. In such situations, care must be taken to analyze and determine where RF loops will occur and how to optimize grounding of the power planes.

Power planes that are positioned next to ground planes provide for flux cancellation in addition to decoupling RF currents created from power fluctuations of components and noise injected into the power and ground planes. Components switching logic states cause a current surge during the transition. This current surge places a strain on the power distribution network. An image plane is a solid copper plane at voltage or ground potential located adjacent to a signal routing plane. RF currents generated by traces on the signal plane will mirror image themselves in this adjacent metal plane. This metal plane must not be isolated from the power distribution network [9]. To remove common-mode RF currents created within a PCB, all routing (signal) layers must be physically adjacent to the image plane. (Refer to Chapter 4 for a detailed discussion of image planes.)

5.6.2 Decoupling Capacitors

Before determining where to locate decoupling capacitors, the physical structure of a PCB must be understood. Figure 5.12 shows the electrical equivalent circuit of a PCB. In this figure, observe the loops that exist between power and ground caused by traces, IC wire bonds, lead frames of components, socket pins, component interconnect leads, and decoupling capacitor. The key to effective decoupling is to minimize R_2, L_2, R'_2, L'_2, R_3, L_3, R'_3, L'_3, R_4, L_4, R'_4, and L'_4. Placement of power and ground pins in the center of the component helps reduce R_4, L_4, R'_4, and L'_4. Basically, the impedance of the PCB structure must be minimized. The easiest way to minimize the resistive and inductive components of the PCB is to provide a solid plane. To minimize the inductance from the component, use of SMT, ball grid arrays, and flip chips is preferred. With less lead bond lengths from die to PCB pad, overall impedance is reduced.

Figure 5.12 [1] makes clear that EMI is a function of loop geometry and frequency, hence, the smallest closed-loop area is desired. We acquire this small area by placing a local decoupling capacitor, C_{pcb}, for current storage adjacent to the power pins of the IC. It is mandatory that the decoupling loop impedance be much lower than the rest of the power distribution system. This low impedance will cause the high-frequency RF energy developed by both traces and components to remain almost entirely within this small closed loop. As a result, low EMI emissions are observed.

If the impedance of the loop is smaller than the rest of the system, some fraction of the high-frequency RF component will transfer or couple to the larger loop formed by the power distribution system. With this situation, RF currents are developed and, hence, higher EMI emissions. This situation is best illustrated in Fig. 5.13.

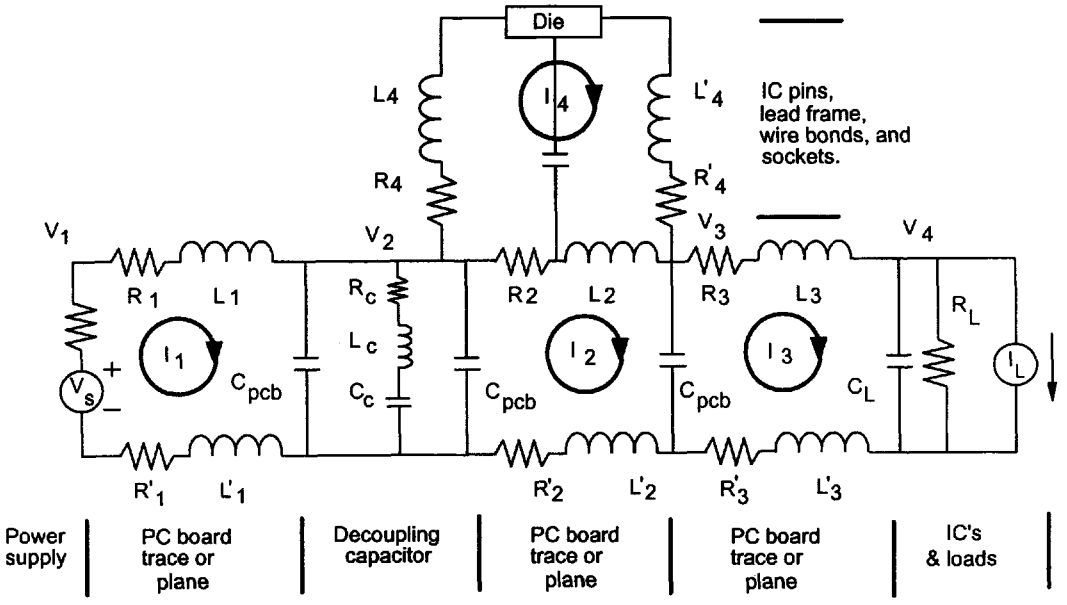


Figure 5.12 Equivalent circuit of a PCB.

To summarize,

The important parameter when using decoupling capacitors is to minimize lead-length inductance and to locate the capacitors as close as possible to the component.

Decoupling capacitors must be provided for every device with edges faster than 2 ns and should be provided, placement wise, for "every component." Making provisions for decoupling capacitors is a necessity because future EMI testing may indicate a requirement for these devices. During testing, it may be possible to determine that there may be excess capacitors in the assembly. Having to add capacitors to an assembled board is difficult, if not impossible. Today, CMOS, ECL, and other fast logic families require additional decoupling capacitors besides the power and ground plane structure.

If a decoupling capacitor must be provided to a through-hole device after assembly, retrofit can be performed. Several manufacturers provide a decoupling capacitor assembly using a flat, level construction that resides between the component and PCB. This flat

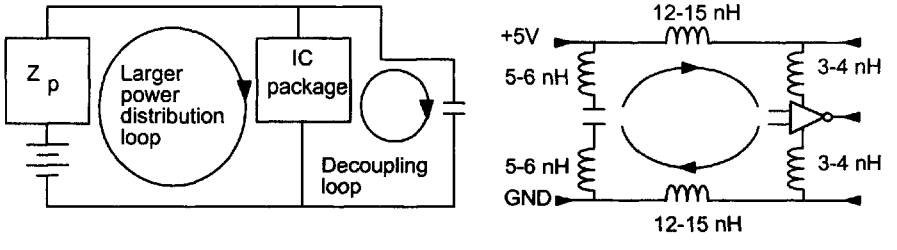


Figure 5.13 Power distribution model for loop control.

pack shares the same power and ground pins of the components. Because these capacitors are flat in construction, lead-length inductance is much less compared to capacitors with radial or axial leads. Since the capacitor and component share the same power and ground pins, R_2, L_2, R'_2 and L'_2 are also reduced. Some lead-length inductance will remain, which cannot be removed. The most widely used board level retrofit capacitors are known as Micro-Q™.[3] Other manufacturers provide similar products. An example of this type of capacitor is detailed in Fig. 5.14. Other configurations exist in pin grid array (PGA) form factor. For PGA retrofit decoupling capacitors, unique assemblies are available based on the particular pinout configuration of the device requiring this part.

A retrofit capacitor has a self-resonant frequency generally in the range of 10–50 MHz, depending on the capacitance of the device. Since DIP style leads are provided, higher frequency use cannot occur owing to excessive lead-length inductance. Although sometimes termed a "retrofit" device, the improved decoupling performance of these capacitors, compared to axial leaded capacitors on two-layer boards, makes them suitable for initial design implementation.

Poor planning during PCB layout and component selection may require use of Micro-Q devices. As yet, there is no equivalent retrofit for SMT packaged components.

When selecting a capacitor, we should consider not only the self-resonant frequency but the dielectric material as well. The most commonly used material is Z5U (barium titanite ceramic). This material has a high dielectric constant. This constant allows small capacitors to have large capacitance values with self-resonant frequencies from 1 MHz to 20 MHz, depending on design and construction. Above self-resonance, performance of Z5U decreases as the loss factor of the dielectric becomes dominant, which limits its usefulness to approximately 50 MHz.

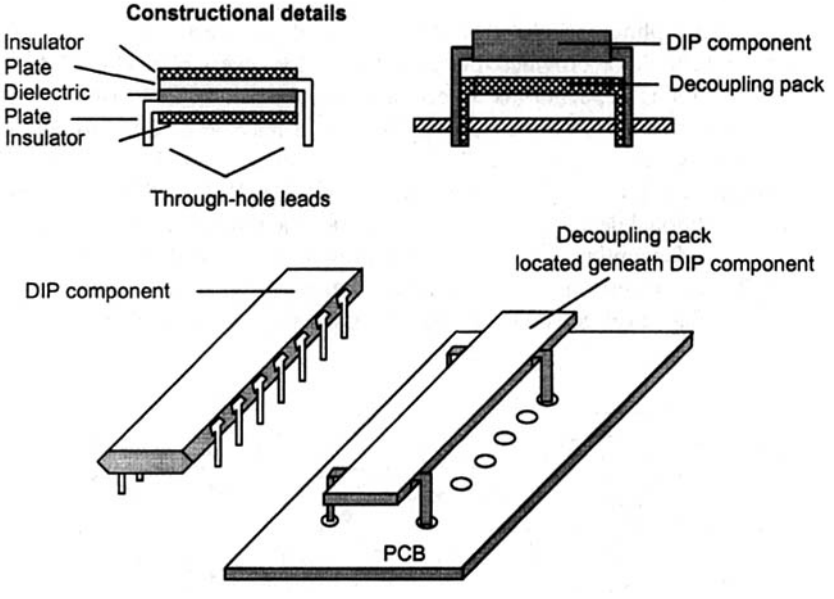


Figure 5.14 Retrofit decoupling capacitor—DIP mounting style.

[3]™ Micro-Q is a trademark of Circuit Components Inc. (formerly Rogers Corporation).

Another dielectric material commonly used is NPO (strontium titanite). This material has better high-frequency performance owing to a low dielectric constant. NPO is also a more temperature-stable dielectric. The capacitance value (and self-resonant frequency) is less likely to change when the capacitor is subjected to changes in ambient temperature or operating conditions.

Placement of 1 nF (1000 pF) capacitors (capacitors with a very high self-resonant frequency) on a 1-inch center grid throughout the PCB may provide additional protection from reflections and RF currents generated by both signal traces and the power planes, especially if a high-density PCB stackup is used [7]. It's not the exact location that counts in the placement of these additional decoupling capacitors. A lumped model analysis of the PCB will show that the capacitors will still function as needed, regardless of where the device is actually placed for overall decoupling performance. Depending on the resonant structure of the board, values of the capacitors placed in the grid may be as small as 30 to 40 pF [7].

VLSI and high-speed components (e.g., F, ACT, BCT, CMOS, ECL logic families) may require decoupling capacitors in parallel. As slew rates of components become steeper, a greater spectral distribution of RF currents is created. Parallel capacitors generally provide optimal bypassing of power plane noise, in addition to removing high-frequency RF energy. Multiple paired sets of capacitors are placed between the power and ground pins of VLSI components located around all four sides. These high-frequency decoupling capacitors are typically rated 0.1 μF in parallel with 0.001 μF for 50-MHz systems. Higher clock frequencies use a parallel combination of 0.01 μF and 100 pF components.

While the focus in this chapter is on multilayer boards, single- and double-sided boards also require decoupling. Figure 5.15 illustrates correct and incorrect ways of locating decoupling capacitors for a single- or double-sided assembly. When placing decoupling capacitors, ground loop control must be considered at all times. When using multilayer boards with internal power and ground planes, placement of the decoupling capacitor may be anywhere in the vicinity of the component's power pins [6], although this implementation may actually cause the PCB to become more RF active. This requirement is based on whether the component has its mounting pins via straight down to the power/ground plane, or whether a routed trace connects to the discrete capacitor. Location of the capacitor is not critical during placement for the previous statement because of the lumped distributed capacitance of the power planes and because the components themselves must via down to the power and ground plane—the same as the decoupling capacitor [6].

Another function of a decoupling capacitor is to provide localized energy storage, thereby reducing power supply radiating loops. When current flows in a closed-loop circuit, the RF energy produced is proportional to IAF, where I is the current in the loop, A is the area of the loop, and F is the frequency of the current. Because current and frequency are predetermined by the type of logic family selected, it becomes necessary to minimize the area of the logic current loop to reduce radiation. Minimal loop area can be accomplished by taking care in placement of decoupling capacitors. A good example of a large loop area is shown in Fig. 5.15.

In Fig. 5.15, V_{gnd} is LdI/dt induced noise in the ground trace flowing in the decoupling capacitor. This V_{gnd} now drives the ground structure of the board and contributes to the overall common-mode voltage across the entire board. One should minimize the ground path that is common with the board's ground structure and the decoupling capacitor.

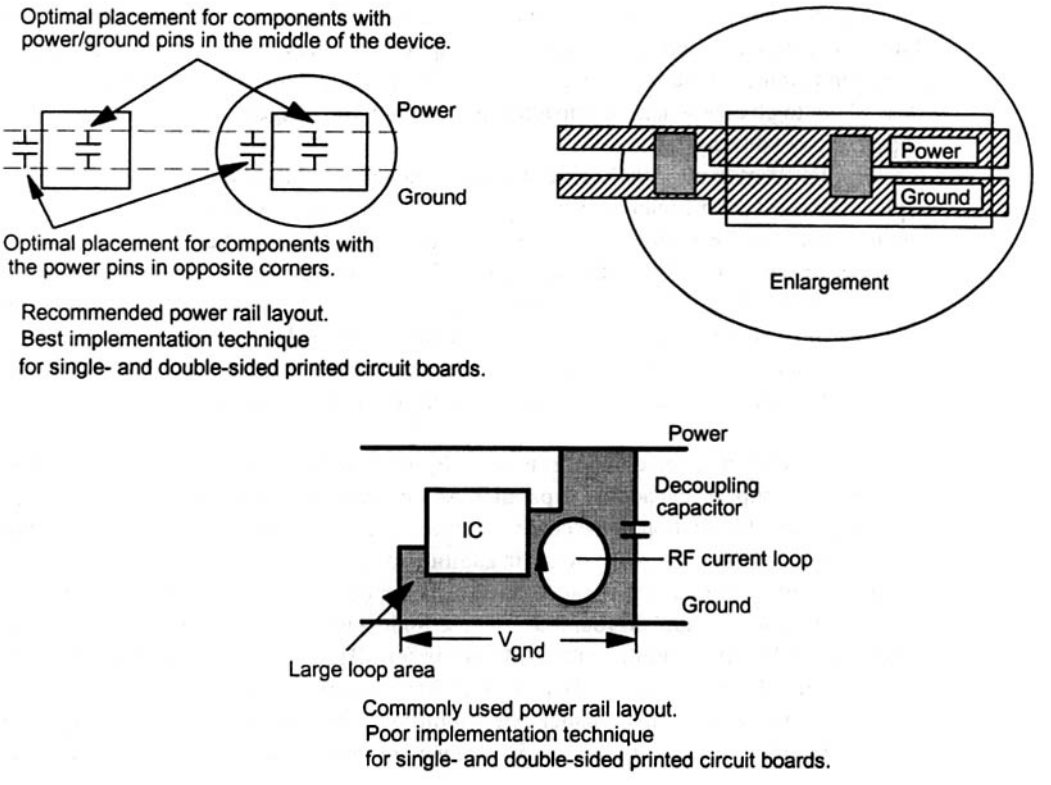


Figure 5.15 Placement of decoupling capacitors—two-layer board.

5.7 SELECTION OF A DECOUPLING CAPACITOR

Clock circuit components must be given emphasis to be RF decoupled. This is due to the switching energy generated by the component injected into the power and ground distribution system. This energy will be transferred to other circuits or subsections as common-mode or differential-mode RF. Bulk capacitors such as tantalum and high-frequency ceramic monolithic are both required, each for a different application. Furthermore, monolithic capacitors must have a self-resonant frequency higher than the clock harmonics requiring suppression. Typically, one selects a capacitor with a self-resonant frequency in the range of 10–30 MHz for circuits, with edge rates of 2 ns or less. Many PCBs are self-resonant in the 200–400 MHz range. Proper selection of decoupling capacitors, along with the self-resonant frequency of the PCB structure (acting as one large capacitor), will provide enhanced EMI suppression. Tables 5.1 and 5.2 are useful for axial or radial lead capacitors. Surface-mount devices have a much higher self-resonant frequency by approximately two orders of magnitude (or 100x) as the result of less lead-length inductance. Aluminum electrolytic capacitors are ineffective for high-frequency decoupling and are best suited for power supply subsystems or power line filtering.

It is common to select a decoupling capacitor for a particular application, usually the first harmonic of a clock or processor. Sometimes, a capacitor is selected for the third

or fifth harmonic since this is where the majority of RF current is produced. There also needs to be plenty of larger discrete capacitors, bulk and decoupling. The use of common decoupling capacitor values of 0.1 μF in parallel with 0.001 μF can be too inductive and too slow to supply charge current at frequencies above 200–300 MHz.

When performing component placement on a PCB, one should make provisions for adequate high-frequency RF decoupling. One should also verify that all bypass and decoupling capacitor chosen are selected based on intended application. This is especially true for clock generation circuits. The self-resonant frequency must take into account all significant clock harmonics requiring suppression, generally considered to be the fifth harmonic of the original clock frequency. Finally, capacitive reactance (self-resonant reactance in ohms) of decoupling capacitors is calculated per Eq. (5.12).

$$X_c = \frac{1}{2\pi f C} \tag{5.12}$$

where X_c = capacitance reactance (ohms)
f = resonant frequency (Hertz)
C = capacitance value

5.7.1 Calculating Capacitor Values (Wave-Shaping)

Capacitors can also be used to wave-shape differential-mode RF currents on individual traces. These parts are generally used in I/O circuits and connectors and are rarely used in clock networks. The decoupling capacitor, C, alters the signal edge of the output clock line (slew rate) by rounding the time period the signal edge takes to transition from logic state 0 to logic state 1. This is illustrated in Fig. 5.16.

In examining Fig. 5.16, we should observe the change in the slew rate (clock edge) of the desired signal. Although the transition points remain unchanged, the time period t_r and t_f is different. This elongation or slowing down of the signal edge is a result of the capacitor charging and discharging. The change in transition time is described by the equations and illustration presented in Fig. 5.17. Note that a Thevenin equivalent circuit is shown without the load. The source voltage, V_b, and series impedance are internal to the driver or clock generation circuit. The capacitive effect on the trace, seen in the figure, is a result of this capacitor being located in the circuit. To determine the time rate of change of the capacitor detailed in Fig. 5.16, the equations in Fig. 5.17 are used.

When a Fourier analysis is performed on this signal edge (conversion from time to frequency domain), a significant reduction of RF energy is observed along with a decrease in spectral RF distribution. Hence, there is improved EMI compliance. Caution is required during the design stage to ensure that slower edges will not adversely affect functional operational performance.

The capacitive value for a decoupling capacitor can be calculated in two ways. Although the capacitance is calculated for optimal filtering at a particular resonant frequency, use and implementation depend on installation, lead length, trace length, and other parasitic parameters that may change the resonant frequency of the capacitor. The installed value of capacitive reactance is the item of interest. Calculating the value of capacitance will be in the ballpark and is generally accurate enough for actual implementation.

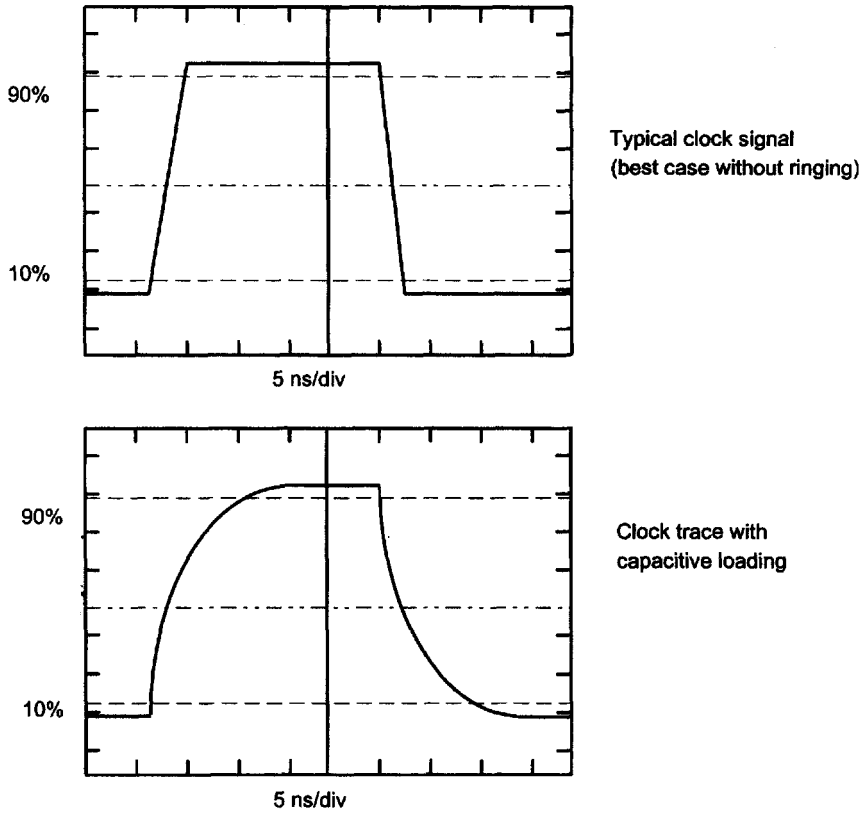


Figure 5.16 Capacitive effects on clock signals.

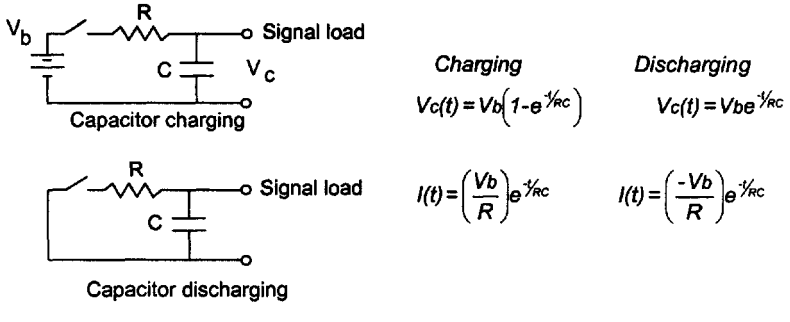
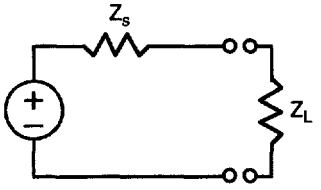


Figure 5.17 Capacitor equations.

Before calculating a decoupling capacitor value, the Thevenin impedance of the network should be determined. This impedance value should be equal to these two resistors values placed in parallel. Using a Thevenin equivalent circuit, we assume $Z_s = 150\ \Omega$ and $Z_L = 2.0\ \text{k}\Omega$.

$$Z_t = \frac{Z_s * Z_L}{Z_s + Z_L} = \frac{150 * 2000}{2150} = 140\Omega \tag{5.13}$$



Method 1. Equation (5.14) is used to determine the capacitance value knowing the edge rate of the clock signal.

$$t_r = kR_tC_{\max} = 3.3 * R_t * C_{\max}$$
$$C_{\max} = \frac{0.3\,t_r}{R_t} \tag{5.14}$$

where t_r = edge rate of the signal (the faster of either the rising or falling edge)
R_t = total resistance within the network
$C_{\max}$ = maximum capacitance value to be used
k = single time constant

Note: C in nanofarads if t_r is in nanoseconds
C in picofarads if t_r is in picoseconds

The capacitor must be chosen so that $t_r = 3.3 * R * C$ equals an acceptable rise or fall time for proper functionality of the signal; otherwise baseline shift may occur. Baseline shift refers to the steady-state voltage level that is identified as logic low or logic high for a particular logic family. The number 3.3 is based on the value for the time constant of a capacitor charging based on the equation $\tau = RC$. Approximately three (3) time constants equals one (1) rise time. Since we are interested in only one time constant for calculating capacitance value, this value of k is $1/3t_r$, which becomes 3.3 when incorporated within the equation.

For example, if the edge rate is 5 ns and the impedance of the circuit is 140 Ω, we can calculate the maximum value of C as

$$C_{\max} = \frac{0.3 * 5}{140} = 0.01\ nF \quad \text{or} \quad 10\ pF \tag{5.15}$$

A 60-MHz clock with a period of 8.33 ns on and 8.33 ns off, $R = 33\ \Omega$ (typical for an unterminated TTL part) has an acceptable $t_r = t_f = 2$ ns (25% of the on or off value). Therefore,

$$\left(C = \frac{0.3 * t_r}{R_t}\right) \qquad C = \frac{0.3(2 * 10^{-9})}{33} = 18\ pF \tag{5.16}$$

Method 2

- Determine highest frequency to be filtered, $f_{\max}$.
- For differential pair traces, determine the maximum tolerable value of each capacitor to minimize signal distortion. Use Eq. (5.17).

$$C_{\min} = \frac{100}{f_{\max} * R_t}$$

$$\frac{1}{2\pi f_{\max} * \frac{C}{2}} \geq 3 * R_t \tag{5.17}$$

where C is in nanofarads and f in MHz.

To filter a 20-MHz signal with $R_L = 140\ \Omega$, the capacitance value would be

$$C_{\min} = \frac{100}{20 * 140} = 0.036\ nF \quad \text{or} \quad 36\ pF \tag{5.18}$$

with negligible source impedance, Z_c.

When using bypassing capacitors, the following should be implemented:

- If degradation of the edge rate is acceptable (generally three times the value of C), increase the capacitance value to the next highest standard value.
- Select a capacitor with proper voltage rating and dielectric constant for intended use.
- Select a capacitor with a tight tolerance level. A tolerance level of +80/–0% is acceptable for power supply filtering but is inappropriate as a decoupling capacitor for high-speed signals.
- Install the capacitor with minimal lead-length and trace inductance.
- Verify that the functionally of the circuit so that it still works with the capacitor installed. Too large a value capacitor can cause excessive signal degradation.

5.8 SELECTION OF BULK CAPACITORS

Bulk capacitors provide DC voltage and current to components when the devices are switching all data, address, and control signals simultaneously under maximum capacitive load. Switching components tend to cause current fluctuations within the power distribution network. These fluctuations can cause improper performance of components owing to voltage sags. Bulk capacitors provide energy storage for circuits to maintain optimal voltage and surge current requirements.

Bulk capacitors (usually tantalum dielectric) are often used in addition to higher self-resonant frequency decoupling capacitors to provide DC power for components and power plane RF modulation. One bulk capacitor should be placed for every two LSI and VLSI components in addition to the decoupling capacitors at the following locations:

- Power entry connector from the power supply to the PCB.
- Power terminals on I/O connectors for daughter or adapter cards, peripheral devices, and secondary circuits.
- Adjacent to power-consuming circuits and components.

- The furthest location from the input power connectors.
- High-density component placement remote from the DC input power connector.
- Adjacent to clock generation circuits and ripple sensitive devices.

When using bulk capacitors, the voltage rating should be calculated that the nominal voltage equals 50% of the capacitor's actual voltage rating requirement to prevent the capacitor from self-destruction if a voltage surge occurs. For example, with power at 5V, a capacitor with a minimum 10V rating should be used.

Table 5.3 shows the typical number of capacitors required for some popular logic families. This table is based on the maximum allowable power drop, which is equal to 25% of the noise immunity level of the circuit being decoupled. Note that for standard CMOS logic, this table is conservative since the trace wiring to the components cannot provide the required peak current without excessive voltage drop. The actual value of the capacitor used will be determined based on functional application.

Memory arrays require additional bulk capacitors owing to the extra current required for proper operation during a refresh cycle. The same is true for VLSI components with high pin counts. High-density pin grid array (PGA) modules also must have additional bulk capacitors provided, especially when all signal, address, and control pins switch simultaneously under maximum capacitive load.

Using Eq. (5.5) to calculate the peak surge current consumed by many capacitors, we observe that more is not necessarily better. An excessive number of capacitors could draw a large amount of current, which places a strain on the power supply.

Selection of a capacitor based on past experience with slower speed digital logic will generally not provide proper bypassing and decoupling when used with high-technology, high-speed designs. Consideration of resonance, placement on the PCB, lead-length inductance, existence of power planes, and the like must all be included when selecting a capacitor or capacitor combination.

For bulk capacitors, the following procedures are provided to determine optimal selection [2].

TABLE 5.3 Number of Decoupling Capacitors for Selected Logic Families

	Peak Transient Current Requirement (mA)		
Logic Family	Gate Overcurrent (mA)	1 Gate Drive (mA)	Number of Decoupling Capacitors for a Fanout of 5 Gates + 10 cm Trace Length
CMOS	1	0.3	1.0
TTL	16	1.7	2.6
LS-TTL	8	2.5	2.0
HCMOS	15	5.5	1.2
STTL	30	5	1.8
FAST	15	5.5	1.8
ECL	1	1.2	1.0

Source: Controlling Radiated Emissions by Design. Reprinted by permission, Van Nostrand Reinhold.

Method 1

1. Determine maximum current *(ΔI)* consumption anticipated on the board. Assume all gates switch simultaneously. Include the effect of power surges by logic crossover (cross-conduction currents).
2. Calculate maximum amount of power supply noise permitted *(ΔV)*. Factor in a safety margin.
3. Determine maximum common-path impedance acceptable to the circuit.

$$Z_{cm} = \Delta V/\Delta I \tag{5.19}$$

4. If solid planes are used, allocate the impedance, Z_{cm}, to the connection between power and ground.
5. Calculate the impedance of the interconnect cable, L_{cable}, from the power supply to the board. Add this value to Z_{cm} to determine the frequency below which the power supply wiring is adequate ($Z_{\text{total}} = Z_{cm} + L_{\text{cable}}$).

$$f = \frac{Z_{\text{total}}}{2\,\pi\,L_{\text{cable}}} \tag{5.20}$$

6. If the switching frequency is below the calculated f of Eq. (5.20), the power supply wiring is fine. Above f, bulk capacitors, C_{bulk}, are required. Calculate the value of the bulk capacitor for an impedance Z_{total} at frequency f.

$$C_{\text{bulk}} = \frac{1}{2\,\pi f Z_{\text{total}}} \tag{5.21}$$

Method 2. A PCB has 200 CMOS gates (G), each switching 5 pF (C) loads within a 2-ns time period. Power supply inductance is 80 nH.

$$\Delta I = GC\frac{\Delta V}{\Delta t} = 200(5\,pF)\frac{5\text{V}}{2\text{ ns}} = 2.5\,A \text{ (worst case peak surge)}$$

$$\Delta V = 0.200\,V \text{ (from noise margin budget)}$$

$$Z_{\text{total}} = \frac{\Delta V}{\Delta I} = \frac{0.20}{2.5} = 0.08\,\Omega \tag{5.22}$$

$$L_{\text{cable}} = 80\text{ nH}$$

$$f_{ps} = \frac{Z_{\text{total}}}{2\,\pi\,L_{\text{cable}}} = \frac{0.08\,\Omega}{2\,\pi\,80\text{ nH}} = 159\text{ kHz}$$

$$C = \frac{1}{2\,\pi f_{ps} Z_{\text{total}}} = 12.5\,\mu\text{F}$$

Capacitors commonly found on PCBs for bulk purposes are generally in the range of 10–100 μF.

Capacitance required for decoupling power plane RF currents due to the switching energy of components can be determined by knowing the resonant frequency of the logic circuits to be decoupled. The hardest part in calculating this resonant value is knowing the inductance of the capacitor's leads (ESL). If ESL is not known, an impedance meter or

network analyzer may be used to measure the ESL value. The drawback of using an impedance meter is that low-frequency instruments may not catch higher frequency responses. ESL can be also approximated by knowing only the capacitance value and the self-resonant frequency parasitics.

5.9 DESIGNING A CAPACITOR INTERNAL TO A COMPONENT'S PACKAGE

Technology has progressed to the point where the majority of radiated emissions need not be caused by poor PCB layout, trace routing, impedance mismatches, or power supply corruption. Radiated emissions are the result of using digital components. What do we mean by the statement that digital components are the primary source of RF energy? The answer is simple. RF energy is produced by the Fourier spectra created by the switching transistors internal to the silicon wafer which is physically glued down inside a protective enclosure. This enclosure is commonly identified as the package, which consists of either plastic or ceramic material.

Recent advances in integrated circuit (IC) components such as microprocessors, digital signal processors, and applications-specific integrated circuits (ASICs) have become significant sources of electromagnetic noise. In recent years, clock rates have increased from 25 and 33 MHz to 200 through 500 MHz and beyond. With these clock rates, we have a resulting corresponding internal dynamic power dissipation increase due to switching currents that may exceed 10 watts within a VLSI device.

The silicon die demands current from a power distribution network and must drive a transmission line at certain levels of voltage and current. In addition, technology has progressed to the point where millions of transistors are provided within a single die on a wafer. Manufacturing technology has also approached the 0.18-micron line width, which allows for faster edge rate devices and die shrink. Die shrink is where the number of individual components on a silicon wafer increase, thus improving the yield and total number of devices from a single process batch. The cost of the product decreases when an increase in the number of functional units occurs. Because of smaller line widths, the propagation delay between the individual gates within the component package becomes shorter, along with corresponding faster edge rates. The faster the edge rate, the greater the ability of the device to create radiated emissions. With faster internal edges, the switching effects can cause greater losses across the inductance internal to the package.

With faster edge rates, DC current is demanded from the power distribution network at a quicker rate. This faster switching speed bounces the power distribution network, creating an imbalance in the differential-mode current between power and ground. With an imbalance in the differential-mode, common-mode currents are produced. Common-mode currents are observed during EMI tests radiating from cable assemblies, interconnects, or PCB components.

To address component-level problems, EMC engineers and component manufacturers must advance state-of-the-art principles in implementing suppression techniques for ICs, especially decoupling. Design and cost margins also play an important part in determining how an EMC solution will be implemented.

As presented earlier, decoupling capacitors provide an instantaneous point source of charge to a component for the time period that the device switches. A decoupling capacitor

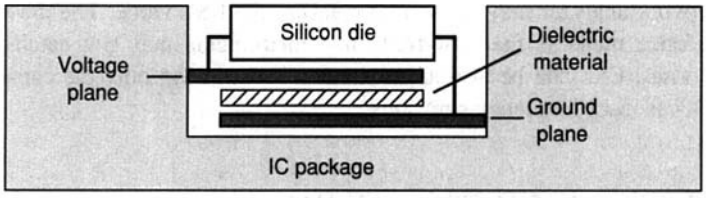


Figure 5.18 Decoupling capacitor internal to a silicon package.

must not only provide a voltage charge to the device at the speed that the device is switching at, but it must also recharge quickly. The self-resonant value of the capacitor depends on various parameters, which include not only the capacitance value but also ESL and ESR.

A component vendor can use various techniques to implement a decoupling capacitor internal to the component package. One approach is to implement a built-in decoupling capacitor before affixing the silicon die into the package, as illustrated in Fig. 5.18.

Two layers of metal film, separated by a thin layer of a dielectric material, will form a high-quality parallel plate capacitor. Since the applied voltage is extremely low, the dielectric layer can be very thin. This thin dielectric results in adequate capacitance for a very small area. The effective lead length approaches zero. The resonant frequency of the parallel plate configuration will thus be very high. The cost to manufacturers to implement this technique will be minimal compared to the overall cost of the IC. In addition to improved performance, the overall PCB cost may be reduced because use of discrete decoupling capacitors may not be required.

Another technique that will provide decoupling within a component package is by brute force. High-density, high-technology components often feature SMT capacitors located directly inside the device package. The use of discrete components is common in multichip modules. Depending on the inrush peak current surge of the silicon die, an appropriate capacitor is selected based on the current charge the device requires, in addition to providing decoupling of differential-mode currents at the self-resonant frequency of the component. Even with this internal capacitor, additional externally located discrete capacitors may be required. An example of how a discrete capacitor is provided in these modules is shown in Fig. 5.19.

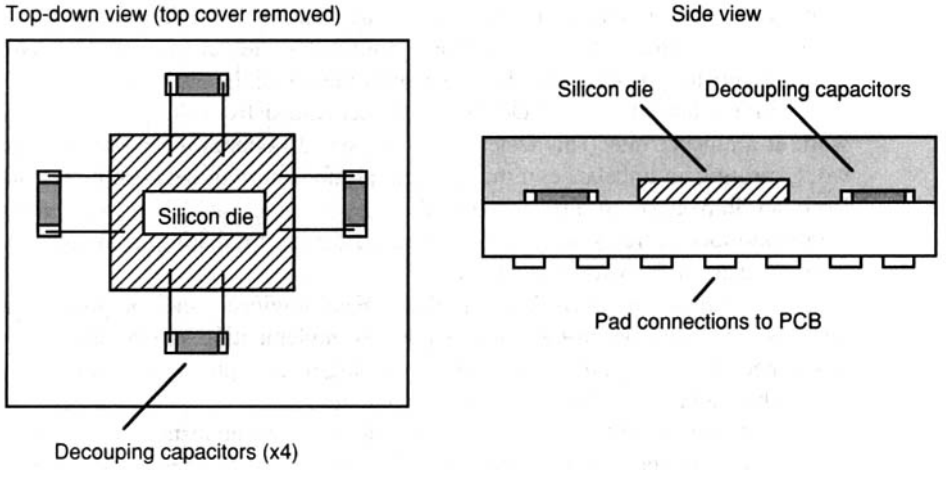


Figure 5.19 Locating decoupling capacitors internal to multichip module packaging.

For a synchronous design, CMOS power dissipation is a capacitive discharge effect. A device that consumes 2400 mW at 3.6V, running at 100 MHz, has an effective load capacitance of approximately 2000 pF, generally observed right after a clock event. If we allow a 10% drop in voltage, this means we require 20 nF of bulk capacitance for optimal performance. A gate capacitance of 6 to 7 $\mu F/m^2$ provides an area of approximately 3 square millimeters. This dimension is huge for a high density component. In addition, the capacitive value is not very large.

CMOS gates provide distributed capacitance by their input capacitance, both by coupling to the supply rails of the devices driving them and by the series capacitance of their own input transistors. This internal capacitance does not come close to the required value for functional operation. Silicon dies do not permit the extra silicon available to be used for bulk capacitance (floor space), since deep submicron designs consume routing space and are required to support the oxide layers of the assembly.

5.10 VIAS AND THEIR EFFECTS IN SOLID POWER PLANES

Use of vias in solid power planes will decrease the total capacitance based on the number of vias and the amount of real estate that has been etched out from the planes. A capacitor works by virtue of energy storage that is contained within a metallic structure. With less metal (copper plane), the current density distribution is decreased. As a result, less area exists to support the number of electrons that create the current density distribution. Figure 5.20 illustrates the value of capacitance between parallel power planes in two configurations: solid power planes and power planes with 30% of the area removed by vias and clearance pads.

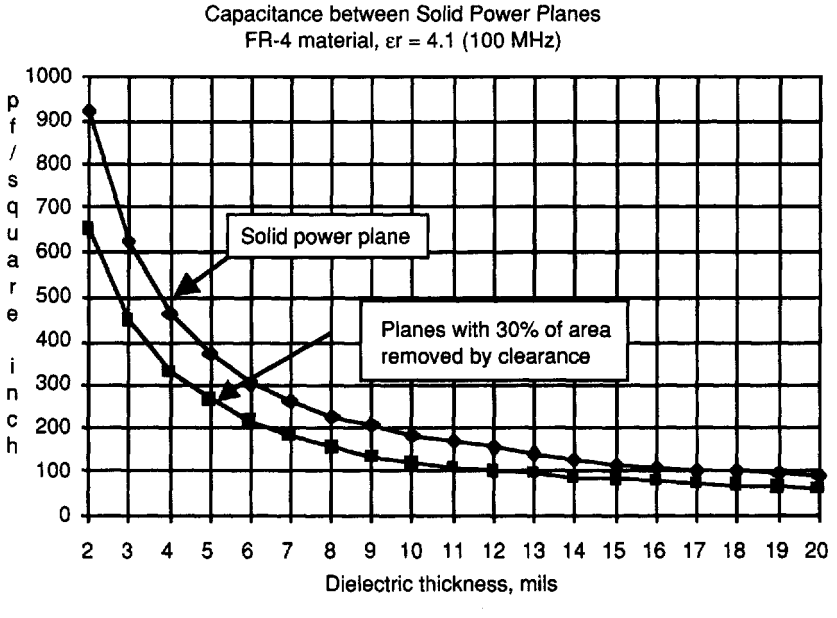


Figure 5.20 Effects of vias in power and ground planes.

REFERENCES

[1] Montrose, M. 1996. *Printed Circuit Board Design Techniques for EMC Compliance*. Piscataway, NJ: IEEE Press.

[2] Johnson, H. W., and M. Graham. 1993. *High Speed Digital Design*. Englewood Cliffs, NJ: Prentice Hall.

[3] Ott, H. 1988. *Noise Reduction Techniques in Electronic Systems*. 2nd ed. New York: John Wiley & Sons.

[4] Paul, C. R. 1992. "Effectiveness of Multiple Decoupling Capacitors," *IEEE Transactions on Electromagnetic Compatibility*, May, vol. EMC-34, pp. 130–133.

[5] Mardiguian, M. 1992. *Controlling Radiated Emissions by Design*. New York: Van Nostrand Reinhold.

[6] Drewniak, J. L., T. H. Hubing, T. P. Van Doren, and D. M. Hockanson. 1995. "Power Bus Decoupling on Multilayer Printed Circuit Boards." *IEEE Transactions on EMC* 37(2): 155–166.

[7] Montrose, M. 1991. "Overview on Design Techniques for PCB Layout Used in High Technology Products." *Proceedings of the IEEE International Symposium on Electromagnetic Compatibility*, 61–66.

[8] Van Doren, T., J. Drewniak, and T. Hubing. 1992. "Printed Circuit Board Response to the Addition of Decoupling Capacitors," Tech. Rep. TR92-4-007, UMR EMC Lab. (September 30).

[9] Montrose, M. 1996. "Analysis on the Effectiveness of Image Planes Within a Printed Circuit Board." *Proceedings of the IEEE International Symposium on Electromagnetic Compatibility*, 326–331.