CURRENT EFFICIENT, LOW VOLTAGE, LOW DROPOUT REGULATORS

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LOW DROP-OUT REGULATORS

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LOW DROP-OUT REGULATORS

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For the hopes of

peaceful coexistence and universal brotherhood !

FOREWORD

The research focuses on the realization of current efficient, low voltage, low drop-out regulators. These characteristics are driven by portable and battery operated products requiring compactness and low power. The approach adopted is to develop circuit techniques that allow maximum use of current existing process technologies. As a result, future and more advanced technologies will have even greater benefits. The dissertation is organized to reflect the necessary sequence of events that lead up to the complete design of a system.

Chapter 1 introduces low drop-out regulators. Their definition and motivation for existence are addressed here. The alternative, or in some cases the supplement, type of regulator is compared to further elucidate the demand of low drop-out regulators in today's market. A typical circuit architecture is illustrated along with a description of the basic characteristics inherent to the system and required by the loading circuits. Lastly, the chapter concludes by identifying and defining the objective of the research.

Chapter 2 discusses the considerations necessary to successfully design the circuits. The loading requirements, which partially determine the frequency response of the control loop, are identified. Their implications on circuit limitations and challenges are illustrated. This is followed by a transient analysis describing the typical response of the system along with the difficulties imposed by low voltage and low quiescent current flow. Finally, the specific circuit implications and requirements of the major blocks of the system are discussed, i.e., the pass device, the error amplifier, and the reference circuit.

A literature survey of the different prevailing topologies for low drop-out regulators is illustrated in chapter 3. The circuit realization of each topology is discussed. The circuits highlighted are realized in relatively inexpensive technologies to constrain the research orientation to generalized circuit techniques and not towards manipulation of the processes. The main concepts are emphasized and evaluated for their appropriateness in a low voltage and low quiescent current atmosphere. Furthermore, circuit enhancement techniques are also studied to show the different ways that the system can be amended to yield improved performance on particular specification parameters.

Techniques that allow proper and practical realization of low drop-out regulators at low input voltages and low quiescent current flow are developed in chapter 4. The motivation and challenges are identified. The areas highlighted include current efficiency, current boosting, and load regulation enhancement. The advantages and the drawbacks of the circuits used to realize these concepts are discussed within the context of a low voltage environment.

Chapter 5 shows the development of a low voltage and curvature corrected bandgap reference. The development starts at the conceptual roots of zener references and first order bandgaps and continues on to curvature corrected references. Respective output structures are discussed and evaluated for their propriety in the system at hand. The chapter then illustrates the different curvature correcting schemes and concludes with the most suitable for the system.

The concepts developed in chapters 4 and 5 are used to design the actual circuit blocks. These circuits are described and illustrated in chapter 6. They include the composite pass device, the gain stage of the amplifier, the buffer stage of the amplifier, and the curvature corrected bandgap reference. The pass device is developed to reap the

benefits of current boosting. The amplifier is designed to take advantage of the current efficiency and the load regulation enhancement concepts discussed in chapter 4. Lastly, the design of the reference reflects the concepts cultivated in chapter 5. The chapter ends with a discussion of the trimming requirements of the bandgap reference.

All the circuit blocks designed in chapter 6 are used to realize the system in chapter 7. Physical design issues are discussed within the context of existing process technologies, such as CMOS, bipolar, and biCMOS processes. This is followed by a discussion of appropriate protection circuitry. The chapter then continues to show the experimental results of the prototype circuit fabricated in MOSIS 2 μm CMOS technology with an added p-base layer. Finally, a summary of the performance specifications obtained as well as those targeted are discussed and illustrated in a table.

Chapter 8 brings forth the conclusions of the research as well as the implications thereof. The enabling techniques for low voltage and low quiescent current flow operation are summarized and discussed in perspective of the overall system. The direction of market demand in terms of technology and circuit requirements is also discussed. The chapter ends with a few concluding statements pertaining to the research as well as recommendations for future work in the area.

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SUMMARY

Regulators are an essential part of any electrically powered system, which includes the growing family of applications of portable battery operated products. Regulators are required to reduce the large voltage variations of battery cells to lower and more acceptable levels. Absence of these power supplies can prove to be catastrophic in most high frequency and high performance circuit designs. As a result, low drop-out regulators and other power supply circuits are always in high demand. In fact, the increasing drive towards total chip integration (single chip solutions) demands that power supply circuits be included in every chip. This is a consequence of the public demand for smaller and less expensive portable products.

In particular, the increasing demand for portable battery operated products has driven power supply design towards low voltage and low quiescent current flow, i.e., cellular phones, pagers, camera recorders, laptops, etc. The thrust is towards reducing the number of battery cells, required to decrease cost and size, while minimizing quiescent current flow to increase battery life. Current efficiency is particularly important because at low load-current conditions the life of the battery is adversely affected by low current efficiency, in other words, high quiescent current flow. At high load-currents, on the other hand, current efficiency is typically high because load-current is significantly larger than quiescent current. In this low voltage environment, a low drop-out regulator is the most appropriate form of linear regulators. However, the prevailing designs do not work at input voltages suitable for single, low voltage battery cells. This research develops techniques that enable practical circuit realizations of low

drop-out regulators at low input voltages and low quiescent current flow without sacrificing performance.

An intimate knowledge of the system reveals that the frequency stability requirements are dependent on load-current. As a result, a load dependent biasing buffer is designed to minimize current flow during low load-current conditions. Moreover, suitable biasing conditions result during transient load-current steps. This transient aid comes in the form of increased slew-rate current capabilities during conditions that warrant it. Another problem with low voltage in a CMOS environment is reduced gate drive for the power transistor. In other words, the output current capability per unit area of the power device under low voltage conditions is appreciably less than its higher voltage counterpart. However, gate drive can be effectively increased by reducing the threshold voltage. This is done by forward biasing the source to bulk junction of the power PMOS device and thus exploiting the bulk effect phenomenon. Yet another problem with low voltage is the realization of an accurate reference voltage. Typical bandgap references are restricted by input voltages greater than approximately 1.4 V (V_{sat} above the bandgap voltage). A circuit topology suitable for low voltages and curvature compensation is developed.

The overall system is designed, simulated, and experimentally evaluated. The process technology utilized is MOSIS 2 μm CMOS with a p-base layer. However, most of the techniques can be adapted to almost any technology ranging from bipolar and vanilla CMOS to relatively inexpensive and full blown biCMOS processes. As a result, the resulting system can be designed and optimized for low cost. The physical layout implications of the circuit realization are discussed with emphasis on reliability and performance. The findings show that a successful low voltage design is achieved by implementing the techniques developed. Furthermore, the techniques also showed that

they are appropriate for maximizing performance of most linear regulator designs outside the realm of low voltage.

CHAPTER I

INTRODUCTION

The demand for low drop-out regulators has been driven by the portable electronics market as well as industrial and automotive applications. Most recently, the increasing demand for portable and battery operated products have forced these circuits to operate under lower voltage conditions. Furthermore, high current efficiency has also become necessary to maximize the lifetime of the battery. Battery life is determined by the total current drain composed of quiescent current and load-current. This chapter discusses the role and the characteristics of low drop-out regulators in today's market. The objective of the research is then identified and defined according to the demands that drive regulator design into the future.

1.1 Definition

A series low-drop-out regulator is a circuit that provides a well specified and stable dc voltage [1] whose input to output voltage difference is low [2]. The drop-out voltage is defined as the value of the input/output differential voltage where the control loop stops regulating. The term series comes from the fact that a power transistor (pass device) is connected in series between the input and the output terminals of the regulator [3]. The operation of the circuit is based on feeding back an amplified error signal to control the output current flow of the power transistor driving the load. This type of

regulator has two inherent characteristics: (1) the magnitude of the input voltage is greater than the respective output and (2) the output impedance is low to yield good performance [2]. Low drop-out (LDO) regulators can be categorized as either low power or high power. Low power LDOs are typically those with a maximum output current of less than 1 A, exhibited by most portable applications. On the other hand, high power LDOs can yield currents that are equal to or greater than 1 A to the output, which are commonly demanded by many automotive and industrial applications [4].

1.2 Market Demand

Current Efficiency, Low Voltage, and Low Drop-out

As a result of high variations in battery voltage, regulators are demanded by virtually all battery operated applications. Furthermore, most designs find it necessary to include regulators and other power supply circuits as products achieve or approach total chip integration. Low drop-out regulator are appropriate for many circuit applications, namely, automotive, portable, industrial, and medical applications. In the automotive industry, the low drop-out voltage is necessary during cold-crank conditions where the battery voltage can drop below 6 V. The increasing demand, however, is readily apparent in mobile battery operated products, such as cellular phones, pagers, camera recorders, and laptops [5]. This portable electronics market requires low voltage and low quiescent current flow for increased battery efficiency and longevity [6]. As a result, high current efficiency is necessary to maximize battery life. Low voltage operation is also a consequence of the direction of process technology towards higher packing densities [7]. In particular, isolation barriers decrease as the component densities per unit area are increased thereby manifesting lower breakdown voltages [8, 9]. Minimization of drop-out voltages in a low voltage environment is also necessary to maximize dynamic

range. This is because the signal-to-noise ratio decreases as the power supply voltages decrease while noise typically remains constant [10, 11]. Consequently, low power and finer lithography drive regulators to operate at lower voltages, produce precise output voltages, and require low quiescent current flow [9]. By the year 2004, the power supply voltage is expected to be as low as 0.9 V in 0.14 μm technologies [9, 12]. Lastly, financial considerations also require that these circuits be fabricated in relatively simple processes, such as standard CMOS, bipolar, and stripped down biCMOS technologies [13].

Alternative: Switching Regulators

The alternatives to low drop-out regulators are dc-dc converters, switching regulators. Switching regulators are essentially mixed-mode circuits that feed back an analog error signal and digitally gate it to provide bursts of current to the output. The circuit is inherently more complex and costly than LDO realizations [9]. Furthermore, switching regulators can provide a wide range of output voltages including values that are lower or greater than the input voltage depending on the circuit configuration, buck or boost. The circuit, for the most part, requires a controller with an oscillator, pass elements, an inductor, capacitors, and diodes. Some switched-capacitor implementations do not require an inductor [14, 15].

The worst-case response time of a dc-dc converter is dependent on the oscillating frequency of the controller (approximately 20 to 200 kHz [16]) and circuit delay. As a result, the corresponding response time is roughly between 6 and 8 μs, whereas the LDO typically requires between 1 and 2 μs [12]. Since the pass elements switch high currents through an inductor at the rate of the oscillator, the output voltage is inherently noisy. This is especially true for boost configurations where RF noise tends to be worse [17]. The high noise present is a consequence of the rectified inductor voltage behavior of the

output of these converters. Furthermore, start-stop clock operation (on/off sleep-mode transitions) further aggravates the noise content of the output voltage [12].

On the other hand, switching regulators benefit from having high power efficiency and the ability to generate larger output voltages than the input. They can yield efficiencies between 80 and 95 % [18]. The efficiency of the LDO counterpart is limited by the quiescent current flow and the input/output voltages, and is expressed as

$$\text{Efficiency}_{\text{Power}} = \frac{I_o V_o}{\left[I_o + I_q\right] V_i} \leq \frac{V_o}{V_i}, \tag{1.1}$$

where I_o and V_o correspond to the output current and voltage, V_i is the input voltage, and I_q is the quiescent current or ground current. The main power issue in LDO design is battery life, in other words, the output current flow of the battery. When the load-current is low, which is the normal operating mode for many applications, the quiescent (ground) current becomes an intrinsic factor in determining the lifetime of the battery. Consequently, current efficiency is important during low load-current conditions. Power efficiency, on the other hand, becomes more pertinent during high load-current conditions where quiescent current is negligible relative to the output current.

If the maximum load-current is much greater than the ground current, then the maximum possible power efficiency is defined by the ratio of the output and the input voltages, as seen in equation (1.1). Power efficiency increases as the voltage difference between the input and the output decreases. Under these conditions, LDOs are better suited for many applications than switching regulators because of lower cost, complexity, and output noise. The choice becomes obscure, however, if the output current increases to the point where the LDO requires a heat sink [12]. A heat sink not only increases cost by requiring an additional component but it also means more real estate area overhead on

the board, which further increases cost. Applications that require high input/output voltage differentials with high output currents greatly benefit from the efficiency of dc-dc converters. Nevertheless, there are some cases where a high input/output voltage differential regulator is required to drive noise sensitive circuits. In these situations, a switching regulator is used to bring down the voltage and an LDO is cascaded to provide a low noise output [4, 18]. These conditions arise in mixed-mode designs where circuits that perform analog functions tend to be more sensitive to noise originated in the supply rails than the digital counterparts [17, 19]. Other applications require output voltages that are larger than the respective inputs. In these situations, dc-dc converters are necessarily used, be it in the form of a boost topology, a boosting switch capacitor implementation, or a charge pump structure. However, LDOs are still required in these applications to suppress noise generated by the switching pre-regulator. In summary, both LDOs and switching regulators have their place in today's market demand.

1.3 Characteristics

Block Level Description

Figure 1.1 illustrates the block level diagram of a generic series low drop-out regulator. The circuit is composed of a reference and associated start-up circuit, protection circuit and associated current sense element, an error amplifier, a pass element, and a feedback network. The reference provides a stable dc bias voltage with limited current driving capabilities. This is usually a zener diode or a bandgap reference. The zener diode finds its applications in high voltage circuits (greater than approximately seven volts) with relaxed temperature variation requirements [1, 3]. The bandgap, on the other hand, is better suited for low voltage and high accuracy applications. The protection circuitry ensures that the LDO operates in safe stable conditions. Some of its

functions include over-current protection (typically a foldback current limiter [6]), thermal shutdown in case of self-heating (junction temperature increases beyond safety levels), and other similar functions. The error amplifier, the pass element, and the feedback network constitute the regulation loop. The temperature dependence of the reference and the amplifier's input offset voltage define the overall temperature coefficient of the regulator; hence, low drift references and low input offset voltage amplifiers are preferred [20, 21].

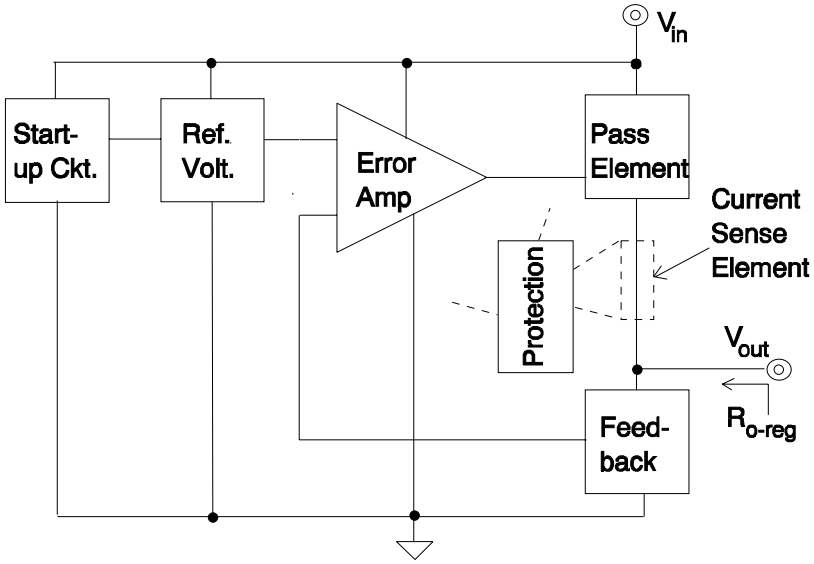

Figure 1.1. Generic low drop-out series linear regulator architecture.

Performance

Overall noise performance is strongly dependent on the physical layout of the chip and the respective process technology. In particular, the noise present at the output of the LDO is composed of three components, namely, noise injected from the system through the substrate and the input voltage, noise generated by the reference circuit, and noise associated with the output trace (lead) inductance and resistance [4]. Switching

regulators can typically be used to provide power to LDOs and can be integrated in the same chip as the LDO thereby injecting noise through the substrate and the input voltage, i.e., cellular phones. In these cases, physical layout isolation techniques and high power supply rejection ratio are intrinsic circuit characteristics for good noise performance. Transient load-current changes also affect the noise content seen by the load. This results from the parasitic resistance and inductance of the trace (lead) from the LDO's output to the load. Therefore, physical proximity of the LDO to its load must be minimized to reduce the noise seen by the load [12].

Low drop-out regulators tend to necessitate large output capacitors that occupy large board areas. Furthermore, typical LDOs require that these capacitors have low electrical series resistance (ESR). Consequently, capacitors play an intrinsic role in the cost of the LDO. High power LDOs may require heat sinks further aggravating the cost issue. However, a system level design choice may circumvent the need for a heat sink by utilizing several smaller LDOs distributed throughout the board [4]. Finally, the emergence of finer lithography and the increasing demand for low power cause low voltage operation to be a necessary condition. Therefore, there are some circuit design techniques that are discouraged, which give rise to more complex and possibly more expensive circuits. Some of the discouraged techniques include unnecessary cascoding, emitter followers, and Darlington configurations [10].

1.4 Specifications

System

The important aspects of the LDO can be summarized into three categories, namely, regulating performance, quiescent current flow, and operating voltages [22]. Some of the specifications that serve as metrics for the LDO include drop-out voltage,

line regulation, load regulation, tolerance over temperature, output voltage variation resulting from transient load-current steps, output capacitor and ESR range, quiescent current flow, maximum load-current, and input/output voltage range. The requirements of these performance characteristics often contradict each other giving rise to necessary compromises. The priority of the performance parameters is defined according to the particular application.

Drop-out voltage is the minimum input/output differential voltage where the circuit just ceases to regulate. This can be expressed in terms of switch "on" resistance, R_{on} [6],

$$V_{drop\text{-}out} = I_{Load}\, R_{on}. \tag{1.2}$$

Typical drop-out voltages range from 0.1 to 1.5 V [4]. The output voltage variation arising from a specific change in input voltage is defined as line regulation. Similarly, load regulation is the change in output voltage for specific changes in load-current [2]. Load regulation is essentially the output resistance of the regulator ($R_{o\text{-}reg}$),

$$R_{o-reg} = \frac{\Delta V_{LDR}}{\Delta I_o} = \frac{R_{o-pass}}{1 + A_{ol}\beta}, \tag{1.3}$$

where ΔV_{LDR} and ΔI_o are the output voltage and the load-current changes, $R_{o\text{-}pass}$ is the output resistance of the pass element, A_{ol} is the open-loop gain of the system, and β is the feedback factor [3]. Therefore, load regulation performance is improved as the dc open-loop gain is increased [12]. The temperature dependence of the output voltage is a function of the temperature drift of the reference and that of the input offset voltage of the error amplifier,

$$TC = \frac{1}{V_o} \cdot \frac{\partial V_o}{\partial Temp} \approx \frac{1}{V_o} \cdot \frac{\Delta V_{TC}}{\Delta Temp} = \frac{\left[\Delta V_{TC\,ref} + \Delta V_{TC\,Vos}\right] \frac{V_o}{V_{ref}}}{V_o \Delta Temp}, \quad (1.4)$$

where TC is the temperature coefficient, ΔV_{TC} is the output voltage variation over the temperature range $\Delta Temp$, ΔV_{TCref} and ΔV_{TCVos} are the voltage variations of the reference and input offset voltage of the error amplifier, and V_o / V_{ref} is the ratio of the nominal output and reference voltages. Transient output voltage variations resulting from sudden load-current changes are dominated by the closed-loop bandwidth of the system, output capacitor, and load-current. The worst-case situation occurs when the load-current suddenly steps from zero to its maximum specified value. The resulting output voltage variation is described as

$$\Delta V_{tr} \approx \frac{I_{Load-max}}{C_o + C_b} \Delta t + \Delta V_{esr}, \quad (1.5)$$

where ΔV_{tr} is the output voltage change, $I_{Load\text{-}max}$ is the maximum specified load-current, C_o is the output capacitor, C_b refers to the bypass capacitors, ΔV_{esr} is the voltage variation resulting from the electrical series resistance (ESR) of the output capacitor, and Δt is the time required for the LDO to respond (approximately equal to the reciprocal of the closed-loop bandwidth (BW_{cl}) if internal slew-rate conditions are neglected). The voltage variation resulting from ESR results because of the momentary current (provided by C_o) flowing through the ESR. This is reduced by the high frequency nature of the bypass capacitors (low ESR capacitors). In other words, the bypass capacitors (C_b) help filter out the effects of the output capacitor ESR. Consequently, fast response times and low ESR values are necessary to yield low transient output voltage variations. Low

output voltage variations are desired to meet the overall accuracy requirements of the system, i.e., 150 - 300 mV [9]. Thus, the circuit as a whole benefits from the use of a high bandwidth amplifier in the feedback loop. A pivotal specification is the output capacitor and associated ESR range for which the LDO is stable. This can typically prove to be a difficult task if a wide range of values is to be allowed. The value of the load-current also affects the frequency response of the circuit. Lastly, long term stability and low external component count are also pertinent factors to keep in mind when designing LDOs.

The effects of line regulation, load regulation, temperature dependence, and transient output voltage variations can be summed up into one specification, accuracy. Accuracy refers to the total output voltage variation and can be described by the absolute minimum and maximum output voltages ($V_{o\text{-}min}$ and $V_{o\text{-}max}$), shown in the following equations:

$$V_{o-min} \le \Delta V_{LNR} + \Delta V_{LDR} + \Delta V_{TC} + \Delta V_{tr} + V_{reference}\left\langle \frac{V_o}{V_{ref}} \right\rangle \le V_{o-max}, \quad (1.6)$$

$$V_{reference} = V_{ref} + \Delta V_{TC_{ref}} + \Delta V_{LNR_{ref}} \pm V_{os}, \quad (1.7)$$

$$Accuracy_{system} = \left\langle \frac{V_{o-max} - V_{o-min}}{V_o} \right\rangle, \quad (1.8)$$

where ΔV_{LNR}, ΔV_{LDR}, ΔV_{TC}, ΔV_{tr}, $\Delta V_{TC_{ref}}$, and $\Delta V_{LNR_{ref}}$ are voltage variations resulting from line regulation, load regulation, temperature dependence, worst-case transient load-current steps, reference circuit's temperature dependence, and reference circuit's line regulation respectively while V_{os} and V_o are the input offset voltage of the

error amplifier and the nominal output voltage of the regulator. In specifying accuracy, the effect of the transient load-current step and the reference circuit is sometimes excluded but they are included here for completeness. Low voltage operation often implies more stringent specifications in the form of overall accuracy. Typical implementations achieve roughly 1 to 2 % total variation resulting from load regulation, line regulation, and temperature dependence while leaving some headroom for transient output voltage variations [12].

Reference

The specifications of the reference include line regulation, temperature dependence, quiescent current flow, and input voltage range. The effects of line regulation and temperature drift on system accuracy are shown in equations (1.6) - (1.7). Line regulation refers to the variation of the reference voltage arising from a unit change in input voltage. In the same token, the temperature coefficient of the reference (TC_{ref}) refers to the variation in output voltage as a result of unit changes in temperature and can be expressed as

$$TC_{ref} = \frac{1}{V_{ref}} \cdot \frac{\partial V_{ref}}{\partial Temp} \approx \frac{1}{V_{ref}} \cdot \frac{\Delta V_{TC_{ref}}}{\Delta Temp}, \tag{1.9}$$

where ΔV_{TCref} is the reference voltage change resulting from a temperature variation equal to $\Delta Temp$ and V_{ref} is the nominal reference voltage. The overall accuracy of references is determined by the combination of line regulation and temperature coefficient performance and is described as

$$Accuracy_{reference} = \frac{\Delta V_{TC_{ref}} + \Delta V_{LNR_{ref}}}{V_{ref}}, \tag{1.10}$$

where ΔV_{TCref} and ΔV_{LNRref} are voltage variations resulting from temperature dependence and line regulation respectively. Load regulation is sometimes included in the accuracy of the reference but most appropriately specified for regulator structures.

1.5 Research Objective

The objective of this research is to enhance performance of low drop-out (LDO) regulators for battery powered electronics. This is targeted to fulfill the present commercial requirements as well as the projected demands of the future. Such an endeavor makes certain characteristics necessary, namely, low quiescent current flow for increased battery life, low voltage operation, and high output current. The techniques that are developed to overcome the aforementioned obstacles not only enhance the prevailing LDO circuit architecture but also push regulator design into the 21st century. This is done with existing standard technologies; thus, the designs take full advantage of all physical aspects of the process while maintaining fabrication costs to acceptable and competitive levels. Moreover, the new design techniques will be able to further exploit the benefits of more advanced technologies in the future.

The intrinsic issues in designing a current efficient (low quiescent current) and low drop-out linear regulator in a low voltage environment can be identified as stability, maximum output current, and regulating performance. Stability in a low quiescent current atmosphere is difficult to achieve because of the presence of potentially low frequency parasitic poles. These are easily circumvented by increasing bandwidth, which usually results at the expense of higher quiescent current flow. Maximum output current capabilities of regulators also becomes restricted under low voltage conditions. This results from the inherent reduction in gate drive for the pass element when input voltages

are decreased. Finally, low voltage circuits tend to limit the regulating performance of regulators because of problems with headroom. As input voltages decrease, the use of common circuit techniques that enhance performance becomes restrained, i.e., cascoding, Darlington configurations, and source [emitter] followers [10]. In a battery powered environment, the number of devices connected from the input voltage to ground must be kept low [10]. The ultimate limit is one diode drop plus one output saturation voltage, V_{be} [V_{gs}] + $V_{ec\text{-}sat}$ [$V_{sd\text{-}sat}$].

An input voltage range appropriate for single, low voltage battery cells is targeted (0.9 to 1.5 V). The circuit technology is MOSIS 2 μm CMOS with an added p-base layer, a relatively inexpensive process. The minimum operating voltage possible for this technology is approximately between 1 and 1.1 V, $V_{sg\text{-}pmos}$ + $V_{ds\text{-}nmos}$. For maximized battery life, the circuits must be current efficient and micro-power. The zero-load quiescent current goal is approximately 60 to 65 μA including the reference and the regulating loop, 15 - 20 μA for the reference and 40 - 45 μA for the remainder. Since the thrust of the driving market demand lies in battery operated regulators, the output current range is defined to be between 50 and 100 mA for respective input voltages ranging from 1.2 to 1.5 V. The design criteria also focuses on minimizing transient output voltage variations resulting from fast load-current step transitions, less than 75 mV.

To further mitigate overall costs, standard tantalum capacitors are used for the output. These are among the least expensive with an electrical series resistance (ESR) range of up to approximately 10 Ω [23]. The target range of ESR is extended to zero to cater to applications where low ESR is necessary. Low values of ESR are demanded for high power supply rejection ratio (PSRR) performance at high frequencies and minimized transient output voltage variations. The PSRR performance of LDOs (generically illustrated in Figure 1.2) at high frequencies is approximated to be

$$\mathrm{PSRR} = \frac{\Delta V_{\mathrm{supply}}}{\Delta V_o} \cdot \frac{V_o}{V_{\mathrm{ref}}} = \frac{\Delta V_{\mathrm{in}}}{\Delta V_o} A_v(s) \approx \frac{R_{o-\mathrm{pass}} + R_{\mathrm{esr}}}{R_{\mathrm{esr}}} A_v(s), \qquad (1.11)$$

where ΔV_{supply} is equivalent to ΔV_{in} for regulators, $A_v(s)$ is the open-loop gain from V_{ref} to V_o, and the terminology of Figure 1.2 is adopted. Consequently, PSRR at high frequencies, when $A_v(s)$ approaches unity, greatly benefits from low ESR values. This is

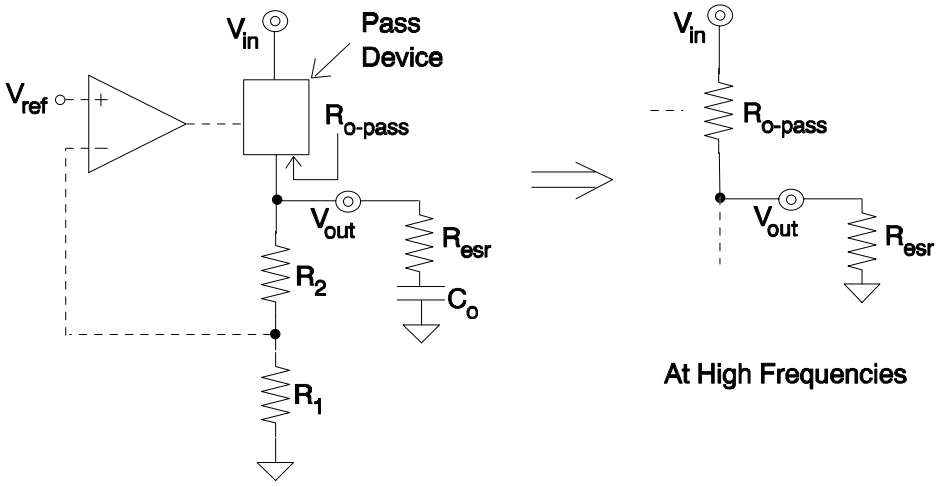

Figure 1.2. PSRR performance implications of high frequency operation.

especially important when considering that $R_{o\text{-}pass}$ for CMOS structures is relatively low because of short channel lengths, which result in poor early voltage performance. Power MOS transistors require shorter channel lengths to provide larger output currents. Power supply rejection ratio performance at high frequencies is important in designs that integrate a switching regulator on to the same chip as the LDO. This results in injection of systematic noise to the output at the frequency of the clock , typically between 100 and 500 kHz.

The typical specifications for low voltage LDOs (≥ 2.3 V input voltage range) include drop-out voltages of 0.4 to 0.9 V at output currents of 40 mA and output voltage accuracy of 4 to 5 % [24, 25, 26]. The design target focuses on a drop-out voltage ranging from 0.2 to 0.3 V at a load-current of 50 to 100 mA (corresponding to an "on" resistance (R_{on}) of 2 to 6 Ω) with a total tolerance of roughly ± 3 to 5 %. Furthermore, the regulator's destination is the commercial market place with a temperature range of -10 to 90 °C, which includes customary temperature limits. Table 1.1 illustrates a summary of the objective performance parameters for this research.

1.6 Summary

This chapter has defined a low drop-out regulator (LDO) and discussed its standing in today's market. The characteristics that are most demanded by the growing number of applications were identified. This was followed by a discussion of switching regulators and their place alongside LDOs. The main building blocks of low drop-out regulators were described as well as some of their associated performance parameters. Moreover, the specifications that gauge these circuits were defined. Lastly, the research objective was identified and defined according to the growing requirements of current and future applications. Overall, this chapter forms the premise and establishes enough background to start analyzing the system under loading conditions and start considering the electrical implications of such an architecture.

Table 1.1 Summary of the objective specifications.

Description	**Specification**
V_{in}	≥ 1.2 V
I_q	≤ 65 μA
$I_{out\text{-}max}$	≥ 50 mA
Accuracy	± 3 to 5 %
$V_{drop\text{-}out}$ @ I_{Load} = 50 - 100 mA	≤ 0.3 V
R_{on}	2 to 6 Ω
Transient $\Delta V_{o\text{-}for\ I_{Load\text{-}Step}}$	≤ 75 mV
Temperature	-10 to 90 °C
Output Capacitance	4.7 μF
ESR	0 to 10 Ω
Technology: MOSIS 2 μm n-well CMOS with added p-base layer	

CHAPTER II

SYSTEM DESIGN CONSIDERATIONS

Proper design of a low drop-out (LDO) regulator involves intricate knowledge of the system and its load. The tasks of maximizing load regulation, maintaining stability, and minimizing transient output voltage variations prove to be challenging and often conflicting. This arises from the innate characteristics of the regulator architecture and its associated working environment. This chapter discusses the relevant analyses that describe the system. Lastly, some of the circuit design issues surrounding the major components of the low drop-out regulator are illustrated in terms of circuit theory and system requirements; these building blocks include the pass device, the amplifier, and the reference.

2.1 AC Analysis

Loading Conditions

Figure 2.1 illustrates the intrinsic factors that determine the stability of the system, namely, an error amplifier, a pass element, feedback resistors, an output load-current and associated output impedance, an output capacitor and associated electrical series resistance (ESR), and bypass capacitors. It is assumed that there is no ac signal polarity inversion across the pass device, corresponding to n-type transistor implementations. The polarity of the error amplifier terminals would be reversed for p-

type devices, which introduce a polarity inversion ($-g_{mp}$ instead of g_{mp}). The ESR of the bypass capacitors can typically be neglected because they are usually high frequency capacitors; in other words, they have low ESR values [23]. The pass device is modeled as a circuit element exhibiting a transconductance of g_{mp} and an output impedance of $R_{o\text{-}pass}$. The value of R_2 is dependent on the desired value of the output voltage, i.e., R_2 is zero if V_{out} is desired to be equal to V_{ref}. The value of R_1, on the other hand, is designed to define the quiescent current flowing through resistors R_1 and R_2 ($R_1 = V_{ref} / I_{R1}$), which is typically high to minimize quiescent current overhead.

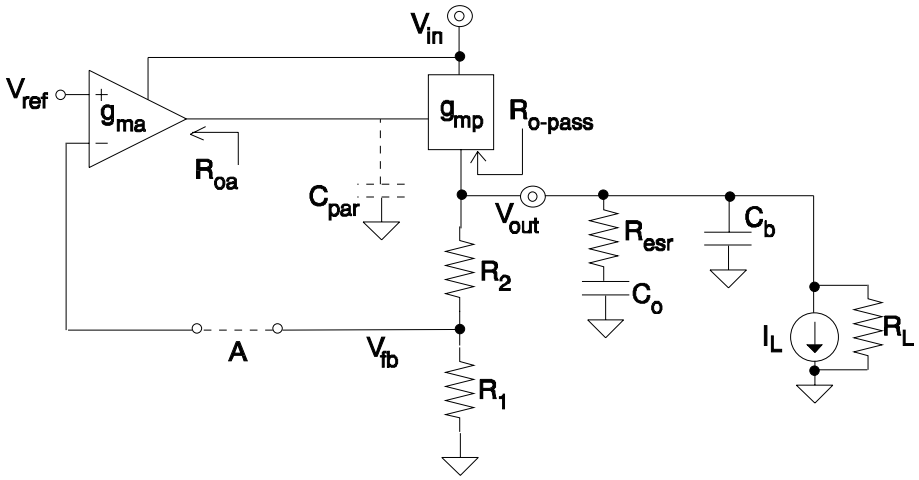

Figure 2.1. System model under loading conditions.

Frequency Response

For the purpose of analysis, the feedback loop can be broken at "A" in Figure 2.1. It is readily apparent that the system must be unity gain stable, considering V_{ref} and V_{fb} to be the input and the output voltages respectively. The open-loop gain can be described as

$$\frac{V_{fb}}{V_{ref}} = |A_v| = \frac{g_{ma} R_{oa} g_{mp} Z}{\left[1 + sR_{oa} C_{par}\right]} \cdot \frac{R_1}{\left[R_1 + R_2\right]}, \tag{2.1}$$

where g_{ma} and g_{mp} refer to the transconductance of the amplifier and the pass element respectively, R_{oa} is the output resistance of the amplifier, C_{par} refers to the parasitic capacitance introduced by the pass element, and Z is the impedance seen at V_{out},

$$Z = R_x || \frac{1 + sR_{esr} C_o}{sC_o} || \frac{1}{sC_b} = \frac{R_x\left[1 + sR_{esr} C_o\right]}{s^2 R_x R_{esr} C_o C_b + s\left[R_x + R_{esr}\right]C_o + sR_x C_b + 1}, \tag{2.2}$$

where C_o and R_{esr} are the capacitance and the ESR of the output capacitor, C_b represents the bypass capacitors, and R_x is the resistance seen from V_{out} back into the regulator defined as

$$R_x = R_{o-pass} \,||\left(R_1 + R_2\right), \tag{2.3}$$

where $R_{o\text{-}pass}$ is the output resistance of the pass element. The output resistance of the load (R_L) is commonly neglected because its value is considerably larger than R_x. If C_o is assumed to be reasonably larger than C_b (typical condition), then Z approximates to

$$Z \approx \frac{R_x\left[1 + sR_{esr} C_o\right]}{\left[1 + s\left(R_x + R_{esr}\right)C_o\right] \cdot \left[1 + s\left(R_x || R_{esr}\right)C_b\right]}. \tag{2.4}$$

It can be observed from equations (2.1) - (2.4) that the overall transfer function of the system consists of three poles and one zero, a potentially unstable system. For the majority of the load-current range, R_x simplifies to $R_{o\text{-}pass}$ since $R_1 + R_2$ is greater in

magnitude (especially at high currents). The poles and the zero can thus be approximated to be the following:

$$P_1 \approx 1 / 2\pi R_{o\text{-}pass} C_o, \quad (2.5)$$

$$P_2 \approx 1 / 2\pi R_{esr} C_b, \quad (2.6)$$

$$P_3 \approx 1 / 2\pi R_{oa} C_{par}, \quad (2.7)$$

and

$$Z_1 \approx 1 / 2\pi R_{esr} C_o. \quad (2.8)$$

Figure 2.2 illustrates the typical frequency response of the system assuming that the output capacitor (C_o) is larger than the bypass capacitors (C_b). Figure 2.3 shows the simulation results of the circuit of Figure 2.1 using a macro-model for the amplifier, a PMOS device for the pass element, and a load-current of 70 mA. The simulation confirmed the overall behavior of the frequency response predicted by analysis with a dc open-loop gain of 43.6 dB, unity gain frequency of 3 MHz, and a phase margin of 29.5 °.

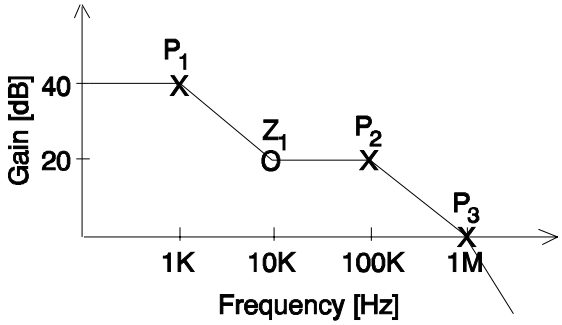

Figure 2.2. LDO frequency response under loading conditions.

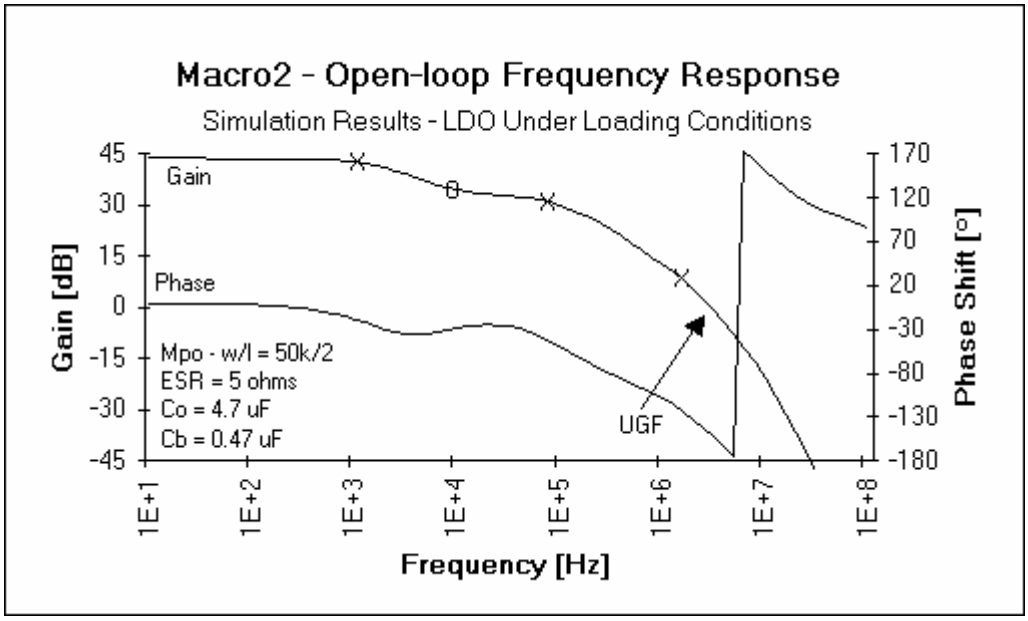

Figure 2.3. AC simulation results of an LDO under loading conditions.

Design Challenge

Worst-case Stability: The worst-case stability condition, given the set of elements shown in Figure 2.1, arises when the phase margin is at its lowest point, which occurs when the unity gain frequency is pushed out to higher frequencies where the parasitic poles reside. This happens when the load-current is at its peak value [23]. This is because the dominant pole (P_1) usually increases at a faster rate ($R_{o\text{-}pass}$ decreases linearly with increasing current, $1/\lambda I_o$ or V_a/I_o where λ is the channel length modulation parameter of MOS devices and V_a is the early voltage of bipolar transistors) than the gain of the system decreases ($g_{mp}R_{o\text{-}pass}$ decreases with the square root of the increasing current for an MOS device or stays constant for a bipolar transistor). The type and value of the output capacitor determine the location of P_1, P_2, and Z_1. Therefore, the permissible range of values of ESR for a stable circuit is a function of load-current and circuit characteristics [5]. Simulations confirm the aforementioned tendencies.

Parasitic Pole Requirements: The parasitic poles of the system can be identified as P_3 and the internal poles of the error amplifier. These poles are required to be at high frequencies, at least greater than the unity gain frequency (UGF). The phase margin for the case where only one parasitic pole was at the vicinity of the UGF is approximately 45°. Ensuring that P_3 is at high frequencies is an especially difficult task to undertake in a low current environment. The pole is defined by the large parasitic capacitance (C_{par}) resulting from a large pass device (necessary trait for reasonable output current capabilities) and the output resistance of the amplifier (R_{oa}). The amplifier's output impedance is usually a function of the circuit topology and the bias current of its output stage. As a result, low quiescent current and frequency design issues have conflicting requirements that necessitate compromises.

Maximum Load Regulation Performance: Load regulation performance (output resistance of the regulator, R_o) is a function of the open-loop gain (A_{ol}) of the system and can be expressed as

$$R_o = \frac{\Delta V_{LDR}}{\Delta I_o} = \frac{R_{o-pass}}{1 + A_{ol}\beta}, \tag{2.9}$$

where ΔV_{LDR} is the output voltage variation arising from a load-current variation of ΔI_o, $R_{o\text{-}pass}$ is the output resistance of the pass device, and β is the feedback factor. Consequently, the regulator yields better load regulation performance as the open-loop gain increases [12]. However, the gain is limited by the closed-loop bandwidth of the system, equivalent to the open-loop unity gain frequency (UGF). The minimum UGF is bounded by the response time required by the system during transient load-current variations, as discussed in the specifications section of chapter 1. Furthermore, the UGF is also bounded at the high frequency range by the parasitic poles of the system, i.e., the

internal poles of the amplifier and pole P_3. If these parasitic poles are assumed to be located at higher frequencies than 1 MHz, then the gain at 1.0 kHz has to be less than approximately 35 - 45 dB depending on the location of Z_1 and P_2, as shown in Figures 2.2 and 2.3. In particular, the worst-case condition occurs when Z_1 is at low frequencies and P_2 is at high frequencies, which corresponds to the maximum value of ESR and the lowest bypass capacitance (C_b). Moreover, the pass element's associated input capacitance (error amplifier's load capacitance) is significantly large. This places a ceiling on the value of the amplifier's output resistance (R_{oa}). The pass element typically needs to be a large device to yield low drop-out voltages and high output current characteristics with limited voltage [current] drive in a low voltage and low power environment. Overall, load regulation is limited by the constrained open-loop gain of the system.

2.2 Transient Analysis

An important specification is the maximum allowable output voltage change for a full range transient load-current step. The application determines how low this value should be. For instance, a relatively relaxed specification for the peak output voltage variation can be tolerated if the regulator is used to provide power to digital circuits, which inherently have high noise margins [6]. However, this is not the case for many analog applications. Figure 2.4 shows the characteristic nature of the stimulus and the typical respective response for the typical system shown in Figure 2.1 [27].

Typical Response

The worst-case time required for the loop to respond (Δt_1, which is ideally the reciprocal of the closed-loop bandwidth) is specified by the maximum permissible output voltage variation (ΔV_{tr}), which is a function of the output capacitor (C_o), the electrical series resistance (ESR) of the output capacitor, the bypass capacitors (C_b), and the maximum load-current ($I_{Load\text{-}max}$),

$$\Delta V_{tr-max} \approx \frac{I_{Load-max}}{C_o + C_b} \Delta t_1 + \Delta V_{esr} \tag{2.10}$$

thus

$$\Delta t_1 \approx \frac{[C_o + C_b]}{I_{Load-max}} [\Delta V_{tr-max} - \Delta V_{esr}], \tag{2.11}$$

where ΔV_{esr} is the voltage variation resulting from the presence of the ESR (R_{esr}) of the output capacitor ($\Delta V_{esr} \propto R_{esr}$). The effects of ESR are reduced by the bypass capacitors

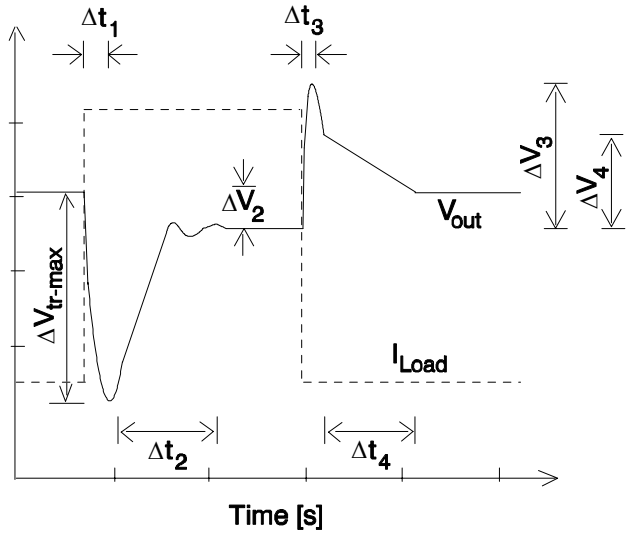

Figure 2.4. Typical LDO transient response to a load-current step.

(C_b), which are typically high frequency thereby exhibiting low ESR values. In typical implementations the time Δt_1 is not only a function of bandwidth but also defined by the internal slew-rate associated with the parasitic capacitance C_{par} of the pass element in Figure 2.1. The resulting time can be approximated to be

$$\Delta t_1 \approx \frac{1}{BW_{cl}} + t_{sr} = \frac{1}{BW_{cl}} + C_{par}\frac{\Delta V}{I_{sr}}, \tag{2.12}$$

where BW_{cl} is the closed-loop bandwidth of the system, t_{sr} is the slew-rate time associated with C_{par}, ΔV is the voltage variation at C_{par}, and I_{sr} is the slew-rate limited current. For instance, if BW_{cl} is 500 kHz, C_{par} is 200 pF, ΔV is 0.5 V, I_{sr} is 5 μA, C_o is 10 μF, R_{esr} is 0 Ω, and $I_{Load\text{-}max}$ is 100 mA, then the maximum output voltage variation is approximately 220 mV (equations (2.10) and (2.11)). If the slew-rate current is large enough, the reciprocal of the closed-loop bandwidth predominantly defines Δt_1. This would be at the cost of quiescent current flow, in other words, battery life. Once the slew-rate condition is terminated, the output voltage recovers and settles to its final value, ΔV_2 below the ideal value,

$$\Delta V_2 \approx R_{o-reg} I_{Load-max}, \tag{2.13}$$

where $R_{o\text{-}reg}$ is the closed-loop output resistance of the regulator. This is essentially the effect of load regulation performance on the output. The settling time (Δt_2) is dependent on the time required for the pass device to fully charge the load capacitors and the phase margin of the open-loop frequency response.

The slew-rate limitation is usually unidirectional in nature thereby creating the asymmetrical response of Figure 2.4. The slew-rate condition typically occurs when the

load-current steps from zero to full range. The direction for which this condition occurs is dependent on the configuration of the buffer and the output pass device. A typical topology is that of a class A buffer driving a PMOS pass element and associated parasitic capacitance (C_{par}). An example of this is illustrated in the simplified schematic of Figure 2.5 where the pass device is assumed to be a p-type transistor. A class A stage yields high current in one direction and limited dc current in the other, i.e., emitter [source] follower biased with a dc current source. More complex topologies, however, could be implemented for the buffer to realize high symmetrical slew-rate currents. The portion of

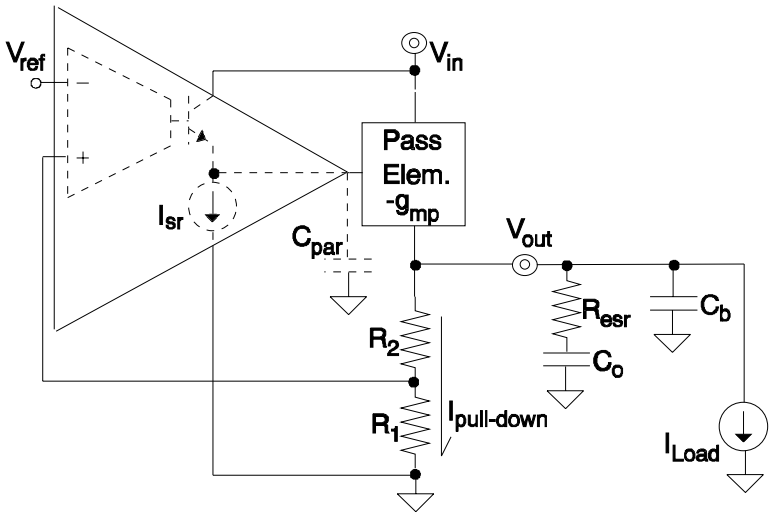

Figure 2.5. Simplified LDO schematic for the purpose of transient analysis.

the time response that does not experience internal slew-rate is dominated by the capacitors, the electrical series resistance (ESR) of the output capacitor, the bandwidth of the system, and the low pull-down current capability of the LDO's output ($I_{pull\text{-}down}$ in Figure 2.5). At first, the output voltage variation peaks at ΔV_3, whose magnitude is defined by the voltage charged on the capacitors and the voltage generated across the ESR of the output capacitor. This results because the momentary current supplied by the

power device ($I_{Load\text{-}max}$ until the circuit reacts to shut it off) flows to the output capacitor C_o and the bypass capacitors (the current is no longer flowing to the load). Consequently, the capacitors charge up and a temporary voltage drop is created across R_{esr}. This transient voltage can be approximtely described by

$$\Delta V_3 \approx \frac{I_{Load-max}}{C_o + C_b}\Delta t_3 + \Delta V_{esr} \approx \frac{I_{Load-max}}{C_o + C_b} \cdot \frac{1}{BW_{cl}} + \Delta V_{esr}, \qquad (2.14)$$

where the terminology of Figures 2.4 and 2.5 is adopted. When the output transistor is finally shut off (after Δt_3) the variation settles down to ΔV_4, the voltage charged on the capacitors ($\Delta V_4 \approx \Delta V_3 - \Delta V_{esr}$). At this point, the output voltage takes time Δt_4 to discharge to its final ideal value,

$$\Delta t_4 \approx \frac{C_o + C_b}{I_{pull-down}}\Delta V_4 = \frac{[C_o + C_b]R_1}{V_{ref}}\Delta V_4. \qquad (2.15)$$

Figure 2.6 illustrates the simulation results of an LDO transient response analysis. The circuit utilized employs the basic topology shown in Figure 2.5 using a macro-model for the amplifier and a PMOS pass device. The addition of high frequency bypass capacitors (capacitors with low ESR) reduce the peaks of the transient response, $\Delta V_{tr\text{-}max}$ and ΔV_3. This results because the current supplied by the output capacitor (C_o) during transient conditions is decreased as C_b is increased thereby exhibiting a lower voltage drop across R_{esr}. The remaining current is furnished by the bypass capacitors, which typically have negligible ESR voltage drops.

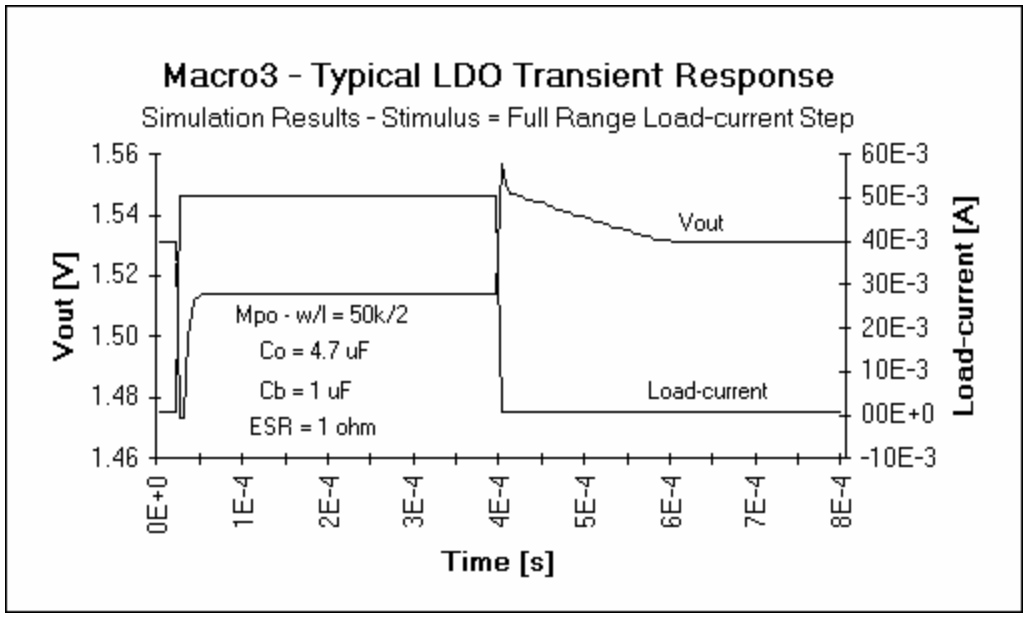

Figure 2.6. Simulated LDO transient response of a circuit similar to that of Figure 2.5.

Design Challenge

The worst-case output voltage variation is a function of the bandwidth and the slew-rate limit of the circuit. However, bandwidth and slew-rate limit are highly dependent on quiescent current flow. As bandwidth is demanded to increase, the parasitic poles are required to increase accordingly thereby necessitating more current flow to decrease associated impedances. Consequently, the error amplifier's quiescent current must necessarily increase to yield faster response times. Moreover, increasing slew-rate performance requires an increase in bias current on the circuit driving the slew-rate limited node. This affects the design of the output stage of the amplifier. As a result, the overall minimum quiescent current flow is limited by the maximum allowable output voltage variation arising from full range load-current steps.

2.3 Pass Device Design Issues

Designing in a low voltage and low current environment provides difficult challenges that contradict performance and stability [23]. The first aspect that is affected is the series pass element of the low drop-out regulator. It must provide large amounts of current while displaying low drop-out characteristics. Drop-out voltage is governed by the on resistance of the pass transistor ($V_{drop\text{-}out} = I_{Load}R_{on}$), which is inversely proportional to the physical size of the device. Drop-out voltage is further increased by series parasitic resistance inherent in the layout, such as the pass device's source [emitter] and drain [collector] contacts, metal traces, and diffusion links. As a result, the size of the transistor must be large under low voltage conditions, which translates to a large load capacitance for the error amplifier. A large device is further demanded because voltage drive is reduced as a result of decreased input voltages. This, in turn, causes the parasitic pole P_3 to move to lower frequencies effectively deteriorating phase margin and compromising the stability of the system. Moreover, the resulting increase in load capacitance for the feedback amplifier requires an increase in quiescent current flow. This is necessary to charge and discharge the capacitance quickly enough during slew-rate conditions, as discussed in the transient analysis section. For the case of MOS pass devices, sub-threshold currents can become appreciably large as the aspect ratio is increased. In other words, the transistor can be difficult to shut off thereby creating problems at zero-load conditions. Finally, the physical design of the large device must also take into account line resistance and capacitance, current density per line, heat distribution, and parasitic devices inherent to the layout. Thermal symmetry as well as equal current density distribution must be maintained for reliability and best performance. Overall, the size of the pass device must be large for increased current capabilities but restrained by stability and slew-rate requirements in a low quiescent current flow and low voltage environment.

The problem of handling large output currents or reducing the "on" resistance of MOS pass devices is sometimes cost efficiently resolved by using a dc-dc converter in addition to the LDO. The purpose of the switching regulator is to bring down the voltage thereby reducing the operating voltages of the LDO. As a result, devices with lower breakdown voltages can be used. In other words, the MOS pass device can reduce its channel length without posing any threat to the reliability of the circuit. Thus, larger aspect ratios per unit area and higher output currents are achieved. The additional cost of the switching regulator is offset by the potential cost of increasing the size of the pass device, increased area overhead. The point where this technique becomes valuable is dependent on the process technology, the application, and the associated specifications.

2.4 Amplifier Design Issues

The specifications of the amplifier that are relevant to the regulator as inferred from the previous discussions are: output impedance, gain, bandwidth, output slew-rate current, output voltage swing, and quiescent current. The output impedance must be low enough to place the parasitic pole P_3 (equation (2.7)) at a frequency greater than the unity gain frequency, thus maintaining stability. The requirement is stringent because of the large value of the load capacitance introduced by the vast pass device. This requires the use of a buffer to isolate the high output resistance of the gain stage (R_{og}) from the high load capacitance (C_{par}), as illustrated in Figure 2.7.

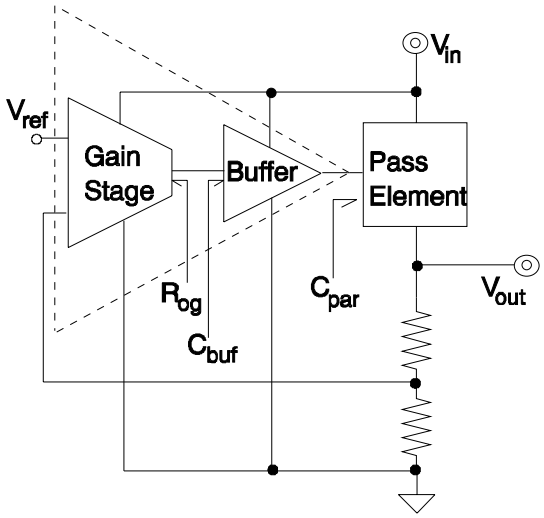

Figure 2.7. LDO buffered architecture.

Load regulation performance is enhanced as the open-loop gain of the system is increased, equation (2.9). However, the gain is limited by the unity gain frequency, as discussed in the ac analysis section. Therefore, caution must be exercised in designing the gain-bandwidth product (GBW) of the amplifier. This is dependent on the location of the output poles and the zero of the system, namely, P_1, P_2, and Z_1 (equations (2.5), (2.6), and (2.8)). It is further noted that the location of the dominant pole (P_1) varies with load-current, i.e., $R_{o\text{-}pass} \propto 1/I_{Load}$ for all pass elements except for the NMOS source follower, where $R_{o\text{-}NMOS} \propto 1/\sqrt{I_{Load}}$.

The topology and the biasing current of the buffer is designed according to the frequency and the transient response requirements of the system. Transient specifications tend to dominate the bias current demands of the buffer. In particular, the slew-rate current available to the output of the buffer partially determines the magnitude of the output voltage variation during transient load-current steps, as discussed in the transient analysis. The choice in topology also reflects the driving requirements of the pass device. For instance, a PMOS pass device requires a high negative voltage swing to

yield maximum gate drive and thus produce large output currents and low drop-out voltages. On the other hand, a sufficiently high positive swing is needed to shut off the device to the point where sub-threshold currents do not become a problem. A simple implementation of the buffer could be a source follower using a natural NMOS transistor, which is a non-threshold adjusted device exhibiting threshold voltages close to zero [3]. These devices are available at the possible cost of one extra mask in the process flow. The product of the input capacitance of the buffer (C_{buf}) and the output resistance of the gain stage (R_{og}) must be kept low to yield an internal frequency pole that is greater than the unity gain frequency of the system. Therefore, the ohmic resistance and line capacitance of the trace path in the layout between the output of the gain stage and the input of the buffer must be minimized.

The overall design of the amplifier must be kept as simple as the specifications will allow to necessitate low quiescent current flow. The limiting factors for low quiescent current are the amplifier's bandwidth and slew-rate requirements. A tradeoff between performance and power dissipation is therefore necessary. In a low voltage environment, such as the case for battery operated applications, the number of devices connected from the input voltage to ground must also be kept low [10]. The ultimate limit is one diode connected device and one saturation voltage drop, V_{be} [V_{gs}] + $V_{ec\text{-}sat}$ [$V_{sd\text{-}sat}$]. More flexibility may be allowed if the limiting factor lies elsewhere in the system, i.e., pass element's voltage drive requirements.

2.5 Reference Design Issues

The main issue involved in the design of the reference is accuracy and low voltage operation, input and output voltages included. Bandgap references are the most appropriate for low voltage. They are accurate circuits with typical output voltages of

roughly 1.2 V. The respective input voltage limitation is roughly 1.4 - 1.5 V (a V_{sat} above the reference). Power supply rejection ratio is another important factor, especially in mixed-signal designs where noise is coupled from high speed digital circuits [13]. As a result, the noise floor must be kept low to maximize dynamic range. This translates to the design of low noise circuits. Typically, 1/f noise tends to be important in prevailing regulator designs [28].

The difficulties in designing a precise low voltage bandgap reference arise from maintaining accuracy at lower power supply voltages while keeping quiescent current at a minimum. The accuracy of references is determined by line regulation and temperature drift performance. Load regulation is sometimes included in the accuracy but is more appropriately specified for voltage regulators. Accuracy performance is sometimes limited by the effects of the package on the output voltage. The causes of this phenomenon are the physical stresses induced on the die by the package. As a result, the physical location of the reference with respect to the overall chip is important. Package induced drifts can be significant especially if trimming is performed at the wafer level. The performance can be improved if trimming is done at the post-package level. Lower dynamic range, a consequence of low voltage operation, demands that reference voltages be more accurate; as a result, bandgaps require curvature correcting schemes. Lower dynamic range results from reductions in power supply voltage, which decreases signal-to-noise ratio in an environment where the noise floor typically remains constant [10].

2.6 Summary

The electrical design considerations and implications of the system have been addressed in this chapter. The frequency and transient response have been analyzed when the system is under typical loading conditions. Their effects on design have been

identified to fully understand the basic performance limitations of the regulator. The consequential requirements of the major circuit blocks were then discussed. This included comments of the parasitic effects of each block on the overall performance. The chapter, in essence, established a conceptual background for evaluating the prevailing circuit topologies.

CHAPTER III

REGULATOR TOPOLOGIES

The circuit architecture of a basic low drop-out regulator can take various forms. The design criterion for each implementation is determined by the specific application as well as by the process technology where the circuit is to be fabricated. However, they all have to function under similar loading conditions, namely, a load-current, an output capacitor and its associated electrical series resistance (ESR), and some bypass capacitors. Several of the prevailing design approaches are scrutinized in this chapter. Each structure is evaluated for its current efficiency and overall performance at low voltage. Moreover, some performance enhancing techniques are also illustrated and evaluated.

3.1 CMOS Topology

Figure 3.1 shows the circuit implementation of a CMOS low drop-out regulator [23]. The feedback amplifier has a single dominant pole and is located at its output, the gate of the output device Mpo (node "A"). The error amplifier is a single, class AB gain stage with a PMOS differential input pair. The class AB gain stage yields a rail-to-rail output voltage swing. Consequently, the power PMOS transistor can be shut off completely as well as be maximally driven to a gate drive approximately equal to the

input voltage, $0 \le V_{sg} \le V_{in}$. The input voltage (V_{in}) for this circuit is limited by the common mode range characteristics of the same,

$$V_{in} \ge V_{ref} + V_{sg} + V_{sd}, \tag{3.1}$$

where V_{ref} is the reference voltage. For the case of an n-type input pair realization, the reference voltage is limited to be greater than or equal to $V_{gs} + V_{ds}$ while the input voltage of the circuit is limited to be greater than $V_{sg} + 2V_{ds}$. Furthermore, the input voltage requirement of the reference ($V_{in\text{-}ref}$) in the latter case would be at least one V_{sd} above the reference voltage, in other words,

$$V_{in-ref} \ge V_{sd} + V_{ref} \ge V_{sd} + V_{gs} + V_{ds} \approx V_{gs} + 2V_{ds}. \tag{3.2}$$

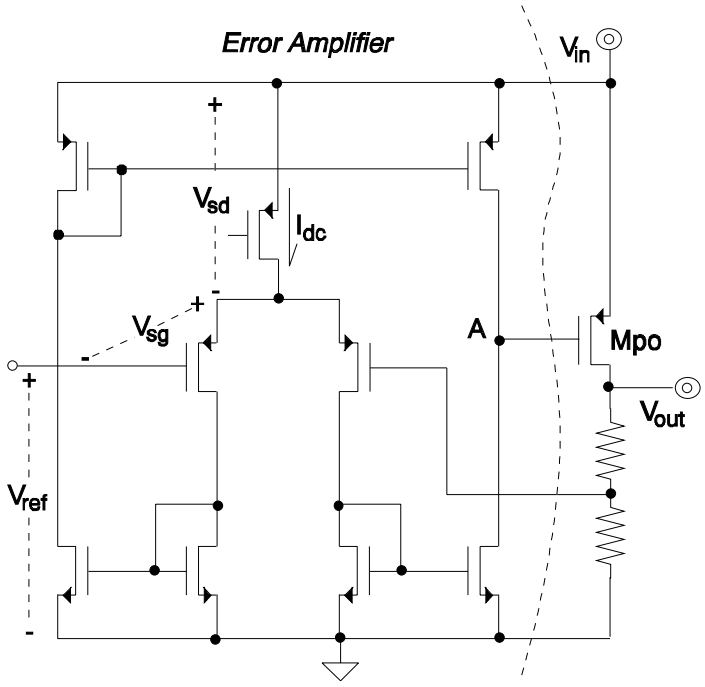

Figure 3.1. CMOS low drop-out regulator topology.

As a result, the input voltage restriction using an NMOS differential pair is dominated by the requirements of the reference and not the regulating loop.

The frequency response of this circuit is typical to most low drop-out regulator topologies. Under loading conditions, there are three poles and one zero, namely, the pole associated with the output capacitor, the pole introduced by the bypass capacitors, the parasitic pole at the output of the error amplifier, and the zero associated with the ESR of the output capacitor. The parasitic pole (P_3 from previous analysis) is the dominant pole of the feedback amplifier. The design reaps the benefits of not having any other significant poles in the amplifier. All the non-dominant poles of the amplifier are at low impedance nodes and therefore reside at high frequencies. Such architecture, however, still necessitates careful design because the dominant pole of the amplifier can easily be at low frequencies. This results from the characteristic high input capacitance of Mpo and the high output impedance of the amplifier. The capacitance can be in the order of 100s of pico farads since the size of Mpo is significantly large, which is a necessary trait for providing high output currents.

The circuit is not inherently current efficient. The bias current of the amplifier is dependent on the slew-rate performance of the same. For instance, the system may require a time response of 2 μs with a voltage swing at node "A" of 800 mV (gate voltage swing of Mpo) to react to a maximum load-current step change. Hence, the amplifier must charge and discharge node "A" with roughly 40 to 160 μA, assuming a gate capacitance of 100 to 400 pF. This places a significant lower limit on the bias current flow of the amplifier during zero load-current conditions, in other words, limit on current efficiency and battery life.

3.2 Buffered Architecture

Figure 3.2 illustrates a topology that isolates the dominant pole of the amplifier from the input terminal of the power pass device. The implementation is intended for a series Darlington PNP pass transistor [29]. The basic topology is formed by a simple single stage amplifier cascaded onto a buffer driving the pass element. During low load-current conditions, the base current of the Darlington PNP structure is low. As a result, the bias current flows mostly through Mp1 and the resistor between the gate and the source of Mn1. At this point, the gate voltage of Mn1 is not high enough to significantly cause Mn2 to conduct current. During high load-current conditions, however, the base current of the Darlington becomes large. As a result, the voltage at the gate of Mn1 becomes large enough to notably turn Mn2 on, whose drain current is a nonlinear mirror ratio of Mn1. Hence, the current sinking capabilities of the buffer are increased as the load-current increases. The overall low voltage limit of the circuit is dominated by the buffer,

$$V_{in} \geq 2V_{sd} + 2V_r + V_{gs}. \tag{3.3}$$

This presents a possible source of concern when single alkaline battery cells (0.9 to 1.5 V) are considered. Thus, the design is not optimum for low voltage.

On the other hand, the circuit benefits from having a good frequency response. This arises as a result of isolating the highly capacitive node (the pass device's input) from the highly resistive gain stage output (the dominant pole of the amplifier). This is done by the buffer, which provides a low impedance for the highly capacitive node and a low capacitance for the highly resistive node. Therefore, the poles at the two nodes can

be at higher frequencies than the single pole of the unbuffered version, a sample of which is embodied in the circuit of Figure 3.1. Consequently, the overall frequency response of the system exhibits higher phase margin and potentially higher bandwidth. In other words, the concept of buffering allows for faster response times, which translate to lower output voltage variations and higher accuracy.

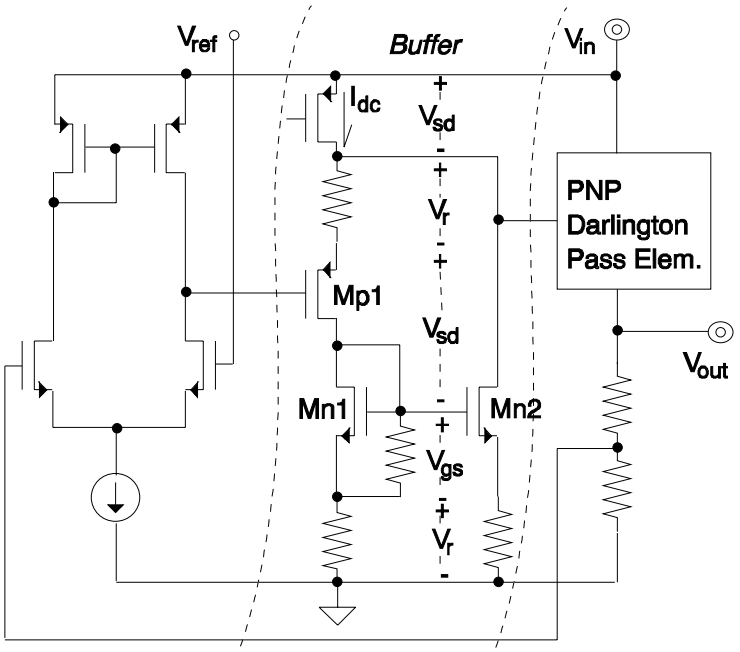

Figure 3.2. Buffered low drop-out regulator architecture.

3.3 All-in-one Approach

The reference and amplifier can be integrated into one circuit as shown in Figure 3.3, which is a modified version of the original circuit of [22] and whose concept is also used by some Analog Devices' parts [4]. The main idea, like before, revolves around defining the regulated voltage at the output and feeding back an error signal to control the pass device. However, instead of using a differential amplifier and a separate reference circuit, a first order bandgap is realized within the feedback circuit itself. The bandgap,

defined at the output, feeds back an error signal through a single common emitter gain stage back to the pass device. In essence, a voltage reference circuit with good load regulation characteristics is realized. Transistor Qn1 and resistor R_1 define the bandgap reference where the voltage across R_1 is proportional-to-absolute temperature (PTAT). Since the regulated output is a first order bandgap, the output voltage range does not have any flexibility in terms of magnitude adjustment and the minimum input voltage is defined by a bandgap and one saturation voltage, V_{bg} and V_{sd},

$$V_{in} \geq V_{bg} + V_{sd} \approx 1.4 - 1.5 \text{ V}. \tag{3.4}$$

This is a problem for single, low voltage battery cells whose voltages range from 0.9 to 1.5 V. The overall circuit can also be realized in a CMOS environment where the bandgap voltage can be generated by either using the bipolar parasitic transistor innate to the process or by using the temperature dependencies of different MOS devices [30, 31].

The frequency response of the circuit in Figure 3.3 is similar to that of Figure 3.1, which is characteristic to a single pole error amplifier. As a result, caution must be

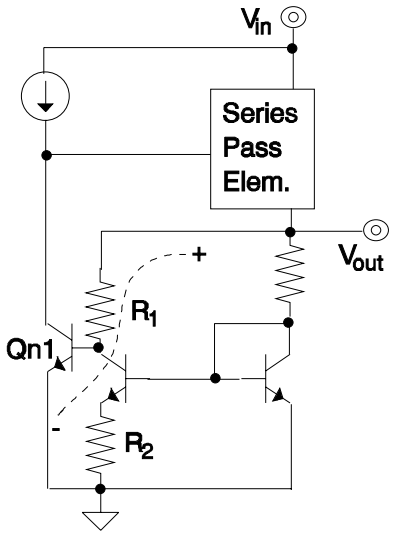

Figure 3.3. All-in-one regulator approach.

exercised to prevent this pole, parasitic pole of the system, from dropping to lower frequencies. This is done to yield good system bandwidth and phase margin. The topology enjoys the benefits of high current efficiency and low active chip area. This arises from a low component count. As a result, the number of current sensitive transistor paths to ground is low thereby exhibiting low quiescent current flow (high current efficiency) and relatively long battery life.

Another class of linear regulators are those that are internally compensated. These typically use some form of miller compensation to make an internal node the dominant pole of the system, such as the input node of the pass device (gate or base). Consequently, the pole associated with the output capacitor has stringent requirements, i.e., frequency location needs to exceed a specified value. Thus, the output capacitors for these regulators are smaller than externally compensated versions. The maximum specified output current is therefore lower for internally compensated linear regulators. This is the consequence of larger transient output voltage variations resulting from smaller output capacitors ($\Delta V_{tr\text{-}max} \propto 1 / C_o$). In summary, these regulators inherently yield lower output currents while exhibiting different frequency response characteristics and requirements.

Table 3.1 shows a qualitative comparison of the design approaches discussed. Internally compensated regulators are excluded because of their output current limitations. The lowest minimum input voltage is achieved by the CMOS topology. The buffered architecture offers the best frequency and transient response. The all-in-one approach achieves the best current efficiency and lowest active area. Unfortunately, the latter approach suffers from stringent input and output voltage range problems. Consequently, a combination of the former two designs can yield the best performance at

low voltage, i.e., circuit architecture similar in nature to that of the CMOS topology with a buffer between the amplifier and the pass device.

Table 3.1. Qualitative evaluation of regulator topologies.

Parameter	CMOS	Buffered	All-in-one
$V_{in\text{-}min}$	Good	Medium	Medium
Current Efficiency	Medium	Medium	Good
System Bandwidth	Medium	Good	Medium
Active Area	Medium	Medium	Good

3.4 System Enhancements

The circuit architecture of the regulators discussed in the previous section can be complemented with some system level performance enhancing techniques. Some of the attributes that can be ameliorated are maximum output current, response time, and output voltage range. However, the benefits arise at some cost, such as active area and/or current efficiency. Some of these techniques are introduced and evaluated for their performance and applicability in the portable electronics market, which demands low voltage and high current efficiency.

Mixed-mode Technique

The benefits of analog and digital operation can be combined to yield improved performance. Figure 3.4 illustrates one sample topology, which is a conceptual version of [32]. The analog section operates like most standard regulator topologies. The additional digital loop uses a feedback amplifier, similar to that of the analog section, to drive a digital inverter. Consequently, Mpod in Figure 3.4 sources a digital current that

is dependent on the output voltage, a sense voltage that reflects load-current behavior. During low load-current conditions, the analog section sources all of the current. During high load-current conditions, however, the digital section sources a constant current that is lower in magnitude than the load-current. At this point, the analog feedback loop regulates the output voltage around the digital current through current I_a ($I_a = I_{Load} - I_d$). If the analog current component becomes zero and the digital current exceeds the load-current, then Mpod is shut off by the digital feedback path. As a result, the operation goes back to the low load-current state where the analog section is the sole supplier of output current.

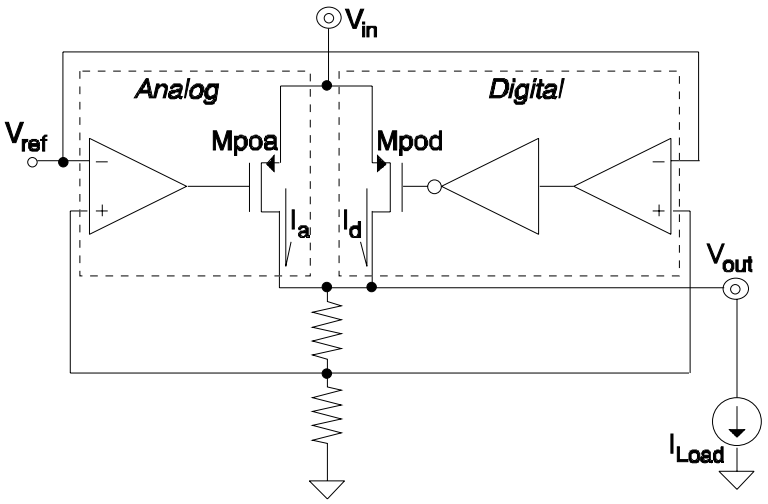

Figure 3.4. Mixed-mode regulator.

The advantage of the digital section is that it consumes less power (less quiescent current). The feedback amplifier in the digital section only drives the input capacitance of one inverter and not the large output PMOS transistor (Mpod). Thus, the slew-rate current performance of the amplifier is relaxed. Furthermore, the size of the output device in the analog section (Mpoa) is not as large as it would be had it been the only

power element. Consequently, the performance requirements of the amplifier in the analog feedback are relaxed. Moreover, the response time versus the quiescent current tradeoff is positively offset by the fast parallel digital signal path. However, caution must be exercised in designing the output voltage swing of the inverter for varying input voltages. If a simple inverter is used to work properly at 2 V, then the digital section would deliver an excessive amount of current at an input voltage of 10 V, corresponding to a gate drive increase from 2 to 10 V. This gate drive problem can be handled by designing the inverter as shown in Figure 3.5, which adds a drain-grounded PMOS device in series with the pull down transistor of an inverter as implemented by [32]. Unfortunately, the inverter realization is detrimental for operation at input voltages of 0.9 to 1.5 V because of voltage headroom problems, consequence of multiple series diode connected devices.

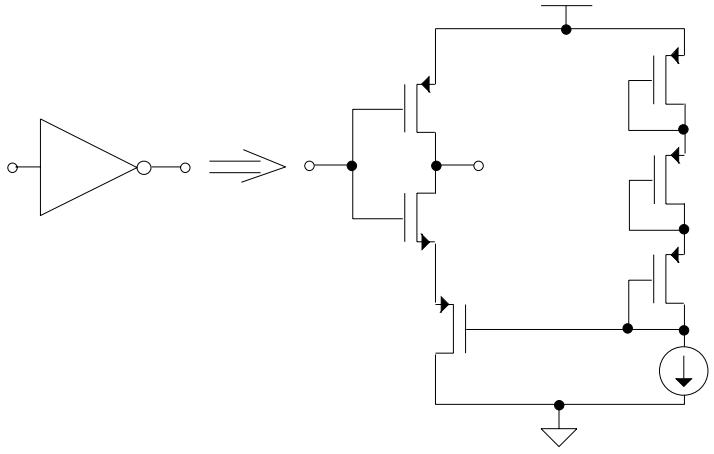

Figure 3.5. Digital inverter for the mixed-mode regulator.

Multi-pass Device Approach

A similar way of relaxing the output current requirement of a regulator is by adding another pass device that delivers a mirror ratio of the main output PMOS

transistor. Figure 3.6 illustrates one such topology realized by [33]. The current through the main output PMOS device (Mpo) is sensed and a mirror ratio is supplied by the additional pass device (Mpx). The mirror ratio is controlled by the resistor ratio of R_1 and R_2, one-tenth for Figure 3.6. The current control is accomplished by the PNP transistors and the load resistor R_{L1}. The voltage across R_2 is forced onto R_1 and the gate voltage of Mpx is controlled via a negative feedback path from the source to the gate of the same, $V_{gate}/V_{source} \approx g_{m_{pnp}} R_{L1}$. The pole associated with the gate of Mpx must be at high enough frequencies such that the overall system response is not degraded, i.e., the pole requirements are similar to those of a single pole amplifier in a standard regulator topology.

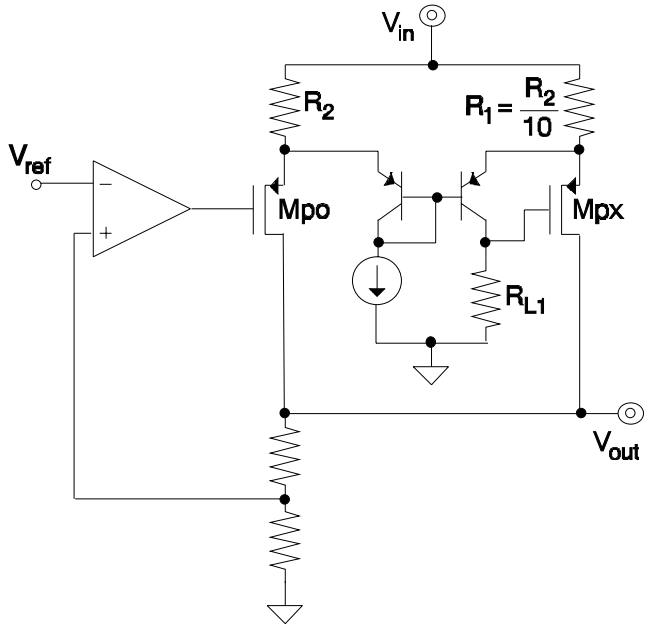

Figure 3.6. Multi-path device regulator.

The demands on the error amplifier in the main feedback are relaxed because the size of the output PMOS transistor is reduced. However, the drop-out voltage is

increased by the series resistance of R_1 and R_2. Thus, these resistors need to have low values to mitigate their negative effects on drop-out voltage. Furthermore, care must be taken in designing the current flowing through the two PNP devices so that current efficiency is not degraded enough to unwarrant the use of the technique. The load resistor R_{L1} could be replaced by a current sink; however, the associated pole tends to go towards lower frequencies and possibly compromise stability when this is done.

Widely Adjustable Structure

The output voltage range of typical low drop-out regulator structures goes from the reference voltage up to approximately 200 mV below the input voltage. Figure 3.7 shows an architecture that extends the output voltage range down to roughly zero volts [34]. This is done by adjusting the voltage at node "A", which is typically connected to ground. As a result, the current flowing through the feedback resistors (I_r) can be manipulated to the point of reversing its direction. Consequently, the output voltage can be defined to be below the reference voltage. Amplifier A_1 is a buffer with a gain slightly greater than one. The second amplifier (A_2) forces a fraction of the reference voltage on node "A". When this fraction is greater than one, then I_r flows towards the output and the output voltage becomes less than the reference voltage,

$$V_{out} = \frac{V_A - V_{ref}}{R_2} R_1 \approx \frac{(k-1)\,V_{ref}}{R_2} R_1, \qquad (3.5)$$

where k is a constant defined by the gain of A_1, the gain of A_2, and the resistor tap of the input of A_2, i.e., $k \approx 0$ - 1.05 in Figure 3.7. A requirement for this structure is that the load-current be greater than or equal to I_r. This can be guaranteed by defining I_r to be small and by placing a constant current sink at the output that is greater than or equal to I_r, as illustrated by the dotted lines in Figure 3.7.

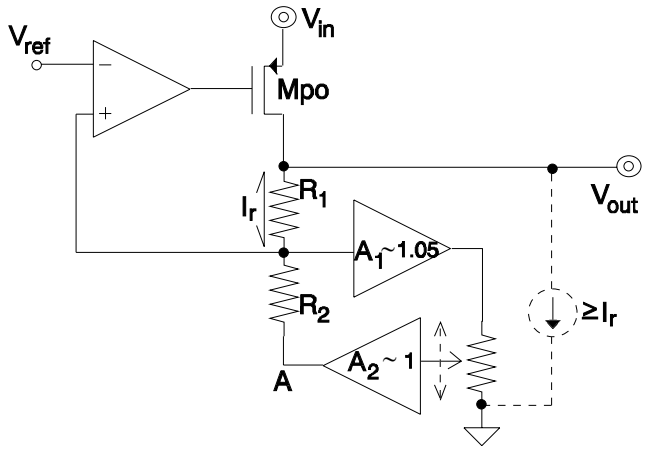

Figure 3.7. Widely adjustable low drop-out regulator structure.

The main disadvantage of the topology lies in current efficiency, in other words, quiescent current flow. The realization of two additional amplifiers comes at the cost of complexity, quiescent current, and active area. The technique is only useful when the application specifically warrants it. Most of the time, integrated circuit applications do not require the characteristics offered by this technique. In low voltage applications, however, this may be necessary if the input and the output voltage of the reference are greater than the input voltage of the regulator. This is a seldom occurrence that may arise during system level design when most of the circuit blocks are realized discretely. At this point, the whole exercise may be circumvented by integrating the reference onto the regulator chip if enough voltage headroom and chip area exist. This comes at the expense of quiescent current and possible design time.

3.5 Summary

This chapter has illustrated some of the prevailing circuit topologies for low drop-out regulators. They embody the basic concepts surrounding LDO design in CMOS,

bipolar, and biCMOS process technologies. The circuits were described and evaluated within the context of low voltage and low quiescent current flow, which are the characteristics demanded by the growing market demand for battery operated products. Moreover, circuit techniques used to enhance particular performance specifications were also described and evaluated. All these approaches constitute the necessary basis for developing new circuit techniques that enable practical and suitable designs for a battery powered environment.

CHAPTER IV

PERFORMANCE ENHANCEMENTS

The general performance of low drop-out regulators deteriorates as input voltages decrease. This has an intrinsic impact on portable, low voltage, and battery operated equipment. Consequently, circuit designs benefit from extensive exploitation of available process technologies. In a battery operated environment, the aspects that need special attention are quiescent current flow, maximum output current capabilities, and regulation performance [35]. Low quiescent current is necessary to maximize current efficiency, which is important during low load-current conditions for prolonged battery life. As the input voltage is decreased, the output current capability of the pass device tends to diminish as a result of voltage headroom degradation. Although these issues are especially important in battery operated products, they are also prevalent in designs for higher input voltages. Consequently, enhancing performance without incurring significant costs in quiescent current or voltage headroom benefit the overall design of LDOs.

4.1 Current Efficiency

Motivation

Current efficiency is an important characteristic of battery powered products. It is defined as the ratio of the load-current and the total battery current drain, which is comprised of the load-current (I_{Load}) and the quiescent current (I_q) of the regulator,

$$\text{Efficiency}_{\text{current}} = \frac{I_{Load}}{I_{Load} + I_q}. \qquad (4.1)$$

Current efficiency determines how much the lifetime of the battery is degraded by the mere existence of the regulator. Battery life is restricted by the total battery current drain. During conditions where load-current is much greater than quiescent current, operation life is essentially determined by the load-current, which is an inevitable characteristic of linear regulators. On the other hand, the effects of quiescent current on battery life are most prevalent during low load-current conditions when current efficiency is low. This condition of low load-currents is the common operating mode of many applications. As a result, current efficiency plays a pivotal role in designing battery powered supply circuits. The two performance specifications that predominantly limit the current efficiency of low drop-out regulators are maximum load-current and transient output voltage variation. They typically require more quiescent current flow for increased performance.

Challenge

Output current and input voltage ranges directly affect the characteristics of the pass element in the regulator, which define the quiescent current requirements of the error amplifier. As the maximum load-current specification increases, the size of the pass device necessarily increases. Consequently, the error amplifier's load capacitance increases. This affects the circuit's frequency performance by reducing the value of the parasitic pole present at the output of the amplifier, pole P_3 from the discussion in

chapter 2. Therefore, phase-margin degrades and stability is compromised unless the output impedance of the amplifier is reduced accordingly. As a result, more quiescent current flow in the buffer stage of the amplifier is required, be it a voltage follower or a more complicated circuit architecture. In a similar manner, low input voltages require that MOS pass device structures increase in size and thus yield the same negative effects on frequency response and quiescent current flow as just described. This is because the gate drive decreases as the input voltages decrease thereby necessitating larger MOS pass elements to drive high output currents.

Further limits to low quiescent current arise from the transient requirements of the regulator, namely, the permissible output voltage variation in response to a maximum load-current step swing. The output voltage variation is determined by the response time of the circuit, the specified load-current, and the output capacitor, as discussed in chapter 2. The worst response time corresponds to the maximum output voltage variation. This time limitation is defined by the closed-loop bandwidth (BW_{cl}) and the slew-rate current (I_{sr}) capabilities of the system. These characteristic requirements become more difficult to realize as the size of the parasitic capacitor (C_{par}) at the output of the feedback amplifier increases, which results from low voltage operation and/or increased output current specifications. As a result, the quiescent current flow of the amplifier's gain stage is limited by a bandwidth minimum while the quiescent current flow of the amplifier's buffer stage is limited by the slew-rate current required to drive C_{par}.

Slew-rate Dependent Boost

The problem of handling an instantaneous load-current stimulus is translated to the slew-rate requirement of driving the pass device. This can be easily resolved by allowing higher quiescent current flow. However, this is not conducive toward the low quiescent current design goal. On the other hand, a cost efficient addendum in the form

of slew-rate dependent bypass switches can be used to enhance the transient capabilities of the system. Figure 4.1 (a) shows one such slew-rate dependent boost circuit. In this case, two normally off switches are added around a unity gain buffer constituting the output stage of the amplifier. The switches conduct significant current only when the amplifier is slewing to the point where a voltage difference across the unity gain buffer develops to be large enough to turn either of the MOS devices on.

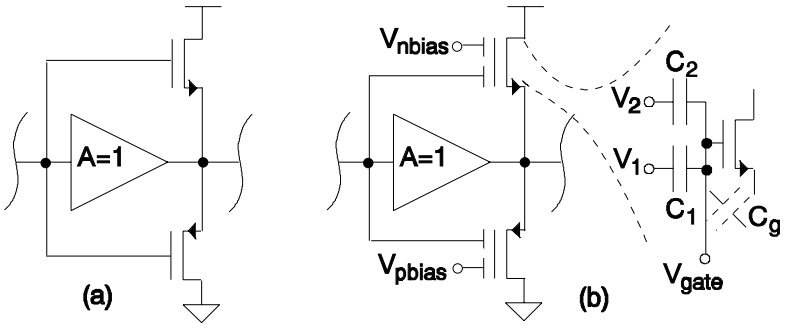

Figure 4.1. Slew-rate dependent boost circuit.

The ability to aid during slew-rate conditions, however, is limited by the large threshold voltage of the switches. Improved performance can be achieved if the threshold voltage (V_{th}) of these bypass transistors were lower, i.e., 0.25 - 0.5 V. This can be accomplished by forward biasing the source to bulk voltage (V_{sb}), for the case of a PMOS transistor, as dictated by the well known threshold voltage equation,

$$|V_{th}| = |V_{to}| + \gamma\left[\sqrt{2|\phi_f| - V_{sb}} - \sqrt{2|\phi_f|}\right], \tag{4.2}$$

where $|V_{to}|$ is $|V_{th}|$ at $V_{sb} = 0$, γ is the body bias coefficient, and $|\phi_f|$ is the bulk Fermi potential [36, 37]. The complement of this can be done for the NMOS transistor case. The access to the bulk terminal of the NMOS device, however, is dependent on process

technology. For instance, access cannot be obtained in a vanilla CMOS process because the bulk is the substrate of the chip. However, the opposite is true for twin well and biCMOS processes where access can be obtained by isolating the NMOS with a p-well, p-base diffusion, or a p-epi region insulated by a ring of deep n+ collector plug and a buried layer.

Another method of adjusting the threshold voltage is through the use of a double gate MOS device [38]. Figure 4.1 (b) shows the resulting scheme. The voltage at the floating gate (V_g), assuming that the source is grounded, is dictated by

$$V_g = \frac{V_1 C_1}{C_{total}} + \frac{V_2 C_2}{C_{total}}, \tag{4.3}$$

thus

$$V_{th1} = \frac{V_{th} C_{total}}{C_1} - \frac{V_2 C_2}{C_1}, \tag{4.4}$$

where V_1 and V_2 are the voltages at terminals one and two, C_{total} is $C_1 + C_2 + C_g$, V_{th1} is the effective threshold voltage of terminal one, and V_{th} is the threshold voltage seen at the floating gate. As a result, proper capacitor ratios can yield lower effective threshold voltages, i.e., if $C_1 = C_2 = 8C_g$, $V_2 = 1.0$ V, and $V_{th} = 0.7$ V then $V_{th1} = 0.49$ V. The disadvantage of this technique lies in generating the necessary bias voltages, V_{nbias} and V_{pbias} in Figure 4.1 (b), for maintaining the same effective threshold voltage over specified input voltage and load-current ranges. This is because the voltage at the source of the MOS bypass transistors is sensitive to the gate drive of the p-type pass device of the linear regulator, which is dependent on input voltage and output current.

Current Efficient Buffer

Another topology that achieves good current efficiency performance is illustrated in Figure 4.2. The operation is based on sensing the output current of the regulator and feeding back a ratio of the same to the slew-rate limited node of the circuit. Transistor Mps sources a fraction of the current flowing through the output transistor Mpo. During low load-current conditions, the current fed back (I_{boost}) is negligible thereby yielding high overall current efficiency and not aggravating battery life. Consequently, the current through the emitter follower is simply I_{bias} when load-current is low. During high load-current conditions, the current through the emitter follower is increased by I_{boost}, which is no longer negligible. The resulting increase in quiescent current flow has an insignificant impact on current efficiency because the load-current is, at this point, much greater in magnitude. However, the increase in current in the buffer stage aids the circuit by pushing the parasitic pole at its output (P_3) to higher frequencies and by increasing the current available for slew-rate conditions. Thus, the biasing conditions for the case of zero load-current can be designed to utilize a minimum amount of current, which yields maximum current efficiency and prolonged battery life.

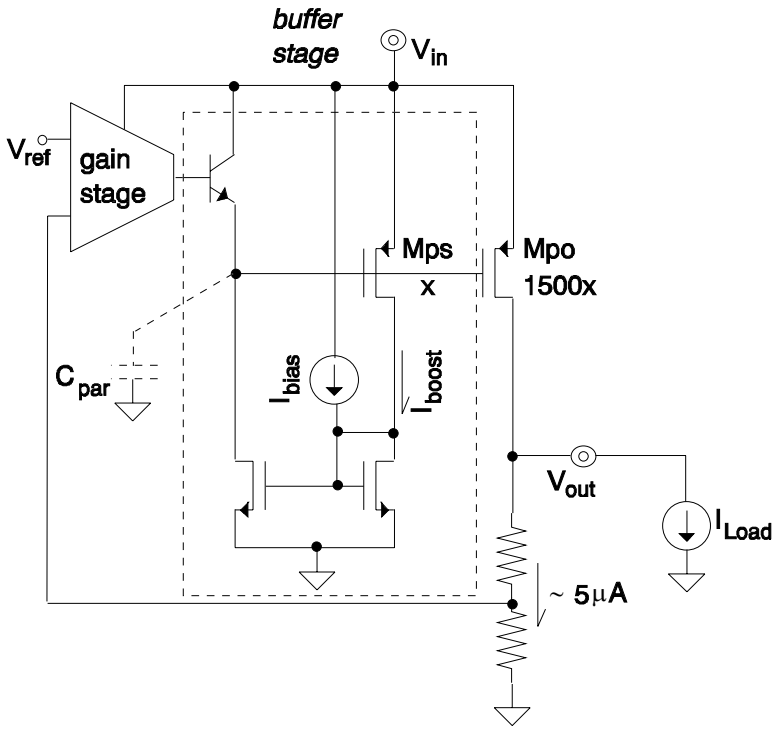

Figure 4.2. Current efficient-transient boost LDO buffer stage.

Frequency Response: The dominant pole of the system is determined by the output capacitor and the output impedance of the pass device, given by P_1 in the ac analysis section of chapter 2. When the load-current is low, the magnitude of this pole is at a minimum. This is because the output impedance of the pass device, which defines the pole for most conditions, is inversely proportional to the current flowing through it,

$$P_1 \approx \frac{1}{2\pi R_{o-pass} C_o} \approx \frac{\lambda I_{Load}}{2\pi C_o}, \tag{4.5}$$

where C_o is the output capacitance, $R_{o\text{-}pass}$ is the output resistance of Mpo in Figure 4.2, λ is the channel length modulation parameter, and I_{Load} is the load-current. Consequently, the unity gain frequency (UGF) is at low frequencies when the load-

current is low, which relaxes the requirement of the parasitic pole P_3 (defined by the input capacitance of the pass device and the output impedance of the error amplifier) to be approximately greater than or equal to the minimum unity gain frequency (UGF_{min}). This corresponds to a phase margin of approximately 45 to 90 ° with the following design equation,

$$P_{3_{no-load-current}} \approx \frac{g_{m_{npn}}}{2\pi C_{par}} = \frac{I_{bias}}{2\pi V_t C_{par}} \geq UGF_{min}, \tag{4.6}$$

where $g_{m_{npn}}$ is the transconductance of the emitter follower and V_t is the thermal voltage.

As load-current increases, however, the dominant pole increases linearly and consequently so does the UGF. The open-loop gain (A_v) is inversely proportional to the square root of the load current,

$$A_v \approx A_{amp}\, g_{mp}\, R_{o-pass} \propto \frac{\sqrt{I_{Load}}}{I_{Load}} = \frac{1}{\sqrt{I_{Load}}}, \tag{4.7}$$

where A_{amp} is the gain of the error amplifier while g_{mp} and $R_{o\text{-}pass}$ are the transconductance and the output resistance of the pass device respectively. Since the dominant pole (P_1) increases faster than the gain decreases with load-current, the unity gain frequency increases as the load-current increases (equations (4.5) and (4.7)). These consequential effects of load-current on frequency response are graphically illustrated in Figure 4.3. Therefore, the parasitic pole (P_3) is also required to increase with load-current, which is achieved by the load dependent boost current. This is apparent from the following equation,

$$P_3 \approx \frac{g_{m_{NPN}}}{2\pi C_{par}} = \frac{I_{bias} + I_{boost}}{2\pi V_t C_{par}} \approx \frac{I_{bias} + kI_{Load}}{2\pi V_t C_{par}}, \tag{4.8}$$

where k corresponds to a constant mirror ratio, i.e., 1/1500 for Figure 4.2. The circuit can be designed such that P_3 increases at a faster rate than the UGF with respect to load-current. This results in the following relation,

$$P_{3-rate} = \frac{\partial P_3}{\partial I_{Load}} \approx \frac{k}{2\pi V_t C_{par}} \geq P_{1-rate} \approx \frac{\lambda}{2\pi C_o} > UGF_{rate} \tag{4.9}$$

or

$$k \geq \frac{\lambda V_t C_{par}}{C_o}, \tag{4.10}$$

where $P_{3\text{-rate}}$, $P_{1\text{-rate}}$, and UGF_{rate} are the rates with respect to load-current of pole P_3, pole P_1, and the unity gain frequency respectively. Thus, current efficiency can be maximized to accommodate the load dependent requirements of P_3. If the load dependence of P_3 is not incorporated into the circuit, then more current than necessary is used during low load-current conditions. The frequency response behavior was confirmed by simulations.

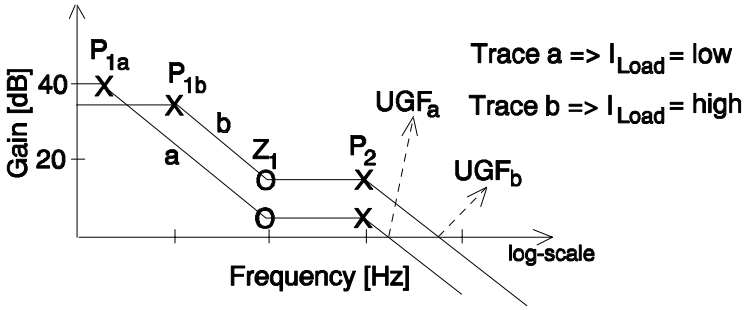

Figure 4.3. System frequency response as a function of load-current.

Transient Response: The circuit of Figure 4.2 exhibits the transient response illustrated in the transient analysis section of chapter 2 where a maximum load-current step swing is applied to the load. One of the parameters that determines the maximum output voltage variation is the response time (Δt_1) required for the system to react. However, the slew-rate current (I_{sr}), which partially determines Δt_1, is not constant for the circuit proposed, $I_{sr} = I_{bias} + kI_{boost}$. As a result, a slew-rate condition does not fully describe the operation of the circuit at hand. During a load-current transition from zero to maximum value, the response time of the circuit is dominated by the bandwidth of the system and the transient response of the buffer stage. In particular, the response time is composed of the time required for the amplifier to respond (t_{amp}), for the sense PMOS transistor (Mps) to start conducting current ($t_{Mps\text{-}on}$), for the positive feedback circuit to latch up ($t_{latch\text{-}up}$), and for the output PMOS device (Mpo) to conduct the load-current (t_{Mpo}). This is illustrated in

$$\Delta t_1 \approx t_{amp} + t_{Mps-on} + t_{latch-up} + t_{Mpo} \approx \frac{1}{BW_{cl}} + t_{Mps-on} + t_{latch-up}, \qquad (4.11)$$

where BW_{cl} is the closed-loop bandwidth of the system (approximately $(t_{amp} + t_{Mpo})^{-1}$).

The composite buffer stage is essentially a localized positive feedback circuit. The system is stable because the positive feedback gain is less than one. Consequently, the circuit attempts to latch up until the output transistor is fully turned on; at which point, the error amplifier forces the circuit back into the linear region. As a result, the performance tradeoffs between the slew-rate and the quiescent current requirements of typical LDOs are circumvented. For instance, if the parasitic capacitance (C_{par}) is 200 pF, the voltage change required for the output PMOS transistor (ΔV_{sg}) is 0.5 V, the closed-loop bandwidth of the system is 1 MHz, and the response time (Δt_1) is confined to

be less than 5 μs, then the slew-rate current ($I_{sr} = I_{bias}$) required for a class A buffer is approximately 25 μA (equation (2.11)). For the case of the circuit of Figure 4.2, a dc current bias (I_{bias}) of only 1 μA can provide the same performance. The dominant factor of Δt_1 is the time required for the sense transistor Mps to go from being off to sub-threshold and finally to strong inversion. Figure 4.4 illustrates the simulation results showing the effects of the

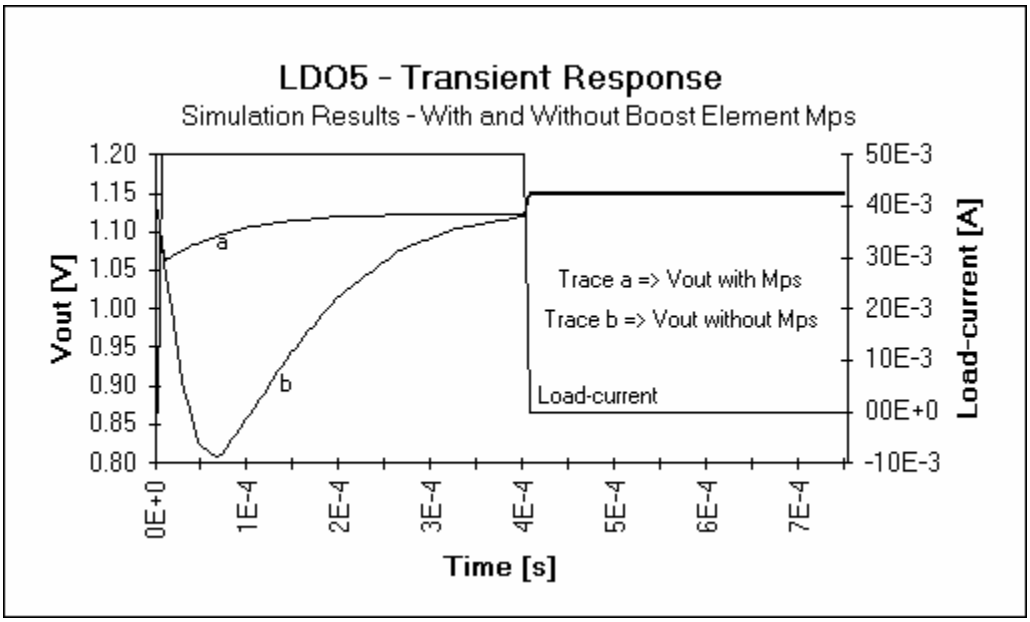

Figure 4.4. LDO output voltage variation with and without the boost element Mps in the current efficient buffer stage.

presence of the boost element Mps, in the circuit shown in Figure 4.2, on the output. It is observed that the output voltage variation is decreased as a result of a reduction in response time. This, however, does not come at the expense of additional quiescent current flow during zero load-current conditions thereby achieving maximum current efficiency and battery life.

4.2 Current Boosting

Motivation

Operation at low voltages is intrinsic in the battery operated products market. This is driven by the public demand for compactness and finer fabrication lithography. Thus, area efficient circuits and lower breakdown voltages necessitate the use of single, low voltage battery cells, i.e., 0.9 to 1.5 V. This limitation, however, could be eliminated from the low drop-out (LDO) regulator by utilizing a dc-dc converter, switching regulator. Consequently, the dc-dc converter needs to be operable at low voltages. In other words, the problem is simply transposed to the dc-dc converter. Hence, the problem of low voltage cannot be avoided and must be handled at either the LDO or dc-dc converter level. The two main limitations of low voltage operation lie in the output current capabilities of the pass device (power switch) and voltage headroom.

Challenge

As the power supply voltages decrease, the gate drive available to the PMOS pass device decreases. As a result, the aspect ratio of the power transistor must be increased to provide acceptable levels of output current. However, the parasitic gate capacitance also increases as the size of the PMOS transistor increases. This constitutes an increase in C_{par} of Figure 4.2, which pulls its associated parasitic pole (P_3) down to lower frequencies. Consequently, the phase margin of the system is degraded and stability may be compromised. This presents a problem when working in a low quiescent current environment.

Composite Output Transistor

One way to improve gate drive without increasing input voltage or device size is by forward biasing the source to bulk junction of the PMOS pass device. This results in a reduction in threshold voltage, commonly referred as the bulk effect phenomenon. The

threshold voltage (V_{th}) is described by equation (4.2). Consequently, the threshold voltage decreases as V_{sb} increases thereby effectively increasing the gate drive of the power PMOS transistor (pass device). This, in turn, permits the transistor to conduct more current under a given input voltage.

Maximum Output Current: For comparative analysis, the maximum current can be observed at the region where the power PMOS device is in saturation, which corresponds to non drop-out conditions. The corresponding drain current (I_{sd}) of the device is

$$I_{sd} \approx \frac{K_p W}{2L}\left[V_{sg}-V_{th}\right]^2 \approx \frac{K_p W}{2L}\left\langle V_{sg}-|V_{to}|-\gamma\left[\sqrt{2|\phi_f|-V_{sb}}-\sqrt{2|\phi_f|}\right]\right\rangle^2, \quad (4.12)$$

where K_p is the transconductance parameter of a PMOS transistor. Maximum output current results when the gate drive is at its peak, which occurs when the source to gate voltage (V_{sg}) is equal to the input voltage (V_{in}). Thus, if K_p is 15 $\mu A/V^2$, $|V_{to}|$ is 0.9 V, W/L is 30 kμm/μm, and V_{in} is 1.2 V, then the maximum output current ($I_{o\text{-}max}$) is 20 mA when the source to bulk junction is not forward biased. However, if the source to bulk junction is forward biased by 0.3 V, then $I_{o\text{-}max}$ is 38.5 mA (assuming that γ is 0.5 $V^{1/2}$ and $2|\phi_f|$ is 0.6 V). As a result, the output current capability of a PMOS device can be significantly increased by simply forward biasing the source to bulk junction. Figure 4.5 illustrates how this technique performs on the prototype circuit of Figure 4.2 where the aspect ratio of the power PMOS transistor is 2 kμm/μm. A battery is placed between the source and bulk of the output PMOS device and the load-current (I_{Load}) is swept from 0 to 500 μA. For the same input voltage, the maximum output current capability is increased as V_{sb} is increased, in other words, the circuit stays in regulation for an

increased load-current range. At a forward biased junction voltage of 0.3 V, the output current is more than doubled compared to its non-forward biased state.

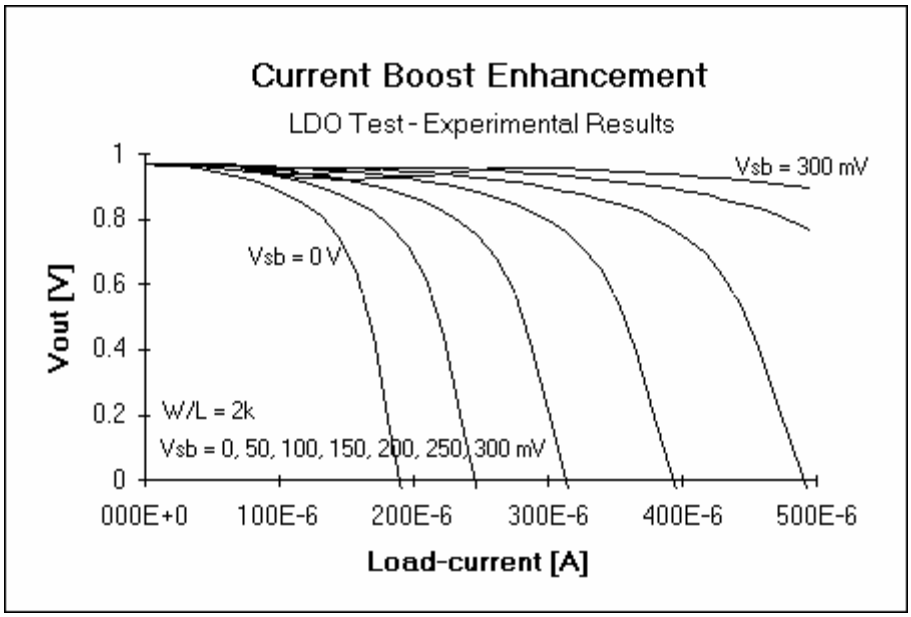

Figure 4.5. Maximum load-current performance of the current boost enhancement.

Figure 4.6 illustrates a successful implementation of the technique in a low drop-out regulator, a technique that could easily be extended to dc-dc converters. The forward biased junction is defined by the voltage drop across the schottky diode (Ds). This voltage drop has to be less than a base-emitter voltage to prevent the parasitic vertical PNP transistors of the power PMOS device (Mpo) from turning on and conducting notable ground current through the substrate via the well. The effects of the parasitic bipolar transistors are mitigated by placing a heavily doped buried layer underneath the well of the power PMOS transistor and/or by increasing the size of the schottky diode. However, the ability to shut off Mpo is not degraded since the forward bias voltage is a function of load-current. This is similar to the operation of the current efficient circuit of Figure 4.2. Thus, I_{boost} is low and V_{sb} is close to zero at low load-currents. At high

load-currents, however, I_{boost} and V_{sb} increase thereby decreasing the threshold voltage and increasing the effective gate drive of the output PMOS device.

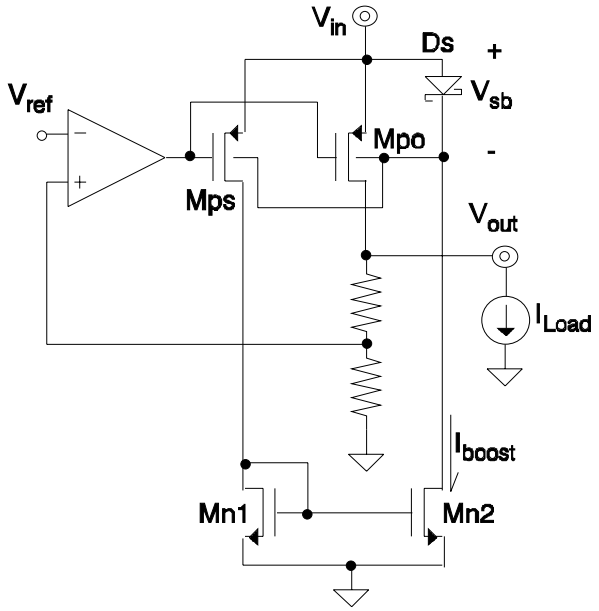

Figure 4.6. LDO with current boosting capabilities.

Drop-out Voltage: The method of forward biasing the source to bulk junction also yields lower drop-out voltages. In other words, the "on" resistance of the pass device (Mpo) is reduced. When the regulator is in drop-out, Mpo is characteristically in the triode region and exhibits the well known current relationship of

$$I_{sd} \approx \frac{K_p W}{2L}\left\langle\left[V_{sg} - V_{th}\right]V_{sd} - V_{sd}^2\right\rangle \approx \frac{K_p W}{2L}\left[V_{sg} - V_{th}\right]V_{sd}. \qquad (4.13)$$

This current relationship can be manipulated to derive the "on" resistance (R_{on}) of the PMOS device to be approximately

$$R_{on} \approx \frac{V_{sd}}{I_{sd}} \approx \frac{2L}{K_p W} \cdot \frac{1}{\left[V_{sg} - V_{th}\right]} \approx \frac{2L}{K_p W} \cdot \frac{1}{\left\langle V_{sg} - |V_{to}| - \gamma\left[\sqrt{2|\phi_f| - V_{sb}} - \sqrt{2|\phi_f|}\right]\right\rangle} \quad (4.14)$$

or the drop-out voltage (V_{do}) to be

$$V_{do} \approx R_{on} I_{Load} \approx \frac{2L}{K_p W} \cdot \frac{I_{Load}}{\left\langle V_{sg} - |V_{to}| - \gamma\left[\sqrt{2|\phi_f| - V_{sb}} - \sqrt{2|\phi_f|}\right]\right\rangle}. \quad (4.15)$$

Therefore, if K_p is 15 μA/V^2, $|V_{to}|$ is 0.9 V, W/L is 30 kμm/μm, V_{in} is 1.2 V, and I_{Load} is 20 mA, then the drop-out voltage is 296 mV (corresponding to 14.8 Ω) when the source to bulk junction is not forward biased. However, if the source to bulk junction is forward biased by 0.3 V, then V_{do} becomes 216 mV (corresponding to 10.8 Ω) assuming that γ is 0.5 V$^{1/2}$ and $2|\phi_f|$ is 0.6 V. There is a theoretical improvement of approximately 27 %. Figure 4.7 illustrates the effects of forward biasing the source to bulk junction on the

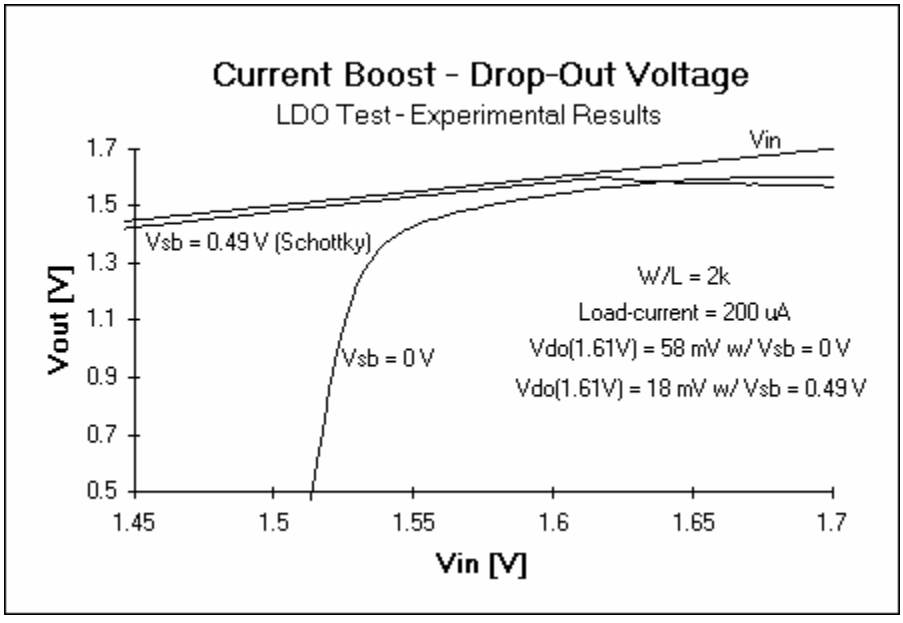

Figure 4.7. Drop-out voltage performance of the current boost topology.

drop-out performance of the prototype circuit of Figure 4.6 where the aspect ratio of Mpo is 2 kμm/μm. There is an experimental improvement of roughly 67 % with a forward bias voltage of 0.49 V.

Frequency Response: During low load-current conditions, the current through the sense transistor (Mps) and consequently the current through the schottky diode (Ds) is negligible. This is because of the high mirror ratio of the output and the sense transistor, Mpo and Mps in Figure 4.6. However, Mps and Ds start conducting appreciable currents at higher load-currents. Therefore, these elements constitute another ac signal path for the system. The effect of this path manifests itself through g_{mp} in the open-loop gain, as seen in equation (2.1). The effective transconductance of the composite pass device of the circuit in Figure 4.6 can be described as

$$g_{mp} \approx g_{m-o} + \frac{g_{mx}\, r_d\, g_{mb-o}}{\left[1 + s r_d C_b\right]} \leq g_{m-o} + g_{mx}\, r_d\, g_{mb-o}, \tag{4.16}$$

where $g_{m\text{-}o}$ is the transconductance of Mpo, r_d is the resistance of diode Ds, C_b is the total bulk capacitance of Mpo and Mps, $g_{mb\text{-}o}$ is the channel conductance of the bulk of Mpo,

$$g_{mb-o} = \frac{\partial I_{sd}}{\partial V_{sb}} \approx \frac{K_p W}{L}\left[V_{sg} - V_{th}\right] \cdot \frac{\gamma}{2\sqrt{2\left|\phi_f\right| - V_{sb}}} = g_{m-o} \cdot \frac{\gamma}{2\sqrt{2\left|\phi_f\right| - V_{sb}}}, \tag{4.17}$$

and g_{mx} is

$$g_{mx} = \frac{g_{m-s} g_{m-n2}}{g_{m-n1}}, \tag{4.18}$$

where $g_{m\text{-}s}$, $g_{m\text{-}n1}$, and $g_{m\text{-}n2}$ are the transconductances of Mps, Mn1, and Mn2 respectively. As a result of the high mirror ratio between Mpo and Mps, the effective transconductance of the PMOS pass device (g_{mp}) is virtually unaffected by the current boosting technique, $g_{mp} \approx g_{m\text{-}o}$. This can be illustrated by assuming that Mn1 and Mn2 have a 1:1 mirror ratio, W/L_s is 20 μm/μm, I_{Load} is 50 mA, and W/L_o is 30 kμm/μm; the effective transconductance of the composite PMOS device is roughly $g_{m\text{-}o}$ (1 + 0.05) at dc, where $r_d \approx V_t / I_{diode}$, $K_p = 15\ \mu A/V^2$, $\gamma = 0.5\ V^{1/2}$, $2|\phi_f| = 0.6$ V, and $V_{sb} = 0.3$ V.

4.3 Load Regulation

Challenge

Load regulation is limited by the frequency response of a typical low drop-out regulator architecture under loading conditions. Load regulation is defined as the output voltage variation resulting from a unit load-current change, which is equivalent to the output resistance of the regulator ($R_{o\text{-}reg}$),

$$R_{o-reg} = \frac{\Delta V_{LDR}}{\Delta I_o} = \frac{R_{o-pass}}{1 + A_{ol}\beta}, \tag{4.19}$$

where ΔV_{LDR} and ΔI_o are the output voltage and the load-current changes respectively, $R_{o\text{-}pass}$ is the output resistance of the pass element, A_{ol} is the open-loop gain of the system, and β is the feedback factor [3]. Thus, load regulation performance is determined by the open-loop gain of the system. Unfortunately, the dc gain is limited by the frequency response of the regulator, as discussed in chapter 2. Frequency analysis shows that there are three poles and one zero, illustrated in Figure 4.8. For a given unity gain frequency (UGF), the magnitude of the system's dc open-loop gain is restricted by the location of the poles and the zero, i.e., 40 dB for the response illustrated in Figure 4.8.

The worst-case condition occurs when Z_1 is at low frequencies and P_2 is at high frequencies, which corresponds to high values of electrical series resistance (ESR) for the output capacitor and low values of bypass capacitance (C_b). The UGF, in particular, is determined by the maximum allowable response time and the frequency range where the parasitic poles of the system reside, such as the internal poles of the error amplifier.

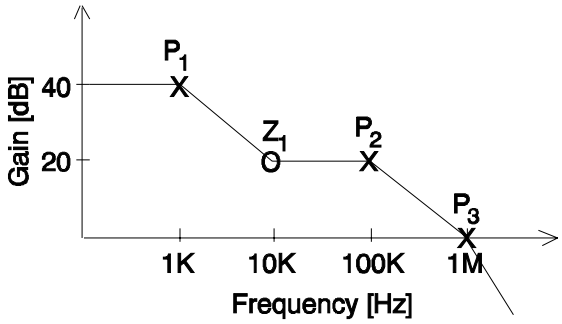

Figure 4.8. Linear regulator frequency response.

Pole/Zero Pair Generation

The dc open-loop gain of the system can be augmented, however, by adding a pole/zero pair as shown in Figure 4.9. For a given unity gain frequency (UGF), the upper limit of the open-loop gain can be increased by manipulating the frequency response as depicted by trace B of the Figure. The basic idea is for the gain to drop quickly as the frequency increases so that a larger dc gain is possible. Hence, regulation is improved while keeping the UGF away from parasitic poles. The placement of the extra pole and zero must take into account that P_1, P_2, and Z_1 are functions of the output capacitance, the electrical series resistance (ESR) of the output capacitor, and the load-current. However, the fact that P_2 and Z_1 track each other (both are inversely proportional to ESR) can be used to optimize the design. It is further noted that the phase shift must be

kept below 180 ° at frequencies equal to and lower than the UGF to maintain stability, as dictated by Nyquist criterion [39].

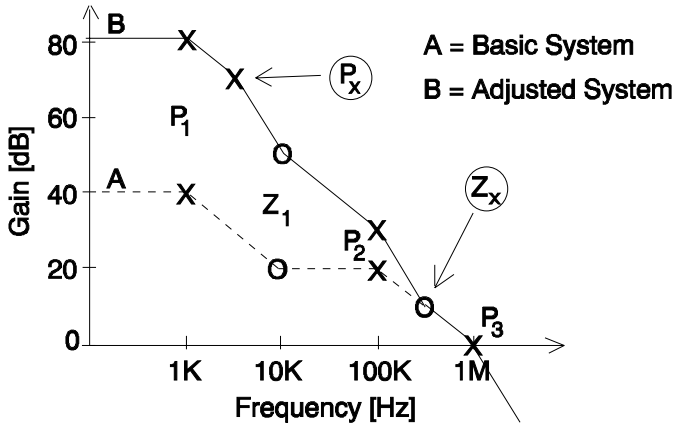

Figure 4.9. System's frequency response with an additional pole/zero pair.

Figure 4.10 illustrates the simulation results of an LDO incorporating the additional pole/zero pair. There is roughly a 17 dB improvement in the dc open-loop gain of the system with the additional pole/zero pair for a given unity gain frequency (UGF). Load regulation performance improved from approximately 41 to 12 mV / 100 mA, corresponding to a 71 % reduction. The design location of the additional pole and zero depends on the gain of the system and the variability of Z_1 and P_2. The achievement of maximum gain comes at the expense of restricted ESR range. This range is important for its variation is dependent on the type of capacitor and the fabrication process. Typically, relatively inexpensive capacitors exhibit the worst ESR variation. Given a constant UGF, maximum gain occurs when P_x and Z_x are maximally displaced from each other in frequency. This is because the drop in gain per decade of frequency in mid-band is larger when P_x is at lower frequencies and Z_x is at higher frequencies. Thus, maximum gain can be achieved efficiently if Z_1 and P_2 are guaranteed to be between P_x

and Z_x throughout their entire range. For this to be true, the ESR must be greater than some finite non-zero number. However, Z_1 and P_2 tend to infinity as the ESR is allowed to approach zero. Consequently, the frequency differential between P_x and Z_x is limited by the phase requirements of the system, less than 180° phase shift. If the ESR is bounded by a finite lower limit where Z_x is guaranteed to be greater than Z_1, the phase minimum is defined by P_x and Z_1, otherwise defined by P_x and Z_x.

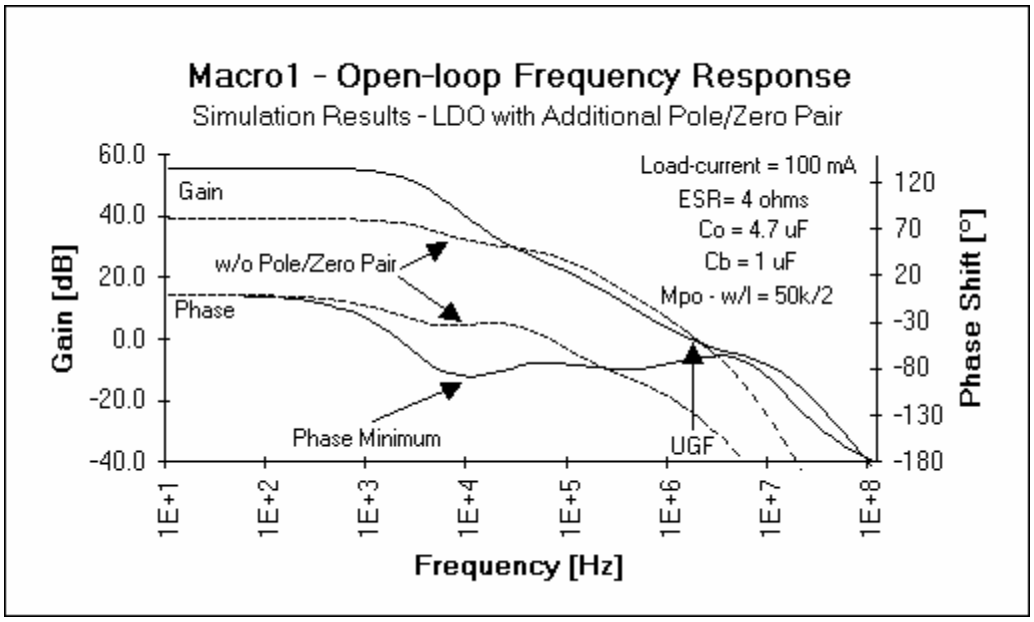

Figure 4.10. AC simulation of LDO with an additional pole/zero pair.

Circuit Realizations

The adjusted circuit architecture needs to provide a new function, namely, adding a pole/zero pair in the frequency response of the open-loop system. A customary method of adding a pole/zero pair is through the use of passive components at the output. Another way to achieve the same goal is to actually incorporate it into the frequency

response of the error amplifier via active components. In essence, the amplifier serves to shape the frequency behavior of the system as well as provide gain.

Parallel Amplifier Structure: One method of integrating the pole/zero pair response into the amplifier is to have dual amplifiers connected in parallel as shown in Figure 4.11. One amplifier has high gain and whose bandwidth determines the location of P_x while the other has lower gain (whose magnitude determines the location of Z_x) and higher bandwidth. The output impedances of both amplifiers need to be relatively low for proper operation. The main concept revolves around feed-forwarding the ac signal through a bypass path constituted by the amplifier with lower gain. The transfer function of both amplifiers and the resulting response of the system are shown in Figure 4.11 (b). The gain-bandwidth product of the high gain amplifier can be utilized to determine the necessary gain of the other amplifier to introduce Z_x at the desired frequency, as shown by the following relation,

$$GBW_1 = \frac{A_1}{2\pi P_x} = \frac{A_2}{2\pi Z_x} \quad \text{or} \quad \frac{A_1}{A_2} = \frac{P_x}{Z_x}, \tag{4.20}$$

where A_1 and A_2 correspond to the gain of amplifier one and two respectively while GBW_1 corresponds to the gain-bandwidth product of amplifier one. It is observed that the bandwidth of the second amplifier constitutes a parasitic pole in the overall system. Furthermore, the frequency of P_x is dependent on the dominant pole of amplifier one, which is subject to process variations. However, the ratio of P_x and Z_x exhibits less variation since it is mainly determined by component matching issues, if designed carefully. The main disadvantage of the circuit is complexity. Consequently, the realization of the two amplifiers may prove to be costly in terms of quiescent current flow. This results from more current sensitive transistor paths to ground because there

are two amplifiers. Figure 4.10 shows the simulation results of a macro-model circuit implementing the parallel amplifier structure.

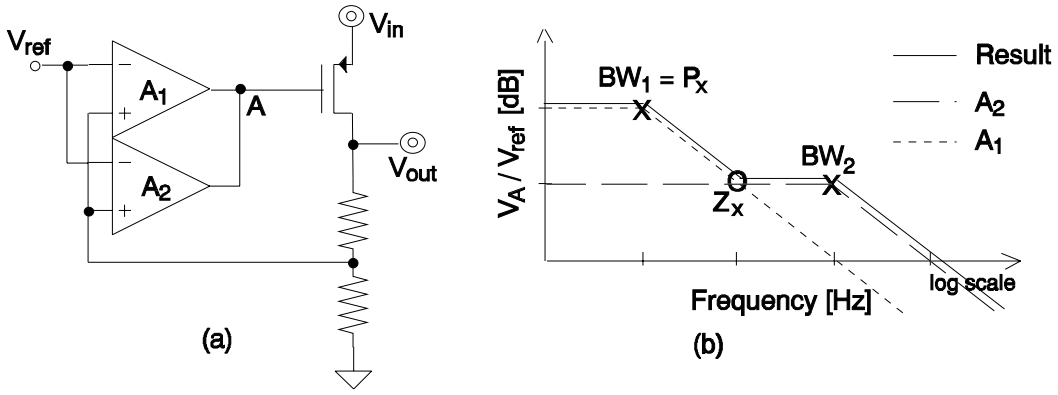

Figure 4.11. Parallel amplifier pole/zero pair realization.

Frequency Shaping Amplifier: A pole/zero pair can also be generated through the use of a feed-forward capacitor in a folded topology as shown in Figure 4.12 (a). At low frequencies, the amplifier is unaffected by the feed-forward capacitor (C_{ff}). Thus, the gain is that of a typical folded topology, which is characteristically high. At high frequencies, the capacitor acts like an electrical short giving rise to the gain of a non-cascoded architecture (lower gain). The corresponding small signal model of the circuit is represented in Figure 4.12 (b). The gain of the amplifier (A_v) is described by

$$A_v \approx g_{m1} R_o = g_{m1}\left[R_{Load} || R_x\right] \approx g_{m1} R_x, \qquad (4.21)$$

where g_{m1} is the transconductance of Mp1, R_{Load} is the output resistance of the mirror load, and R_x is

$$R_x = \frac{r_{ds3}\left[1 + g_{m3} r_{ds2}\right]}{1 + s r_{ds3} C_{ff}} + r_{ds2} = \frac{\left\langle s + \dfrac{r_{ds2} + r_{ds3}\left[1 + g_{m3} r_{ds2}\right]}{r_{ds3} r_{ds2} C_{ff}} \right\rangle r_{ds2}}{s + \dfrac{1}{r_{ds3} C_{ff}}}, \tag{4.22}$$

where g_{m3} is the transconductance of Mn3 and r_{ds2} [r_{ds3}] is the output resistance of

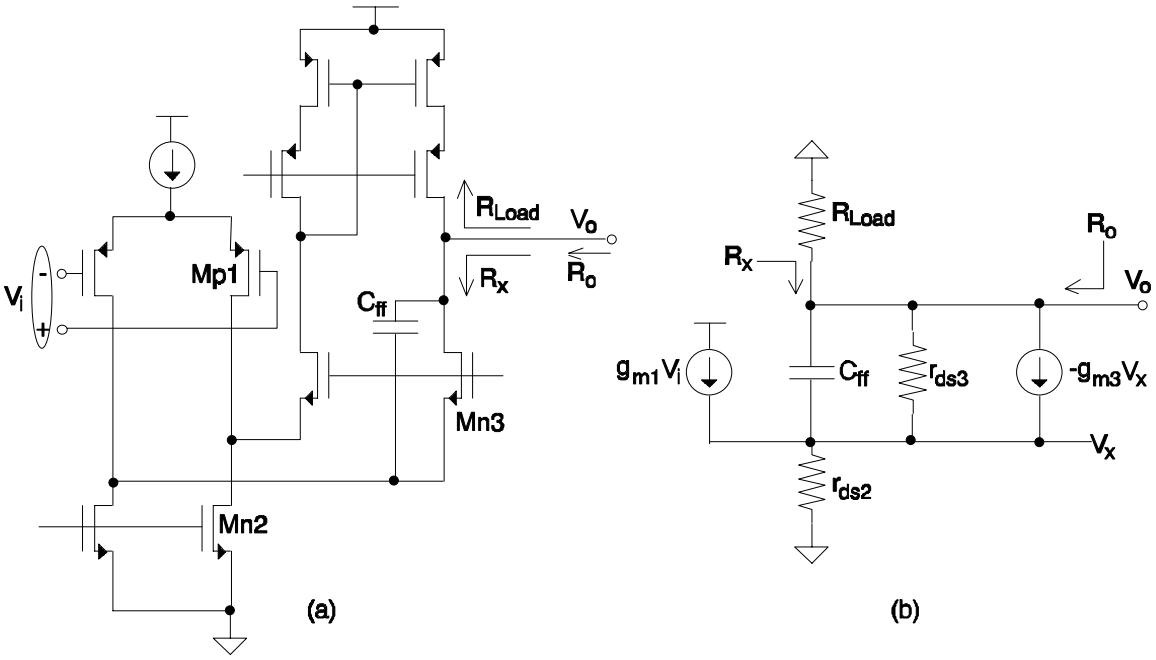

Figure 4.12. Pole/zero pair generation by a feed-forward capacitor.

transistor Mn2 [Mn3]. Consequently, the locations of the pole and the zero are

$$Z_x \approx \frac{g_{m3}}{2\pi C_{ff}} \tag{4.23}$$

and

$$P_x \approx \frac{1}{2\pi r_{ds3} C_{ff}}, \tag{4.24}$$

where g_{m3} and r_{ds3} correspond to the transconductance and the output resistance of Mn3. The cascoding element's transconductance (g_{m3}) needs to be small, which implies the use of MOS devices instead of bipolar transistors in a biCMOS environment.

The frequency shaping amplifier can also take a couple of other forms within the same folded architecture, as is illustrated by the different loading structures in Figure 4.13. A variation of the feed-forward concept is embodied in the circuit of Figure 4.13 (a). Small signal analysis shows that the pole and the zero locations for this structure are described by

$$Z_x \approx \frac{1}{2\pi RC_{ff}} \tag{4.25}$$

and

$$P_x \approx \frac{1}{2\pi\left[R + r_{o3}\right]C_{ff}}, \tag{4.26}$$

where r_{o3} is the output resistance of Qn3. Yet another realization of the pole/zero pair is illustrated in Figure 4.13 (b). This circuit takes advantage of the input and the output impedance of the mirror load, composed of Mp4 and Mp5, to help shape and define the frequency response of the amplifier. The corresponding pole and zero locations are described by

$$Z_x = \frac{1}{2\pi\left\langle R + \frac{1}{g_{m5}}\right\rangle C} \tag{4.27}$$

and

$$P_x = \frac{1}{2\pi\left\langle R + \frac{1}{g_{m5}} + r_{ds4}\right\rangle C}, \tag{4.27}$$

where g_{m5} is the transconductance of Mp5 and r_{ds4} is the output resistance of Mp4.

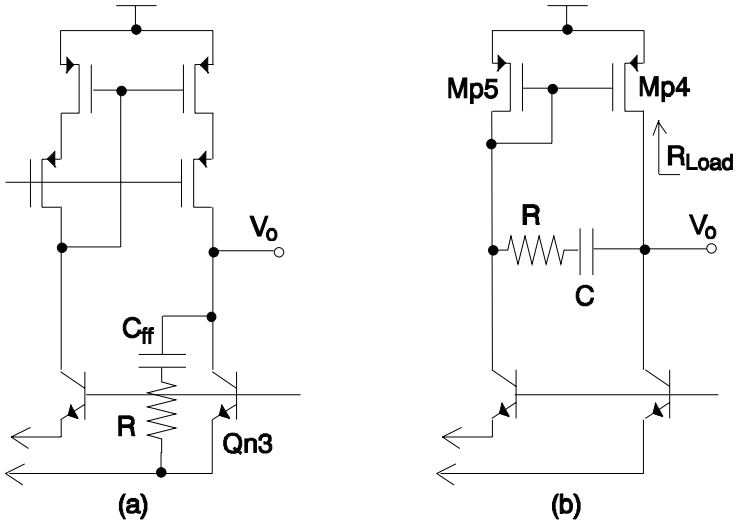

Figure 4.13. Variations of the frequency shaping amplifier.

The frequency response of the amplifiers introduce a single parasitic pole to the overall system. This parasitic pole is formed by the loading capacitor of the amplifier. This may be significantly large if the amplifier drives the gate of the large power PMOS transistor directly, pass device in the linear regulator structure. The severity of this problem can be alleviated by buffering the output of the amplifier and thus isolating the large capacitive load from the amplifier. The effects of process variations on performance manifest themselves through deviations in transconductances and transistor output impedances, which in turn define the locations of the pole and the zero as well as the parasitic pole. Simulations confirmed the operation of the frequency shaping amplifier topologies showing results that closely resemble those illustrated in Figures 4.9 and 4.10.

4.4 Summary

This chapter has identified the challenges of designing in a low voltage and low quiescent current atmosphere and developed appropriate techniques for achieving the necessary performance requirements. Current efficiency was identified as an intrinsic regulator characteristic for prolonged battery life. This was followed by a circuit development culminating in a current efficient buffer circuit. The problems with output current capabilities under reduced gate drives were addressed, which led to the development of the composite current boosted pass device. Lastly, the inherent limit of load regulation was identified along with a technique used to enhance its performance, the addition of a pole/zero pair. Appropriate circuits were then developed climaxing in the frequency shaping amplifiers. At this point, all that is needed is a low voltage and low quiescent current reference. Chapter 5 develops the techniques necessary for generating such a reference.

CHAPTER V

REFERENCE DEVELOPMENT

There are many reference topologies available for a variety of different applications and process technologies. Currently, a large portion of the market demand is driven by portable electronic products whose operating voltages range from 0.9 to 5 V and whose temperature drift requirements are in the order of 10 to 50 ppm/°C. In particular, the direction of the market is towards single, low voltage battery cell operation. As a result, the specifications become more stringent because of an inherent reduction in dynamic range. This chapter illustrates several of the prevailing concepts that lead to the development of low voltage references. The discussion places emphasis on performance and feasibility in a low voltage environment. This is followed by a description of the pertinent output structures and some of their circuit implications. Finally, the chapter concludes by portraying several curvature correcting schemes appropriate for second order bandgaps.

5.1 Topologies

Zener

One of the most common and simplest realizations of a reference circuit is through the use of a zener diode and a resistor [1, 21] as shown in Figure 5.1. When the diode is forward biased, the voltage across the diode exhibits the well known exponential

relationship to current. When the diode is reverse biased, the current through the diode becomes negligible. However, if enough reverse bias voltage is applied, the diode goes into the reverse breakdown region. In this mode of operation, significant changes in current lead to nearly negligible fluctuations in diode voltage. As a result, a low output impedance at the cathode of the diode arises varying typically from 10 to 300 Ω. Most common zener diodes have a breakdown voltage between 5.5 and 8.5 V and a positive temperature drift, approximately between +1.5 and +5 mV/°C. This temperature drift can be reduced by cascading a negative temperature coefficient element, i.e., a forward biased diode with a typical drift of roughly -2 mV/°C. This performance enhancement, however, comes at the expense of increased output voltage. As a result of high operating voltages, the zener diode is appropriately demanded by high voltage applications [1, 3].

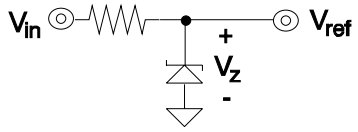

Figure 5.1. Zener diode reference.

First Order Bandgap

First order bandgap references are more accurate and suitable for low voltage operation than the zener counterparts. Typical bandgap references have an output voltage of approximately 1.2 V, which corresponds to the bandgap voltage. The operation is based on the temperature dependence of the base-emitter voltage of a bipolar transistor (V_{be}) or equivalently a forward biased diode. This dependence can be observed to have a linear and a nonlinear component with respect to temperature, as described by

$$V_{be} \approx V_{go} - \frac{T}{T_r}\left[V_{go} - V_{be}(T_r)\right] - [\eta - x] V_t \ln \frac{T}{T_r}, \qquad (5.1)$$

where V_{go} is the bandgap voltage at 0 K (constant), T is the temperature, T_r is a reference temperature, $V_{be}(T_r)$ is the value of V_{be} at T_r, η is a process dependent constant, V_t is the thermal voltage, and x is determined by the temperature dependence of the collector current ($I_c \propto T^x$, i.e., x = 1 for $I_c = I_{PTAT} = CT^1$ where C is a constant). Appendix A describes the derivation of said equation, which is a variant of that offered by [40]. First order bandgaps compensate the linear component and ineffectively compensate the nonlinear component by summing a proportional-to-absolute temperature (PTAT) voltage and a base-emitter drop. The PTAT voltage increases linearly with temperature thereby efficiently canceling the effect of the negative linear temperature dependence of the base-emitter voltage. The resulting output voltage exhibits improved temperature variation performance, typically between 20 and 50 ppm/°C [41]. However, the extent of the improvement is limited by the nonlinear component embodied in the logarithmic term of equation (5.1) and whose effect is depicted by the curvature of V_{ref} in Figure 5.2.

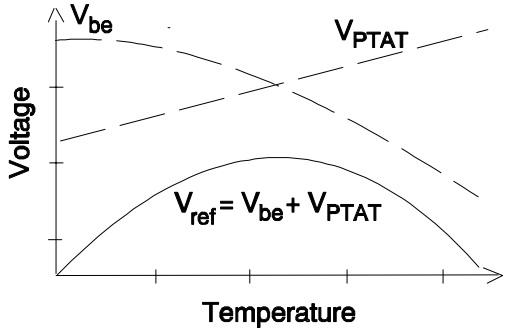

Figure 5.2. Temperature behavior of first order bandgaps.

Curvature Corrected Bandgap

Curvature corrected bandgaps attempt to approximately cancel the nonlinear component of the base-emitter voltage, typically referred to as a second order effect. The classical method of doing such compensation is through the addition of a squared PTAT term to the output voltage relation of first order bandgaps [42]. The idea is to offset the negative temperature dependence of the logarithmic term in V_{be} with a positive parabolic term. Figure 5.3 shows the typical temperature drift performance achieved by a squared PTAT term curvature corrected bandgap. The lower temperature range is predominantly controlled by the base-emitter voltage and the linear PTAT term (V_{be} + V_{PTAT}). However, the squared PTAT term ($V_{PTAT}2$) becomes considerably large as the temperature increases. This behavior is used to cancel the increasingly negative temperature dependence of the base-emitter voltage to yield the curvature depicted by V_{ref} in Figure 5.3. One implementation of the squared PTAT term is through the use of a Gilbert Multiplier cell and a PTAT current generator. Prevailing curvature corrected bandgaps achieve a temperature drift performance of roughly 1 to 20 ppm/°C [41].

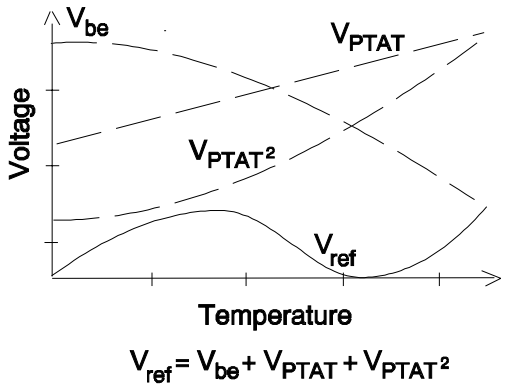

Figure 5.3. Squared PTAT curvature correction method for bandgaps.

5.2 Output Structures

V-mode and I-mode

Typical circuit realizations of references adopt a voltage-mode approach, labeled here as V-mode. In other words, the reference voltage is defined by the summation of temperature dependent voltages, as intimated by the previous discussion and realized by many curvature corrected bandgap references like that of [43]. This is also the case for zener and most bandgap references, i.e., $V_{be} + V_{zener}$ for compensated zener references or $V_{be} + V_{PTAT}$ for bandgaps as shown in Figure 5.4 (a). The resulting output voltage is approximately 1.2 V, which corresponds to the bandgap voltage at 0 °K (equation (5.1)). One benefit of this approach is that temperature compensation can be manipulated at the output by a simple adjustment, i.e., changing the resistor value in the reference circuit of Figure 5.4 (a). On the other hand, the magnitude of the reference voltage places a harsh limit on low voltage operation. The corresponding input voltage must be greater than or equal to approximately 1.4 V (a V_{sat} above the bandgap voltage). The driving market, unfortunately, demands single, low voltage battery cell operation. Consequently, there are applications that require and significantly benefit from references whose output voltages are less than 1.2 V.

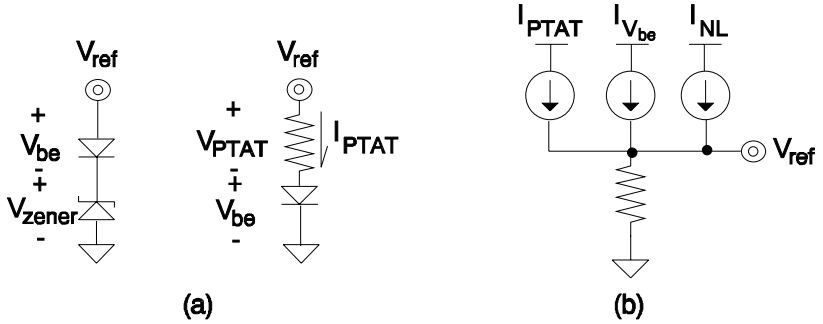

Figure 5.4. Output structures (a) voltage-mode and (b) current-mode.

Lower reference voltages can be achieved by the implementation of a current-mode topology, depicted here as I-mode. The technique relies on summing temperature dependent currents into a resistor, as shown in Figure 5.4 (b). For the case of curvature corrected bandgaps, the temperature dependencies of the current components are PTAT, base-emitter voltage, and some nonlinear behavior (NL). The value of the output voltage is determined by the product of the magnitude of the currents and the resistor. Consequently, the output voltage for this configuration is flexible enough to accommodate a wide range of values ranging from a few millivolts to several volts. Such a circuit is realized and embodied in the bipolar, low voltage reference design of [40]. If designed properly, the temperature dependence of the resistor is canceled out by the nature of the currents, which are defined by resistors of equal type. This is illustrated by the relationship of the reference voltage and the temperature dependence of the resistor where the values of the currents reflect how they are physically generated,

$$V_{ref} = \left\langle I_{V_{be}} + I_{PTAT} + I_{NL} \right\rangle R = \left\langle K_a \frac{V_{be}}{R_a} + K_b \frac{V_t}{R_b} + I_{NL} \right\rangle R, \qquad (5.2)$$

where K_a and K_b are constants, R_a and R_b are resistors (same type as R), and the terminology of Figure 5.4 (b) is adopted. The temperature dependence of the resistors can be described as

$$R(T) = R(T_r) \cdot \left[1 + A(T - T_r) + B(T - T_r)^2 \right], \qquad (5.3)$$

where T is temperature, A and B are the linear and the quadratic temperature coefficients, and $R(T_r)$ is the resistance at room temperature (T_r). Consequently, the reference voltage can be re expressed as

$$V_{ref} = \left\langle K_a \frac{V_{be}}{R_a(T_r)} + K_b \frac{V_t}{R_b(T_r)} + I_{NL} \right\rangle \frac{R(T_r)\cdot\left[1 + A(T - T_r) + B(T - T_r)^2\right]}{1 + A(T - T_r) + B(T - T_r)^2} \quad (5.4)$$

or

$$V_{ref} = \left\langle K_a \frac{V_{be}}{R_a(T_r)} + K_b \frac{V_t}{R_b(T_r)} + I_{NL} \right\rangle R(T_r), \quad (5.5)$$

where I_{NL} is redefined to absorb the temperature dependence of the resistor. Hence, the temperature coefficients of the resistors are canceled as long as R_a, R_b, and R are all the same type, i.e., base-diffusion resistors.

IV-mode

The benefits of a current-mode and a voltage-mode topology can be combined to generate a widely flexible structure. Such a structure is illustrated in Figure 5.5 and referred as an IV-mode structure. The resulting architecture complements the basic current-mode topology with a voltage-mode ladder. The current-mode approach offers the possibility of lower reference voltages while the voltage-mode ladder gives greater temperature compensation maneuverability. Hence, a low voltage reference is realized whose individual temperature components can be optimized during the trimming process. The resulting relation of the reference voltage (V_{ref}) can be described by

$$V_{ref} = I_{V_{be}}\left[R_1 + R_2 + R_3\right] + I_{PTAT}\left[R_1 + R_2\right] + I_{NL}R_1, \quad (5.6)$$

where I_{Vbe}, I_{PTAT}, and I_{NL} correspond to the base-emitter, PTAT, and nonlinear temperature dependent currents respectively. The temperature dependence of the resistors is canceled by the nature of the currents, similar to the current-mode case. A trimming algorithm for this type of structure is shown in appendix B.

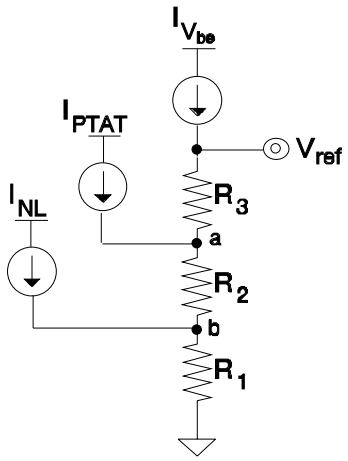

Figure 5.5. IV-mode output topology.

5.3 Bandgap Curvature Correction Techniques

The consequence of the growing demand for low voltage operation is reduced voltage swings as well as reduced dynamic range [10]. This results because the noise floor does not decrease linearly with reductions in power supply voltage. As a result, precise references are necessary. Thus, curvature correction techniques for bandgap circuits need to be scrutinized. The typical correction technique of generating a squared PTAT term is effective but its circuit realization tends to be expensive in terms of component count and quiescent current flow. Alternative methods include a base-emitter voltage loop, beta (β) compensation, quasi-nonlinear cancellation, temperature dependent resistor ratio, and current subtraction.

V_{be} Loop

Through the combination of different temperature dependent currents and a base-emitter voltage loop a nonlinear current component can be effectively generated [40]. This technique is appropriate for I-mode and IV-mode output topologies. The circuit realization is illustrated in Figure 5.6. The nonlinear current component (I_{NL}) is defined

by the temperature dependent currents and by the transistor loop formed by Qn1 and Qn2,

$$I_{NL} = \frac{V_t}{R_3} \ln \frac{I_{c1} A_2}{A_1 I_{c2}} = \frac{V_t}{R_3} \ln \frac{2I_{PTAT}}{I_{NL} + I_{constant}}, \tag{5.7}$$

where $I_{constant}$ is a quasi-temperature independent current that is subject to the temperature coefficient of the resistors,

$$I_{constant} = I_{NL} + I_{PTAT} + I_{V_{be}} \approx I_{NL} + \frac{V_t}{R_x} + \frac{V_{be}}{R_2}, \tag{5.8}$$

where V_t is the thermal voltage, I_{c1} [I_{c2}] and A_1 [A_2] are the collector currents and areas of Qn1 [Qn2] respectively, and R_x is a resistor used to define I_{PTAT}. The current I_{NL} is a logarithmic function of itself thereby exhibiting a nonlinear behavior. The resulting reference voltage (V_{ref}) of this current-mode circuit is

$$V_{ref} = \left\langle \frac{V_{be}}{R_2} + \frac{V_t}{R_3} \ln \frac{2I_{PTAT}}{I_{NL} + I_{constant}} + I_{PTAT} \right\rangle R_1. \tag{5.9}$$

Although the method is appropriate for high accuracy in a low voltage environment, the circuit's complexity is conducive towards relatively high quiescent current flow. The physical realization of the circuit by [40] achieved a temperature coefficient (TC) of roughly ± 3.0 ppm/°C with a total quiescent current flow of 95 μA.

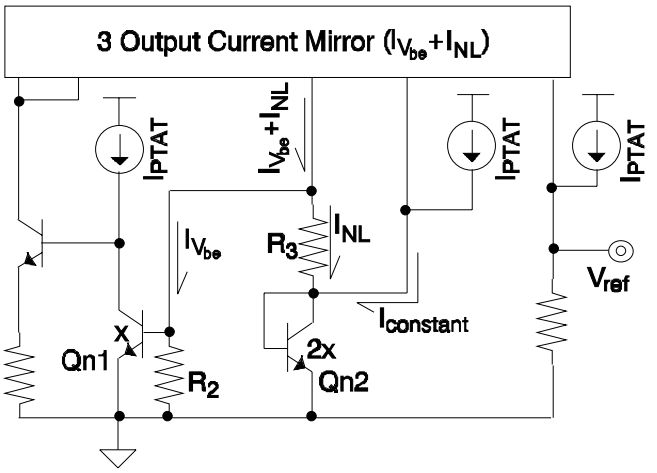

Figure 5.6. V_{be} loop curvature correction method.

β Compensation

Another technique for correcting the nonlinear behavior of the base-emitter voltage is by exploiting the exponential temperature dependence of the NPN transistor's forward current gain (β), $\beta \propto e^{-1/T}$ [44]. Figure 5.7 illustrates a simple circuit realization that takes advantage of this relationship to temperature. The circuit implements a negative reference but its translation to a positive voltage architecture is simply achieved by designing the complement of the structure. The resulting reference voltage is

$$V_{ref} = -\left\langle AT + \frac{BT}{\beta} \right\rangle R - V_{be}, \tag{5.10}$$

where A and B are constants and T refers to temperature. The circuit has the advantage of being simple and achieving good performance at low quiescent currents. However, the circuit falls within the category of a voltage-mode topology. Consequently, it is not appropriate for low voltage operation because the input voltage is limited by the bandgap

voltage, $V_{in} \geq |V_{ref}| + V_{sat} = V_{go} + V_{sat} \approx 1.4$ V. A more complex circuit would be required to transform the topology into a low voltage, current-mode structure.

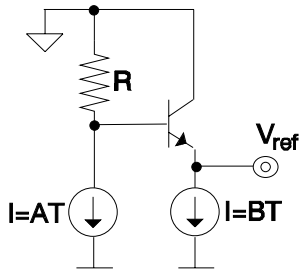

Figure 5.7. β curvature corrected bandgap.

Nonlinear Cancellation

The ideal method of performing curvature correction lies in completely correcting the nonlinear behavior of a bandgap reference by eliminating the nonlinear term of the base-emitter voltage relationship, the logarithmic term of equation (5.1). This can be accomplished by manipulating the variable x to equal the extrapolated process dependent constant η, which is approximately four [45]. In particular, x is dependent on collector current; thus, when the collector current for an NPN device is PTAT ($I_c \propto T^1$) x is equal to one. On the other hand, x is equal to zero when the collector current is independent of temperature ($I_c \propto T^0$). This behavior is exploited in the circuit illustrated in Figure 5.8 where an NPN diode loop is implemented. The resulting reference voltage can be described by

$$V_{ref} = V_{PTAT} + 4V_{be}(I_{PTAT}) - 3V_{be}(I_{constant}), \qquad (5.11)$$

where $V_{be}(I_{PTAT})$ and $V_{be}(I_{constant})$ are base-emitter voltages with I_{PTAT} and $I_{constant}$ as collector currents respectively. If equation (5.1) is substituted into (5.11), the reference voltage becomes

$$V_{ref} = V_{go}\left[1 - T_r^{-1}\right] + V_{PTAT} + T\frac{V_{be}(T_r)}{T_r} - \left[\eta - 4\right]V_t \ln\frac{T}{T_r}; \qquad (5.12)$$

however, η - 4 approximately cancels to zero yielding a theoretically linear relationship with respect to temperature,

$$V_{ref} \approx V_{go}\left[1 - T_r^{-1}\right] + V_{PTAT} + T\frac{V_{be}(T_r)}{T_r}. \qquad (5.13)$$

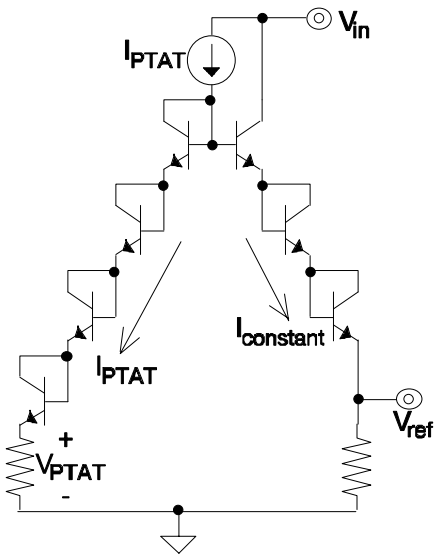

Figure 5.8. Quasi-nonlinear term cancellation bandgap reference.

This relation, unfortunately, is susceptible to two non idealities, namely, the effects of the temperature coefficient of the resistors in the circuit and the non integer nature of the value of η. Nevertheless, the circuit provides an accurate reference voltage with

potentially low quiescent current flow. The major drawback, however, is that the circuit topology is not appropriate for low voltage operation. This a result of the stack of multiple base-emitter voltages,

$$V_{in} \geq V_{PTAT} + 4V_{be} + V_{current\text{-}source}. \qquad (5.14)$$

Temperature Dependent Resistor Ratio

A nonlinear component can be generated by exploiting the temperature dependence of resistors in a given process. Typically, this is either canceled or considered a parasitic in most circuit realizations. Figure 5.9 illustrates how the temperature coefficient (TC) of resistors can be used in an IV-mode bandgap reference for curvature correction. The idea is to temperature compensate by generating a squared PTAT term (classical curvature correction method) without incurring a significant cost in quiescent current flow. The reference voltage of the sample circuit is

$$V_{ref} = \frac{AV_{be}}{R_1} R_4 + \frac{AV_t}{R_2} R_4 + \frac{AV_t}{R_2} R_3, \qquad (5.15)$$

where A and B are constants, V_t corresponds to the thermal voltage, and all the resistors are the same type except for R_3. Thus, the temperature dependence of the resistor ratio of R_3 and R_2 must be roughly linearly positive to generate an approximated $PTAT^2$ term. This can be achieved by choosing two appropriate resistor types. Consequently, the third term of equation (5.15) corresponds to the curvature correcting component while the first two correspond to a first order bandgap. The architecture has the advantage of being simple to realize as well as not require any additional quiescent current. The circuit suffers from a subtle disadvantage, namely, the large mismatch between the two types of

resistors. This simply translates to more stringent trimming procedures. A significant disadvantage, however, lies in successfully finding two types of resistors whose ratio has a positive and linear temperature dependence within a given process technology.

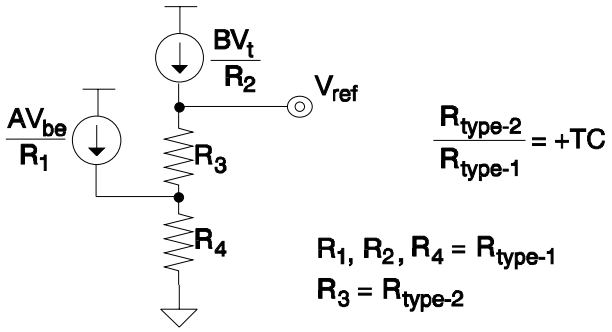

Figure 5.9. Temperature dependent resistor ratio curvature correction.

Current Subtraction

A curvature correcting nonlinear component can also be realized by manipulating different temperature dependent currents via ordinary transistors. Figure 5.10 shows how a current subtraction circuit can generate this nonlinear component (I_{NL}). The essence of the circuit revolves around current subtraction and the innate characteristics of non ideal transistors. Transistor Mp1 acts like a non ideal current source of a current that is proportional to a base-emitter voltage. At the lower half of the temperature range, the PTAT current sunk (I_{PTAT}) is less than the supplied V_{be} dependent current (I_{Vbe}). As a result, Mp2 is off and Mp1 becomes non-saturated and provides only the PTAT current. At the upper half of the temperature range, however, the current sunk becomes larger than the V_{be} dependent current supplied by Mp1. Consequently, Mp1 becomes saturated and only supplies the V_{be} dependent current while Mp2 sources the current difference. The resulting current through Mp3 (mirror ratio of Mp2) is nonlinear, off during the first

half of the temperature range and on during the latter half. This behavior can be described by

$$I_{NL} = \begin{cases} 0 & I_{V_{be}} \geq I_{PTAT} \\ I_{PTAT} - I_{V_{be}} & I_{V_{be}} < I_{PTAT} \end{cases}. \tag{5.16}$$

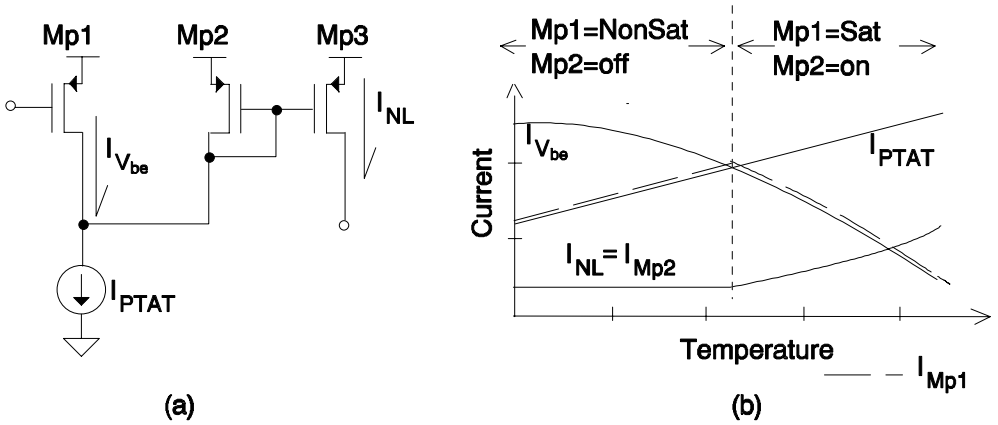

Figure 5.10. Current subtraction method for generating I_{NL}.

Figure 5.10 (b) graphically illustrates the operation of the circuit throughout the temperature range. Curvature correction is achieved by combining the three temperature dependent elements to yield an output that is stable over temperature. These components can be used to temperature compensate by partitioning the temperature range in two, the portion for which the nonlinear current component is (1) zero and (2) non-zero. As a result, the reference voltage (V_{ref}) can be temperature compensated to exhibit a behavior that is graphically described by Figure 5.11. The lower temperature range is basically a first order bandgap, since the nonlinear component (I_{NL}) is zero. At higher temperatures, the resulting behavior is similar to that of the lower temperatures but the operation is not. The nonlinear behavior of I_{NL} (equivalent to $I_{V_{be}}$ - I_{PTAT}) attempts to diminish the effects of the nonlinear term of $I_{V_{be}}$. Consequently, the addition of these two currents

(I_{NL} + I_{Vbe}) and I_{PTAT}, at the upper temperature range, generate a curvature corrected trace whose behavior is depicted by V_{ref} in Figure 5.11. Overall, the circuit benefits from being simple, process independent, and appropriate for low voltage operation.

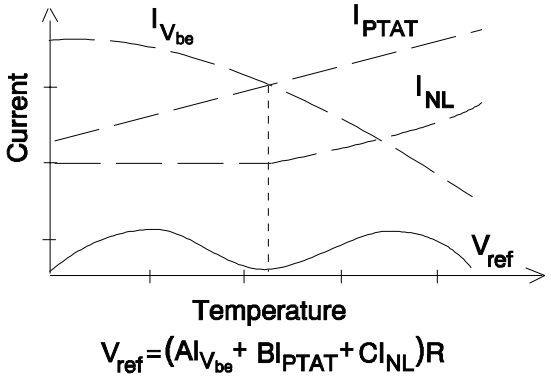

Figure 5.11. Temperature dependence of the curvature corrected bandgap.

5.4 Summary

The chapter has presented the prevailing reference topologies ranging from simple zener realizations to more complex curvature corrected bandgap references. They were evaluated for their temperature drift performance in a low voltage environment. As a result of stringent accuracy requirements, it was concluded that a curvature corrected bandgap reference was necessary. Appropriate output structures were then illustrated culminating in a mixture of voltage and current mode structures (IV-mode), which produced the best combined characteristics. This was followed by a discussion of the different methods of performing curvature correction. These were gauged with respect to low voltage and low quiescent current flow. The least expensive technique in terms of component count, voltage overhead, and additional quiescent current flow was the current subtraction technique. Therefore, the bandgap circuit implementing the IV-mode output structure and the current subtraction curvature correction method is suitable for

low voltage and low quiescent current applications. At this point, the concepts developed in this chapter and those discussed in the previous chapter can be used to do the actual circuit design, whose development is described in the following chapter.

CHAPTER VI

CIRCUIT DESIGN

The problems of low voltage operation typically emerge in the form of voltage headroom, common mode range, dynamic range, and voltage swings. Appropriate design techniques must be therefore implemented to approach the practical low voltage limits of a given process technology. Some of the techniques that are generally recommended are complementary input amplifiers and common source [emitter] gain stages. On the other hand, some of the discouraged techniques are unnecessary cascoding, Darlington configurations, and source [emitter] followers [10]. At the end, however, the choice of circuit topology and configuration depends on the specific application and process technology. The theoretical headroom limit for low voltage operation is a transistor stack of one diode connected device and one saturation voltage drop ($V_{gs}[V_{be}] + V_{ds}[V_{ce}]$), which approximately ranges between 0.9 and 1.1 V in most of today's standard technologies.

The theoretical headroom limit of low voltage for the MOSIS process technology is approximately 1 to 1.1 V (corresponding to $V_{sg\text{-}pmos} + V_{ds\text{-}nmos}$). The threshold voltage of MOS devices in this technology ranges from roughly 0.88 to 0.9 V. The same process also offers a p-base layer for the realization of vertical NPN transistors; however, the respective saturation voltage is large as a consequence of high series collector resistance. The absence of a highly doped buried layer prevents this series resistance

from decreasing to more favorable levels. Consequently, NPN saturation voltages are avoided in transistor stacks that define the headroom limit of low voltage.

In a purely CMOS environment, the absence of NPN transistors tends to yield more complex and/or lower quality circuits. The reference, in such processes, uses available pn junction diodes to generate base-emitter voltages as well as proportional-to-absolute temperature currents (PTAT). In an attempt to fully utilize the technology, however, the threshold implant diffusion (p-type for n-well processes) can be used as a p-type base [46]. As a result, a vertical NPN device can be formulated by using the n+ diffusion as the emitter, the threshold implant diffusion as the p-base, and the n-well as the collector (assuming an n-well technology). The resulting device has the advantage of high forward current gain (β) arising from low base-widths. The drawback, however, is high saturation voltage resulting from the absence of a buried layer, as is the case for the MOSIS technology. This concept can also be exploited in biCMOS technologies to reduce the number of masks required in the process flow. Consequently, relatively inexpensive products can be manufactured. Other device structures that can be utilized in vanilla CMOS processes are lateral and substrate bipolar transistors.

The block level diagram of the proposed low drop-out (LDO) regulator is illustrated in Figure 6.1. The circuit takes advantage of the performance enhancement techniques developed in chapter 4 and the low voltage reference circuit ideas discussed in chapter 5. The pass device is a PMOS composite structure that reaps the benefits of the current boosting technique. The amplifier is composed of a frequency shaping gain stage and a current efficient buffer. The gain stage effectively adds a pole/zero pair to the system's frequency response for the purpose of enhancing load regulation performance. The reference is composed of a low voltage, IV-mode, curvature corrected bandgap and a crude pre-regulator circuit. The output structure of the reference (IV-mode) is a mixture

of a current-mode and a voltage-mode topology. Lastly, a protection circuit block is added for completeness but its design is not included in this chapter. Protection circuitry is discussed in chapter 7 where the assembly of the system is addressed.

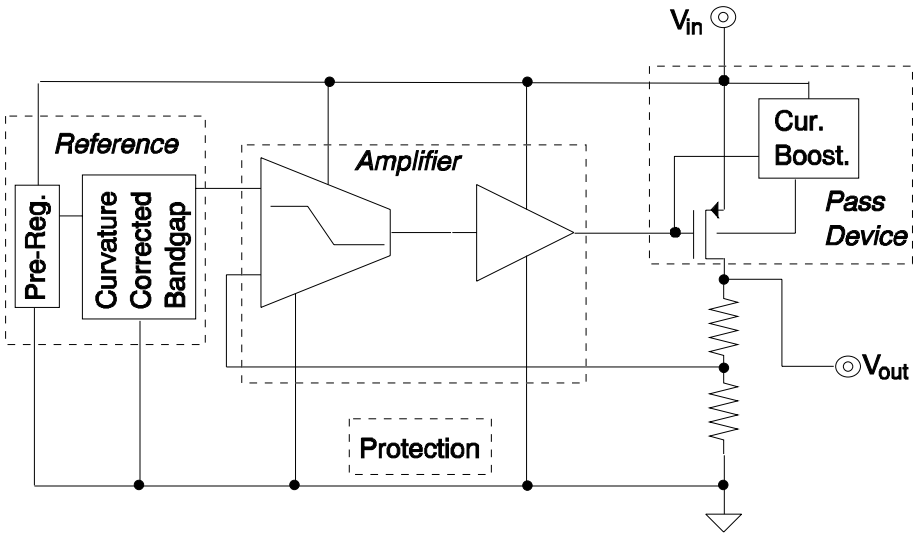

Figure 6.1. Block level diagram of the system.

6.1 Control Loop

Pass Device

The five basic possible configurations for the pass element are illustrated in Figure 6.2, namely, NPN Darlington, NPN emitter follower, common emitter lateral PNP, NMOS source follower, and common source PMOS transistor [4]. The degree of freedom for the choice of topology is dependent on the process technology and the required specifications of the LDO. Multiple transistor structures are also possible candidates for pass devices. However, the intrinsic performance characteristics of these structures revolve around the transistor that actually delivers the output current. The remaining devices can be grouped into the output stage of the error amplifier, otherwise referred as the buffer stage.

Table 6.1 shows a comparison between the different pass elements with respect to their applicable LDO performance parameters. Bipolar devices are capable of delivering the highest output currents for a given supply voltage. The output current capabilities per unit area of MOS transistors exhibit limited performance with high dependencies on aspect ratio and gate drive. However, the voltage driven nature of MOS devices is beneficial in minimizing quiescent current flow. Bipolar transistors are current driven devices with finite forward current gains (β) that can be as low as 20 A/A over process variations. As a result, the error amplifier that drives a bipolar pass element must be able to source or sink relatively high base currents during high load-current conditions. The base current of the NPN transistor, however, flows to the output while that of the PNP counterpart is lost as ground current. Consequently, NPN structures are better suited for low quiescent current designs than PNP realizations. Moreover, the quiescent current flow during drop-out conditions for PNP pass devices can become significantly large. The fastest response, needed for transient load-current steps, is achieved by the NPN structures. PNP transistors, on the other hand, are commonly created as lateral devices and thus exhibit inherently slower response times. Vertical PNP structures yield fast response times but their availability in standard process technologies is limited. MOS transistors are typically slower than vertical bipolar devices but faster than lateral PNP realizations.

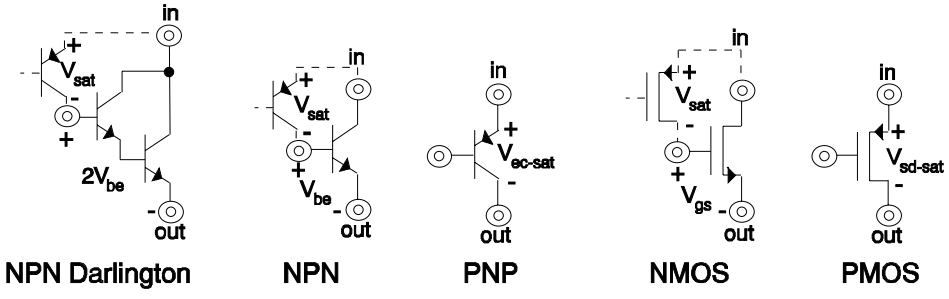

Figure 6.2. Pass element structures.

Table 6.1. Comparison of pass element structures.

Parameter	Darlington	NPN	PNP	NMOS	PMOS
$I_{o\text{-}max}$	High	High	High	Medium	Medium
$I_{quiescent}$	Medium	Medium	Large	Low	Low
$V_{drop\text{-}out}$	$V_{sat}+2V_{be}$	$V_{sat}+V_{be}$	$V_{ec\text{-}sat}$	$V_{sat}+V_{gs}$	$V_{sd\text{-}sat}$
Speed	Fast	Fast	Slow	Medium	Medium

Lowest drop-out voltages are achieved by PMOS ($V_{sd\text{-}sat}$) and PNP ($V_{ec\text{-}sat}$) transistors, approximately between 0.1 and 0.4 V. The NPN Darlington, NPN, and NMOS structures involve at least one V_{be} [V_{gs}] in addition to one $V_{ec\text{-}sat}$ [$V_{sd\text{-}sat}$] with a minimum drop-out voltage of roughly 0.8 to 1.2 V. However, the drop-out voltage of these pass devices can be improved by utilizing a charge pump. The disadvantage of this technique lies in complexity and cost. It requires an oscillator thereby increasing quiescent current overhead, noise injection, and circuit complexity. Excluding the charge pump method, PMOS transistors exhibit the lowest drop-out voltages because of their characteristically variable resistance, V_{sd} changes with gate drive and aspect ratio. On the other hand, PNP devices have a constant saturation voltage of approximately 200 mV. In conclusion, PMOS devices are typically the best overall choice yielding a good compromise of drop-out voltage, quiescent current flow, output current, and speed.

A composite PMOS pass device implementing the current boosting technique discussed in chapter 4 is illustrated in the schematic of Figure 6.3. The size of the schottky diode must be sufficiently large to ensure that its voltage drop is kept below one base-emitter drop. This is to prevent the parasitic vertical PNP transistors inherent in the

layout of a PMOS device within an n-well from conducting appreciable currents. The parasitic collector current flows from the source through the well and finally to the substrate (ground). This phenomenon can be further mitigated by placing a heavily doped buried layer underneath the PMOS device to reduce the forward current gain of the parasitic PNP transistors. The effect of forward biasing this source to bulk junction on the characteristics of the PMOS transistor is lower effective threshold voltage. The width of the metal traces for the source [emitter] and drain [collector] terminals must be large enough to handle the high current density required. Furthermore, series parasitic resistance inherent in the layout must be low to prevent drop-out voltages from significantly degrading, such culprits include the pass device's terminal contacts, metal traces, and diffusion links. The drive requirements of the pass device can generally define the minimum input voltage of the regulator, i.e., the gate drive of the PMOS transistor necessary to yield high output currents and low drop-out voltages ($V_{in} \geq V_{sg} + V_{ds}$, where V_{ds} corresponds to the voltage overhead of a current sink transistor).

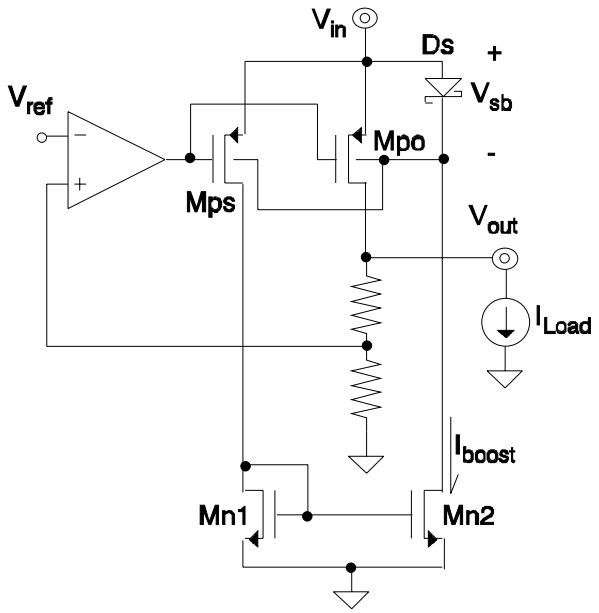

Figure 6.3. Composite PMOS pass device.

Drop-out Handicap: Ground current for the structure shown in Figure 6.3 can become significantly large during drop-out conditions when the nominal output voltage is greater than one V_{gs}. This results because the output PMOS transistor (Mpo) and the sense device (Mps) are in different regions of operations. For instance, if the output voltage is nominally 3.6 V and the input voltage is 3.65 V, then Mpo is in triode (V_{sd} = 0.05 V) and Mps is in saturation ($V_{sd} = V_{in} - V_{gs\text{-}Mn1} \approx 2.2 - 2.65$ V). As a result, the quality of the mirror is degraded and Mps conducts more current than predicted by the mirror ratio, possibly up to 1 mA. This is illustrated by a simulation whose results are shown in Figure 6.4 for a 2 μm CMOS MOSIS design where the current through Mps peaks at roughly 950 μA. Consequently, the source to bulk voltage of the PMOS transistor is increased and the overall current efficiency of the circuit is decreased thereby reducing battery life. The only way to ensure proper mirror operation during drop-out conditions is by forcing the source to drain voltages of Mpo and Mps to be equal.

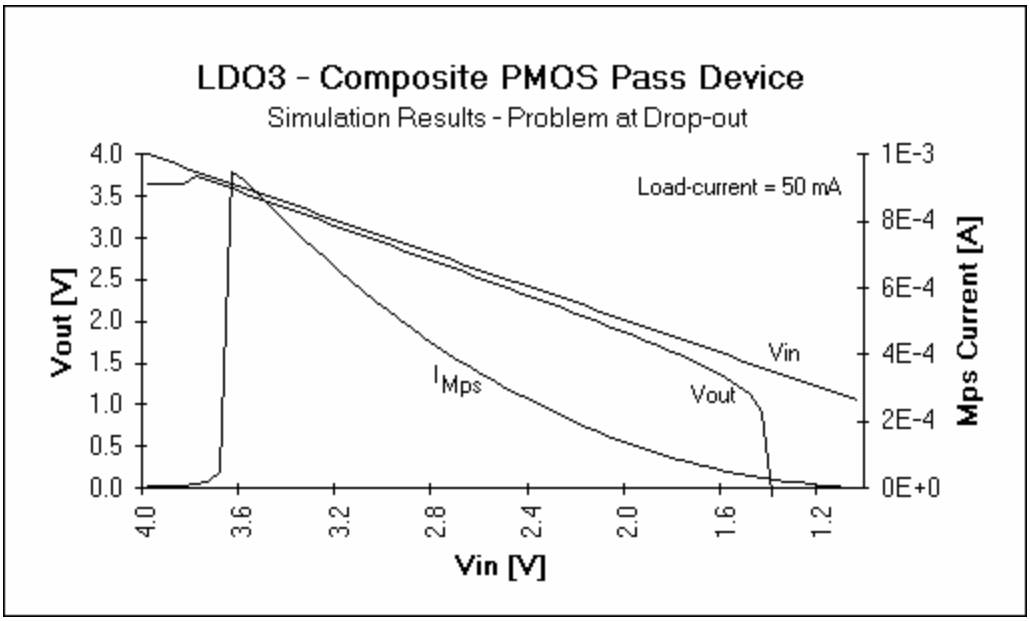

Figure 6.4. Simulation of current sensing problem at drop-out.

Solution: Figure 6.5 illustrates the development of a current replica mirror into a cost-efficient circuit that ensures that Mpo and Mps are in the same region of operation (V_{sg} and V_{sd} for both devices are equal). The concept is to sense the voltage at the output terminal (drain of Mpo) and force that voltage onto the drain of Mps. The lateral PNP transistors (Qp1 and Qp2) in Figure 6.5 (b) are used for this purpose. The drain of the sense transistor is cascoded by a lateral PNP device defining its drain voltage to be equal to that of transistor Mpo via a V_{be} loop. The current used to bias Qp2 can be small,

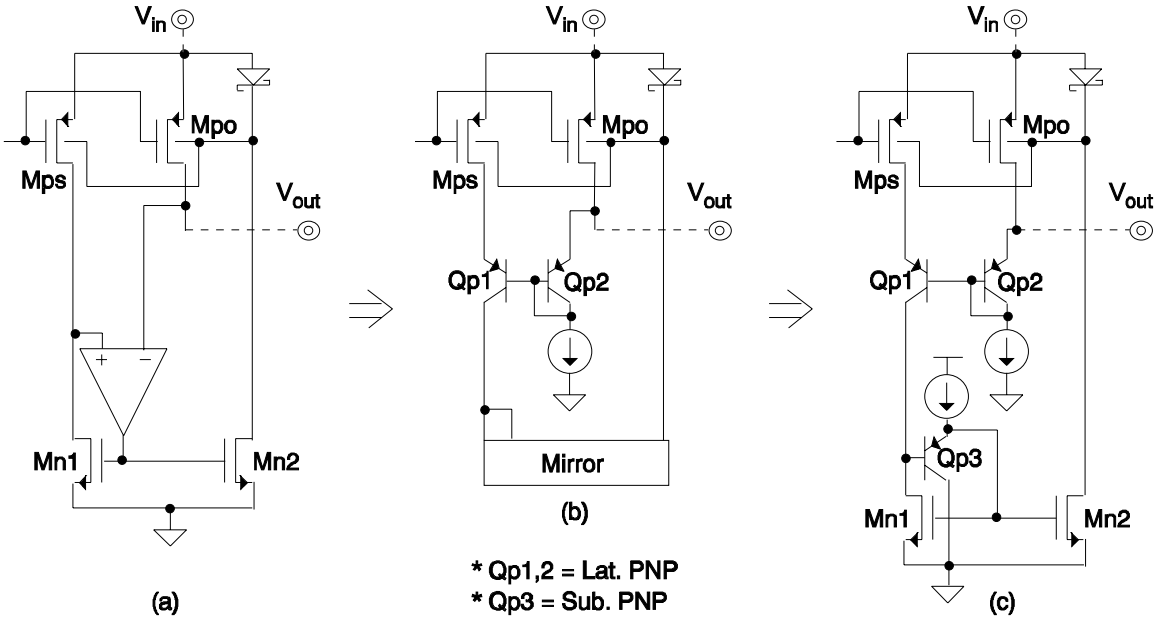

Figure 6.5. Pass device design development for efficient current sensing.

i.e., 0.5 - 1.0 μA. Unfortunately, a regular n-type mirror load for Qp1 is not appropriate for a low voltage environment. For instance, if a standard NMOS mirror is used, then the input voltage is limited to be greater than approximately 1.2 to 1.3 V ($V_{sd\text{-}Mps} + V_{ec\text{-}Qp1}$

+ $V_{gs\text{-}Mirror}$). Consequently, a low voltage mirror is necessary for the proper realization of the circuit. Figure 6.5 (c) shows the final version of the composite PMOS pass device with accurate current sensing capabilities using a low voltage mirror. Transistors Mn1, Mn2, and Qp3 basically constitute a standard mirror with a V_{eb} level shift. The voltage across the drain and source of Mn1 is V_{gs} - V_{eb}, which can be roughly between 0.15 and 0.3 V assuming that $V_{th\text{-}mos}$ is between 0.75 - 0.9 V. Transistor Qp3 can be a substrate bipolar device thereby exhibiting good frequency response and more compact layout characteristics than a lateral device. Simulated results show that the current through Mps is a proper mirror ratio of Mpo, even during drop-out conditions.

Amplifier

The circuit design of an LDO is thoroughly affected by the physical characteristics of the pass device. The pass device must be physically large to yield high output currents and low drop-out voltage characteristics. This translates to a large load capacitance for the error amplifier, characterized as C_{par} in the ac analysis section of chapter 2. Consequently, the parasitic pole at the output of the amplifier is pulled to lower frequencies thereby degrading the phase margin and possibly compromising the stability of the system. Moreover, leakage currents increase as the size of the device increases, i.e., MOS sub-threshold currents. This places an upper limit on device size, a lower limit on quiescent current flow, and/or more stringent requirements on the error amplifier. **Buffer:** A buffer is necessary to isolate the gain stage of the amplifier from the large power transistor since the gate of the output pass element is characterized by high capacitance. The idea is to insulate the large capacitor from the large resistance associated with the output of the gain stage. Therefore, the requirements of the buffer are low input capacitance and low output impedance. Furthermore, the output voltage swing needs to extend from as low as possible to the point where it will cause the pass device to

discontinue conducting current ($V_{ds} \leq V_{o\text{-}swing} \leq V_{in}$ - 0.7 V). The lower limit is defined to provide maximum gate drive for the pass element (PMOS transistor). On the other hand, the upper limit is set by the voltage necessary to shut off the pass device, i.e., extend to just beyond the threshold voltage.

The buffer can be implemented in one of several ways. The most apparent method is through the use of a differential amplifier in a feedback configuration as illustrated in Figure 6.6 (a) and (b). Using a buffer in unity gain configuration demands that the output voltage swing requirements of the gain stage be as stringent as those of the buffer. However, a typical non-unity gain amplifier structure (gain of 5 to 10 V/V) reduces the output swing requirements of the gain stage by a factor equal to the gain of the buffer.

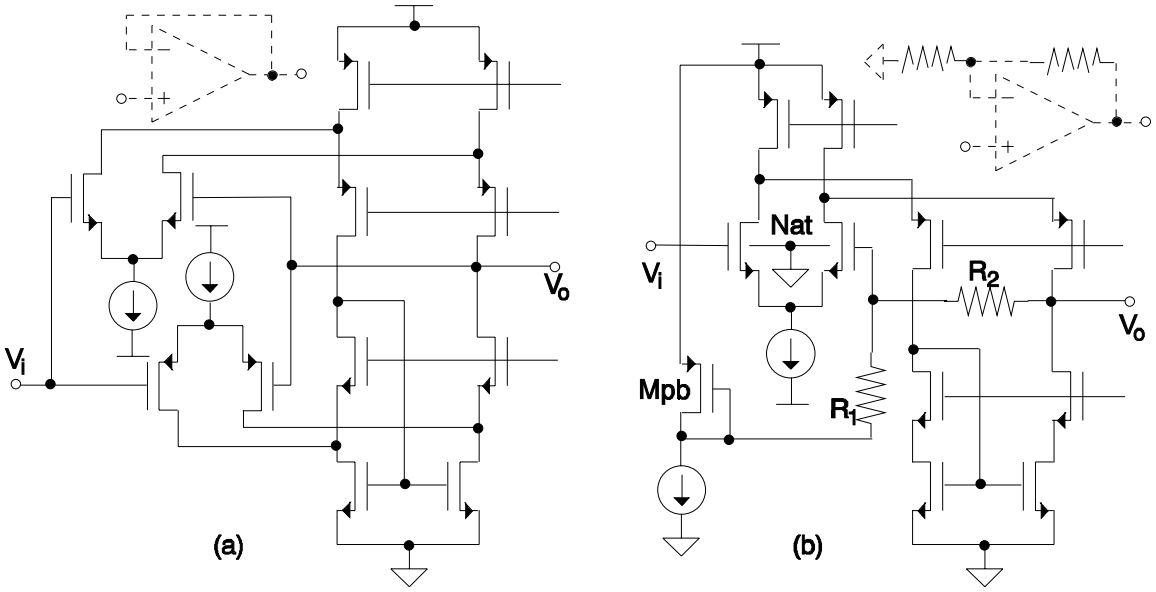

Figure 6.6. Non-inverting amplifier topologies.

This, unfortunately, comes at the expense of chip area and power consumption. In addition to the quiescent current flow associated with several transistor paths to ground,

there can be a large current flowing through the feedback resistors at high input voltages. This is because the output voltage of the buffer goes up with increasing input voltage since its magnitude is defined by the pass device to be one V_{sg} below the input voltage. As a result, the voltage across the grounded resistor in the feedback network is increased accordingly with a current flow equal to $(V_{in} - V_{sg}) / R$, i.e., 90 μA for V_{in} = 10 V, V_{sg} = 1 V, and R = 100 kΩ. Figure 6.6 (b) shows a topology that minimizes the current flow through the resistors by using an alternate ac ground whose dc value is dependent on the input voltage. The low impedance node is defined by a p-type diode connected device (Mpb). The differential pair for this alternate amplifier topology is composed of two natural NMOS transistors (non threshold adjusted devices). The threshold voltage for these natural transistors is approximately zero volts [3] thereby exhibiting good common mode range performance.

Two other amplifier buffer structures are illustrated in Figure 6.7. These circuits exploit the low threshold voltage nature of natural NMOS transistors. The circuit in Figure 6.7 (a) utilizes a current sensing resistor (R) to provide a feedback loop to the current sinking device (Mn2) via an amplifier. The resulting output impedance is

$$R_o = \left\langle \frac{R + r_{ds}}{1 + [R + r_{ds}]g_{m1}} \right\rangle \cdot \left\langle \frac{1}{1 + RAg_{m2}} \right\rangle \approx \frac{1}{RAg_{m1}g_{m2}}. \qquad (6.1)$$

This configuration has a slight advantage over the non-inverting configurations of Figure 6.6, namely, relaxed common mode range requirements for the differential amplifiers. An NPN transistor could also be used in place of the natural NMOS device if voltage swings permit. Figure 6.7 (b) shows a unique configuration where an NMOS transistor is also used as a Channel JFET (CJFET) [47]. The device operates by first creating an

inversion layer in response to an applied gate to source voltage. A subsequent change in bulk to source voltage effectively modulates the depletion region. As a result, the inversion layer is modulated accordingly thereby causing the drain current to change. The input impedance of the bulk (CJFET's input) is high as long as the bulk to source junction is not forward biased enough to turn on the parasitic bipolar transistors inherent in the device ($V_{bs} < 0.5$ V). In summary, the circuit takes advantage of the availability of a bulk terminal by using it as a feedback path. Consequently, the resulting device utilizes the gate terminal for forward signal propagation while using the bulk terminal for feedback control. The output impedance of this configuration is derived to be

$$R_o = \frac{r_{ds}}{1+\left[g_m + g_{mb}\right] r_{ds} + A g_{mb} r_{ds}} \approx \frac{1}{A g_{mb}}. \qquad (6.2)$$

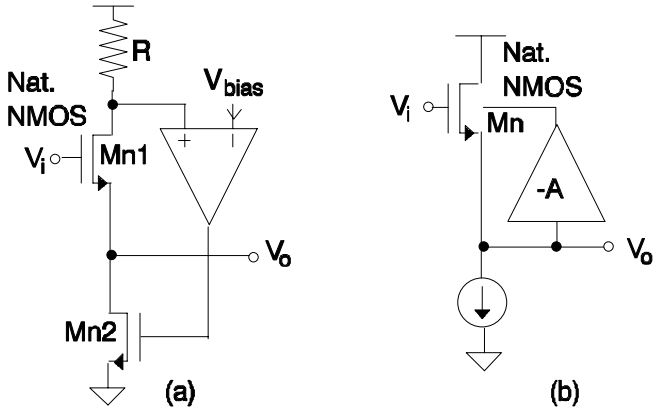

Figure 6.7. Feedback buffer structures.

The disadvantage of this configuration lies in ensuring that the bulk to source voltage of Mn is not forward biased more than 0.4 - 0.5 V. Furthermore, the bulk needs to be isolated from the substrate, which is not readily accomplished in n-well processes. However, this can be done by using a buried layer and deep n+ plugs (typically used for

the collector of NPN transistors) in a doughnut configuration. As a result, a p-epi region is isolated in which a natural NMOS device can be built. Isolation can also be achieved by using the p-base layer of NPN transistors as a p-type well. The device performance, however, is affected by the different well depth and doping density profile of the base relative to the epitaxial region.

The circuits of Figures 6.6 and 6.7 make use of a feedback amplifier to reduce output impedance without incurring excessive costs in quiescent current. However, minimum quiescent current flow is limited by the required bandwidth of the buffer, which constitutes a parasitic pole in the overall frequency response of the system. As a result, current efficiency at low load-currents is adversely affected. If the current efficient buffer introduced in chapter 4 is utilized, however, the need for a feedback amplifier within the buffer is avoided and quiescent current flow is kept at a minimum. The proposed circuit is illustrated in Figure 6.8 where the accurate current sensing circuit developed for the pass device is shared. Consequently, only two additional transistors are required to implement the current efficient buffer, namely, Qn1 and Mn3.

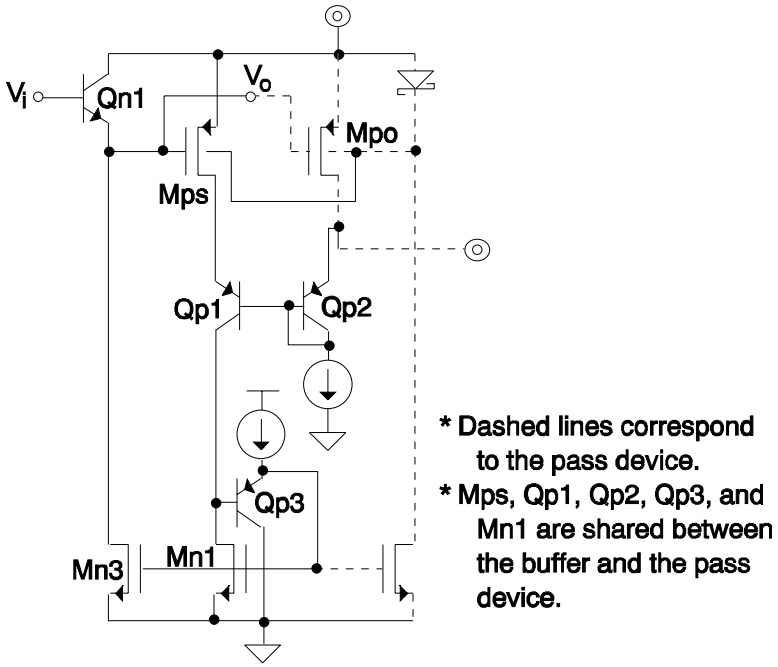

Figure 6.8. Current efficient buffer.

The buffer is essentially a class A NPN emitter follower whose bias current is dependent on load-current. The bias current dependence is achieved by a PMOS sense transistor, labeled Mps in the schematic of the current efficient buffer. Consequently, the parasitic pole introduced by the buffer exhibits the same load-current dependence as the unity gain frequency of the system. In other words, the architecture uses the minimum bias current required for stability throughout the load-current range thereby achieving maximum current efficiency and consequently yielding prolonged battery life. The load-current dependence of the quiescent current is illustrated in the simulation results of Figure 6.9 for a low drop-out regulator implementing the current efficient buffer with a simple, single stage amplifier.

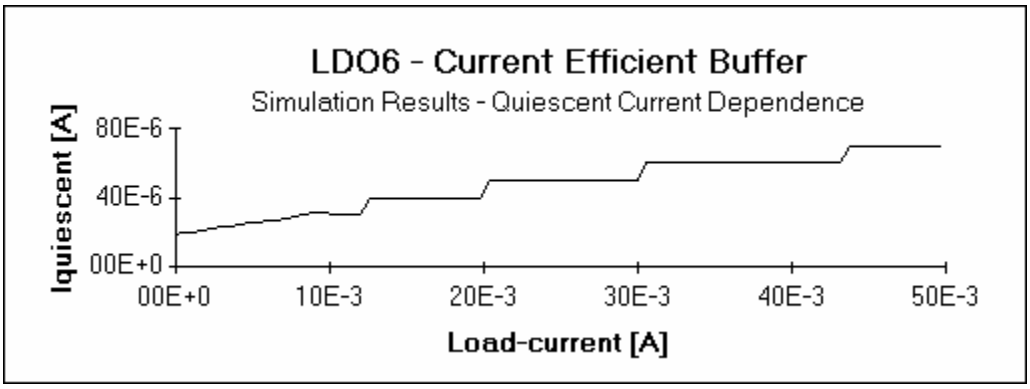

Figure 6.9. Quiescent current dependence of buffer on load-current.

Gain Stage: The gain stage of the amplifier needs a relatively small common mode range and an output swing that includes the positive supply voltage, if the current efficient buffer is assumed to be the load. The common mode range is defined around the reference voltage (V_{ref}), which in turn can be designed to be almost any value [48]. Low voltage bandgap reference topologies are discussed in chapter 5. As a result, the best device choice for a low voltage differential pair is the NPN transistor (for the case of MOSIS). This is because its base-emitter voltage drop is approximately 0.6 - 0.7 V whereas the gate to source voltage of MOS devices is roughly 0.9 V. Thus, a 0.85 - 0.9 V reference is necessary to accommodate the voltage headroom requirements of the NPN differential pair in a low voltage environment.

The choice of amplifier topology, however, is limited if the theoretical low voltage limit is to be approached ($V_{sg} + V_{ds}$). Figure 6.10 illustrates some appropriate amplifier topologies where the pole/zero pair generation discussed in chapter 4 is realized by the dashed resistor and capacitor. The single stage, five-transistor amplifier shown in Figure 6.10 (a) is simple enough to yield good frequency response for a given amount of quiescent current flow. However, a regular current mirror load presents a problem for low voltage operation. A regular mirror load, as seen in the figure, yields a transistor

stack whose associated voltage drop is $V_{sg} + V_{ce} + V_{ds}$, which is approximately between 1.4 and 1.5 V in the MOSIS technology. Therefore, a low voltage mirror load that yields the theoretical low voltage limit for the MOSIS technology is proposed ($V_{sg} + V_{ds} \approx 1$ - 1.1 V) and illustrated in Figure 6.10 (b). The mirror is the complement of the version used in the composite PMOS pass device and current efficient buffer. It is essentially a standard mirror with a V_{be} level shift achieved by an emitter follower. The current through the NPN device is designed such that the parasitic pole at the gate of the PMOS transistor is at high frequencies. This parasitic pole ($P_{parasitic}$) is approximated to be

$$P_{parasitic} \approx \frac{g_{m_{npn}}}{2\pi} \cdot \frac{1}{2C_{gs}}, \tag{6.3}$$

where $g_{m_{npn}}$ is the transconductance of the NPN transistor and C_{sg} is the gate to source capacitance of each PMOS device in the mirror. Among the amplifiers in Figure 6.10, this topology exhibits the best systematic offset performance because the voltages at the collectors of both NPN transistors in the differential pair are the same, $V_{in} - V_{sg} + V_{be}$. This results because the voltage at the input of the buffer stage (or output of the gain stage) is defined by a PMOS pass device and an emitter follower, as seen in the current efficient buffer shown in Figure 6.8. Another possible topology for the amplifier is that of a folded architecture, Figure 6.10 (c). This circuit also works properly at the theoretical limit of $V_{gs} + V_{sd}$ (equivalent to $V_{sg} + V_{ds}$). However, systematic offset performance for this circuit is poor. Furthermore, bandwidth performance per given total quiescent current flow is not as favorable as that of the circuit shown in Figure 6.10 (b) because there are more current sensitive transistor paths to ground.

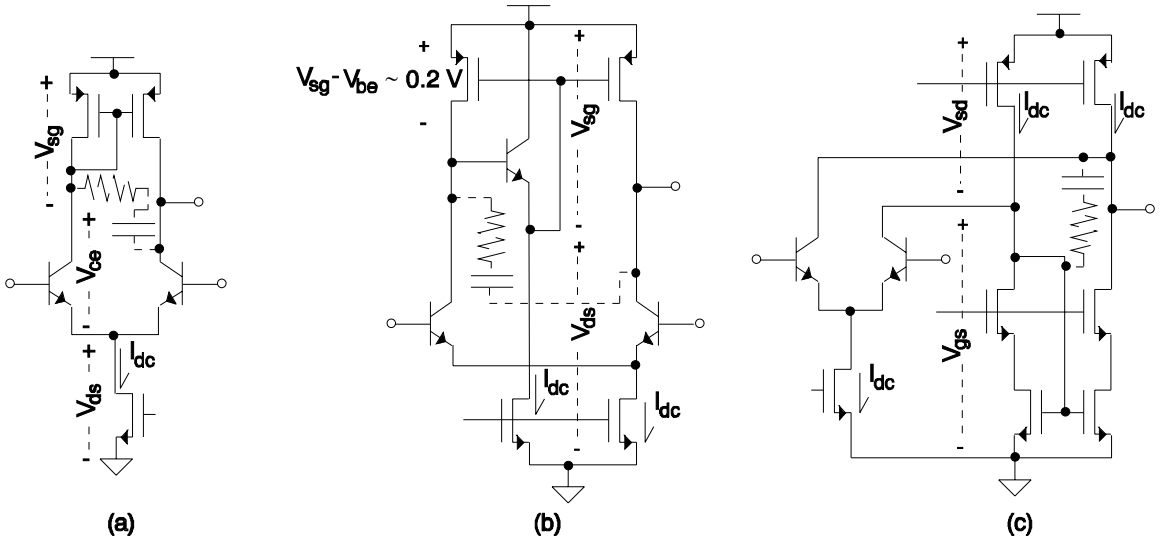

Figure 6.10. Gain stage topologies.

6.2 Reference

Current Components

An IV-mode output structure, curvature corrected bandgap reference is illustrated in Figure 6.11 (a). The proportional-to-absolute temperature (PTAT) current component is realized by Qn1, Qn2, Qn3, and R_p, which constitute a typical V_{be} loop. The base-emitter dependent current is defined by the base-emitter voltage of Qn3 and R_b. This is controlled by the negative feedback loop comprised of Qn3, Qn5, and the PMOS current mirror of Mpb1 and Mpb2. Capacitor C_c and resistor R_c are used to frequency compensate this internal feedback loop thereby ensuring stability, miller compensation. In designing the values of the capacitor and the resistor, the additional loop path composed

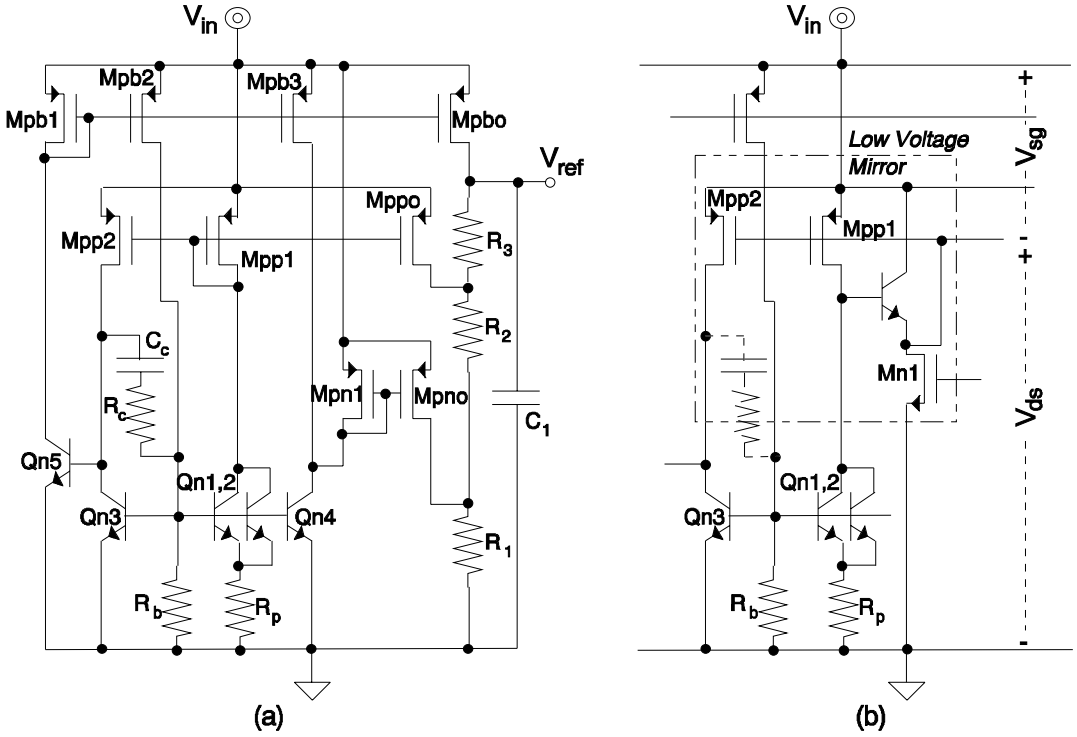

Figure 6.11. Bandgap with current subtraction curvature correction.

of Qn1, Qn2, Mpp1, and Mpp2 must be considered. Capacitor C_1 is used to limit the noise bandwidth of the reference circuit thereby reducing the overall noise content at the output of the regulator, in other words, enhancing noise performance. Finally, the nonlinear temperature dependent current is formed by Qn4 (PTAT current sink), Mpb3 (I_{Vbe} current source), Mpn1, and Mpno, which implement the current subtraction technique discussed in chapter 5. Transistors Qn3 and Qn4 constitute a linear current mirror and so do transistors Mpb1, Mpb2, and Mpb3. A resistor could be placed between the emitter of Qn4 and ground thereby making a linear current mirror with Qn1, Qn2, and R_p. The circuit simulated to have a temperature drift performance of 3.1 μV/°C and is illustrated in Figure 6.12.

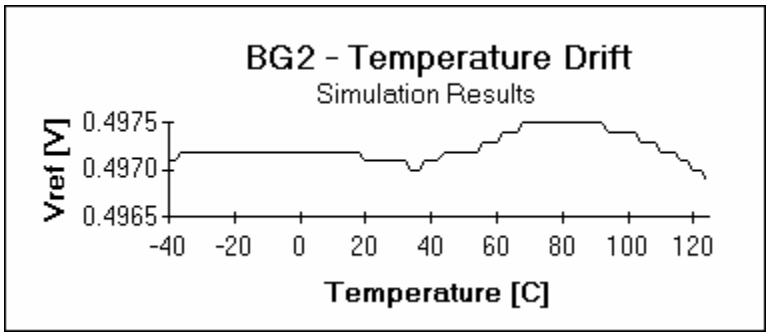

Figure 6.12. Temperature drift performance of the bandgap reference.

The realization of this circuit in MOSIS 2 μm CMOS n-well technology with a p-base layer can benefit from the use of the low voltage mirror used in the gain stage of the amplifier of Figure 6.10 (b). The minimum input voltage ($V_{in\text{-}min}$) for the bandgap cell in Figure 6.11 (a) is

$$V_{in-min} = V_{sg-Mpp1} + V_{ce-Qn1} + V_{R_p}, \tag{6.4}$$

where the voltage across R_p is relatively small, Mpp1 is in sub-threshold, and $V_{ce\text{-}Qn1}$ is approximately 0.3 V. The high saturation voltage of the NPN transistor is inherent to technologies that do not offer a heavily doped buried layer, which is the case for MOSIS. The buried layer effectively decreases the series collector resistance. Figure 6.11 (b) illustrates the circuit implications of adopting a low voltage current mirror for all PMOS mirrors used in the schematic shown in Figure 6.11 (a). The new corresponding minimum input voltage is

$$V_{in-min} = V_{sg-Mpp1} + V_{ds-Mn1}, \tag{6.5}$$

where Mn1 is simply used as a current source. Consequently, the minimum input voltage is improved by isolating the high saturation voltage of the NPN transistor from the transistor stack that determines the voltage headroom limit, which corresponds to an improvement of roughly 100 - 150 mV over the previous circuit. Thus, the minimum input voltage limit for weak-to-moderate inversion operation can be as low as 0.9 V in the MOSIS process technology. Unfortunately, the drawback is that the temperature stability of the reference is degraded because at high temperatures the input PMOS transistor, Mpp1 in Figure 6.11 (b), can go into the triode region. This results because the base-emitter voltage of the NPN device in the mirror drops faster with temperature than the source to gate voltage of the PMOS transistor. As a result, the voltage across the source and drain terminals of Mpp1 is significantly decreased at high temperatures. When this occurs, the accuracy of the mirrors defining the temperature dependent currents is reduced, which in turn degrade the ability to minimize output voltage variations throughout the specified temperature range. Consequently, reducing the minimum input voltage of this cell from roughly 1 to 0.9 V comes at the expense of accuracy.

Line Regulation Enhancement

The straight forward implementation of the current-mode bandgap relies on the high and finite output impedance of the current mirrors. Consequently, the output voltage varies as the input voltage changes because of the finite output impedance of the transistors sourcing the currents. One way to increase this output impedance is by actively cascoding the mirrors. However, a more effective method is to pre-regulate the supply voltage of the bandgap, as illustrated in Figure 6.13, which is similar in concept to the circuit in [13]. As a result, line regulation performance is ameliorated. The pre-regulator basically provides a first order voltage-mode bandgap reference. The current

through the diode connected transistor (q_1) and the resistor (R_2) is proportional-to-absolute temperature (PTAT). Consequently, the pre-regulated supply voltage of the bandgap is equal to a diode on top of a PTAT voltage drop. The disadvantage of this circuit is that the common mode range of the amplifier needs to include ground and approximately 0.5 - 0.6 V above ground, corresponding to a pre-regulated supply of 1.1 - 1.2 V. This would require the use of a complementary input amplifier to yield the desired common mode range in a low voltage environment, 1 - 1.5 V. Moreover, complementary differential pair amplifiers tend to limit the power supply voltage to approximately 1.3 V ($V_{be\text{-}NPN} + V_{eb\text{-}PNP}$) or 1.5 V ($V_{gs\text{-}NMOS} + V_{sg\text{-}PMOS}$) [47].

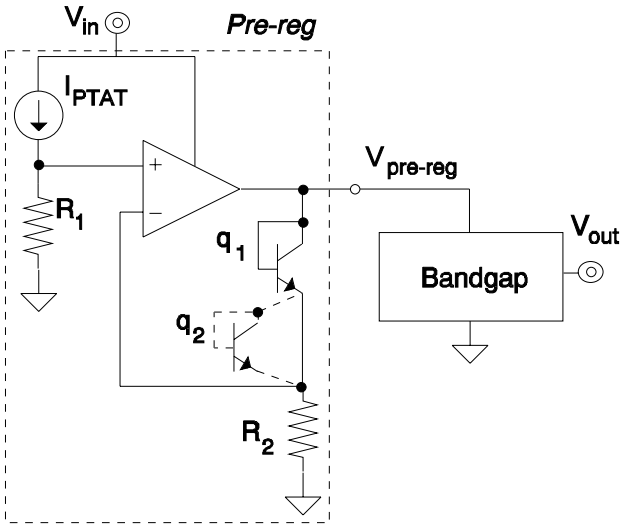

Figure 6.13. Pre-regulated supply voltage realization.

On the other hand, the pre-regulator does not need to be well temperature compensated. The current mirrors in the bandgap will have high enough output impedance to effectively reject small voltage fluctuations experienced by the pre-regulated supply ($V_{pre\text{-}reg}$). Therefore, an appropriate variation of the circuit discussed would be to use two diodes instead of one; this corresponds to adding q_2 in Figure 6.13.

As a result, a more crude and less expensive circuit is achieved (in terms of complexity and component count for the amplifier). The voltage across the resistor needs to be small thereby only requiring the use of a simple PMOS differential pair in the feedback amplifier. The new pre-regulated supply ($V_{pre\text{-}reg}$) is the sum of two diode-connected NPN transistors with PTAT collector current and one small PTAT voltage drop. This corresponds to a first order bandgap with poor temperature compensation. It is noted that $V_{pre\text{-}reg}$ (in both circuit versions) begins to decay as the input voltage approaches 1.1 - 1.2 V. Consequently, the effective line regulation of the bandgap exhibits its worst performance when the input voltage is lower than 1.2 V. Lastly, the minimum input voltage of the overall reference circuit is only degraded by one $V_{sd\text{-}sat}$ incurred between the input voltage and the pre-regulated supply. As a result, the minimum input voltage for the complete circuit is roughly 1 to 1.1 V for the MOSIS technology. Cascoding the current mirrors would have had the same effect on the minimum input voltage.

The implementation of the overall circuit is illustrated in Figure 6.14. The effects of the pre-regulated supply on line regulation performance are illustrated in Figure 6.15, 1.8 mV / 9 V and 175 mV / 9 V for the circuit with and without the pre-regulator. All the resistors can be made of any material as long as they are all the same type. Base-diffusion resistors are recommended because of their high sheet resistance and their ability to be isolated from the substrate via a well. The capacitors can be stacked to minimize area, i.e., second polysilicon layer (poly 2), first polysilicon layer (poly 1), and base-diffusion capacitors with poly 1 as one terminal and poly 2/base-diffusion as the other terminal. The n-well insulating the capacitor and the resistors can be connected to the pre-regulated supply for minimized line regulation effects. The p-channel JFET can be implemented with a long p-base as the channel, n+ diffusion as the top gate, and n-well as the bottom gate; the top and bottom gates are electrically shorted together. The

only purpose of the JFET is to provide some current for the start-up circuit to work, between 0.5 and 3 μA. The operation of the start-up circuit is based on sensing the base-emitter voltage of the NPN transistors generating and defining the temperature dependent currents and ensuring that they are operating at a non zero state by feeding back a current, typical concept of bi-stable start-up circuits.

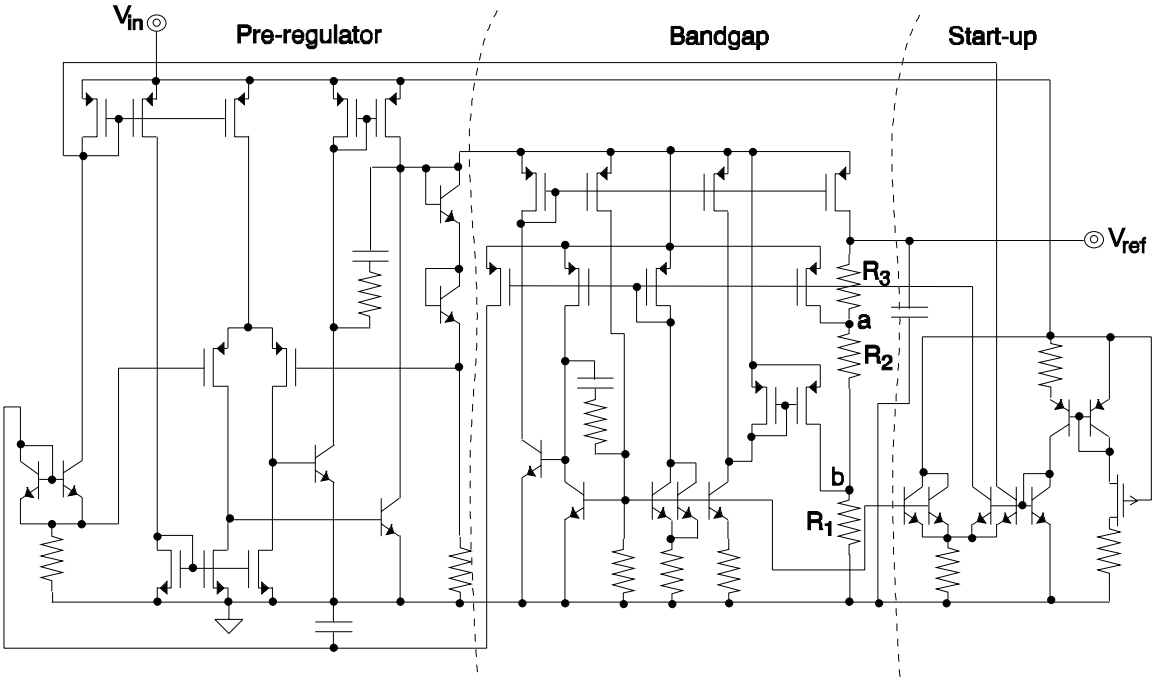

Figure 6.14. Low voltage curvature corrected bandgap.

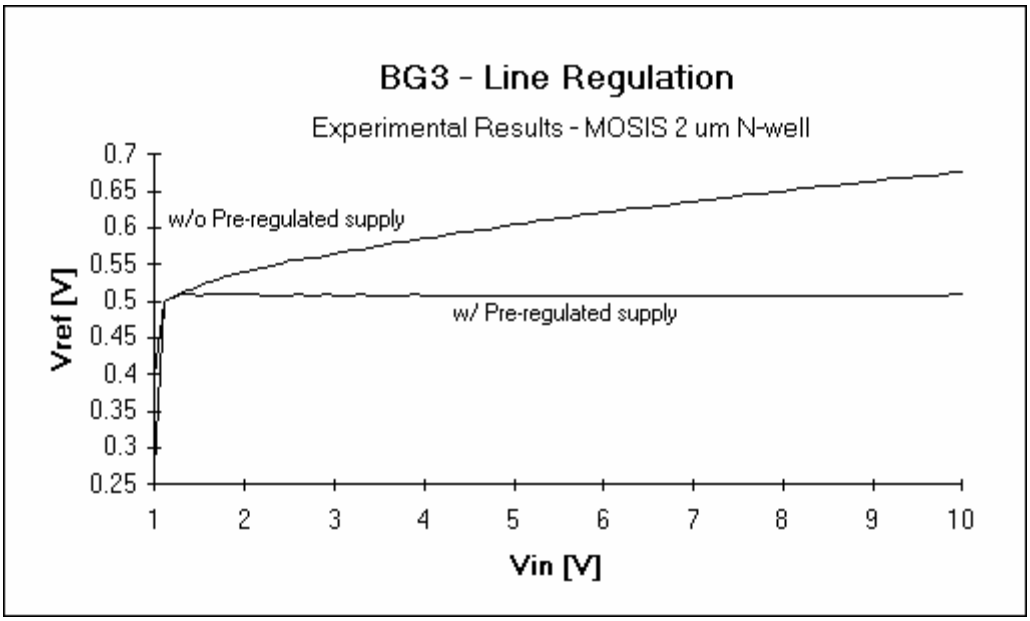

Figure 6.15. Line regulation performance of the bandgap with and without the pre-regulator.

Trimming

The output voltage as well as the temperature coefficients of the individual components can be trimmed by simply changing the resistor ratios at the output. Temperature compensation is achieved by trimming throughout the temperature range. Data points are collected for the voltages at V_{ref}, node "a", and node "b" (from Figure 6.14) throughout the temperature sweep. At this point, the currents multiplied by an initial reference resistor can be extrapolated since the initial resistor ratios and the voltages across the resistors are known,

$$I_{V_{be}} R_{2_{initial}} = \frac{V_{ref} - V_a}{\left\langle \frac{R_3}{R_2} \right\rangle_{initial}}, \tag{6.6}$$

$$I_{PTAT} R_{2_{initial}} = [V_a - V_b] - I_{V_{be}} R_{2_{initial}}, \tag{6.7}$$

and
$$I_{NL} R_{2_{initial}} = \frac{V_b}{\left\langle \frac{R_1}{R_2} \right\rangle_{initial}} - [V_a - V_b], \tag{6.8}$$

where I_{Vbe}, I_{PTAT}, and I_{NL} are the temperature dependent currents flowing through the output resistors R_1, R_2, and R_3 while V_a and V_b correspond to the voltages at nodes "a" and "b". These derived voltages exhibit temperature characteristics that are independent of the temperature coefficient of the resistors, as discussed in the IV-mode output structure section of chapter 5. Thus, the coefficients of each component can be extracted and manipulated to yield proper temperature compensation by means of a computer. The reference voltage can be expressed as

$$V_{ref} = I_{V_{be}}[R_1 + R_2 + R_3] + I_{PTAT}[R_1 + R_2] + I_{NL} R_1. \tag{6.9}$$

This relationship can be adjusted to use the values derived in equations (6.6) - (6.8) and illustrate the appropriate coefficients that can be manipulated to yield a curvature corrected reference voltage,

$$V_{ref} \frac{R_{2_{initial}}}{R_2} = I_{V_{be}} \left\langle \frac{R_1}{R_2} + \frac{R_2}{R_2} + \frac{R_3}{R_2} \right\rangle R_{2_{initial}} +$$

$$I_{PTAT} \left\langle \frac{R_1}{R_2} + \frac{R_2}{R_2} \right\rangle R_{2_{initial}} + I_{NL} \left\langle \frac{R_1}{R_2} \right\rangle R_{2_{initial}}, \tag{6.10}$$

or $$V_{ref}\frac{R_{2_{initial}}}{R_2} = AI_{V_{be}}R_{2_{initial}} + BI_{PTAT}R_{2_{initial}} + CI_{NL}R_{2_{initial}} \qquad (6.11)$$

where A, B, and C are the extracted coefficients. Once values for these coefficients are obtained by using a computer, new resistor ratios for R_1/R_2 and R_3/R_2 can be derived.

The next and final step in the trimming procedure is to adjust the magnitude of the output voltage at room temperature or at whatever temperature desired. This can be accomplished by changing the ratio of the initial and the final values of R_2 ($R_{2_{initial}}/R_2$). This value is determined by using the resistor ratios previously derived and the voltages obtained at room temperature (V_{ref}, $I_{V_{be}}R_{2_{initial}}$, $I_{PTAT}R_{2_{initial}}$, and $I_{NL}R_{2_{initial}}$) and solving for $R_{2_{initial}}/R_2$. It is noted that knowledge of the absolute value of the resistors is not necessary. Instead, the intrinsic parameters that require control are the ratios of the resistors. The trimming algorithm has been successfully implemented by way of a spreadsheet and whose procedure is described in appendix B.

The procedure not only trims the absolute magnitude of the reference but it also performs temperature compensation. The disadvantage of this algorithm lies in the cost involved, namely, spending the time and allocating the equipment to trim the circuit over a specified temperature range. This could be avoided by only trimming for the voltage magnitude at room temperature and relying on simulations for proper temperature compensation. Typical trimming procedures only do the latter. Furthermore, the aforementioned trimming technique can optimize temperature compensation for any set of current components independently of their individual temperature dependencies by merely adjusting resistor ratios at the output.

6.3 Summary

This chapter used the concepts developed in chapters 4 and 5 to design the circuits for the control loop and the reference of the system. Different devices were considered for the pass device leading to the conclusion that PMOS transistors are the most appropriate for low drop-out voltage performance and low quiescent current flow. This was followed by the implementation of the current boosting technique. Different architectures were also studied for the buffer of the amplifier. This culminated in the realization of the class A current efficient buffer. A circuit was also designed for the frequency shaping gain stage. The circuit development of the reference was then addressed. Lastly, the chapter discussed the trimming implications of the reference circuit designed. The process of translating the circuit blocks designed into a system is described in chapter 7.

CHAPTER VII

SYSTEM DESIGN

In assembling the circuits onto a system, there are several issues that need special attention. Physical layout design and circuit protection techniques are two such issues. General layout notes pertaining to the circuit blocks and associated interconnects are therefore discussed in this chapter. A section is also allocated to illustrate the different methods of protection, such as overload current, reverse battery, and thermal protection. Their feasibility in a low voltage and low quiescent current environment is evaluated. Lastly, experimental results of the system designed are illustrated and evaluated.

7.1 Block Level Diagram

The low voltage and low quiescent current circuits developed in chapters 4 and 5 and designed in chapter 6 are used to assemble the system illustrated in Figure 7.1. The reference is composed of a pre-regulator and a curvature corrected bandgap cell. There is also a start-up circuit associated with the overall reference. The amplifier is composed of a frequency shaping gain stage and a current efficient buffer. The pass device is a PMOS power transistor whose performance is enhanced by a current boosting circuit. Part of the circuit forming the pass device is common to the current efficient buffer but is distinctly separated in the figure for clarity. Finally, three common forms of protection are included in the drawing. They include overload current protection, reverse battery

protection, and thermal shutdown protection. As a whole, they ensure that the system operates under safe and stable conditions. Most of the protection, however, revolves around the power transistor. This is because the pass device is usually the most susceptible to extreme environmental and loading conditions.

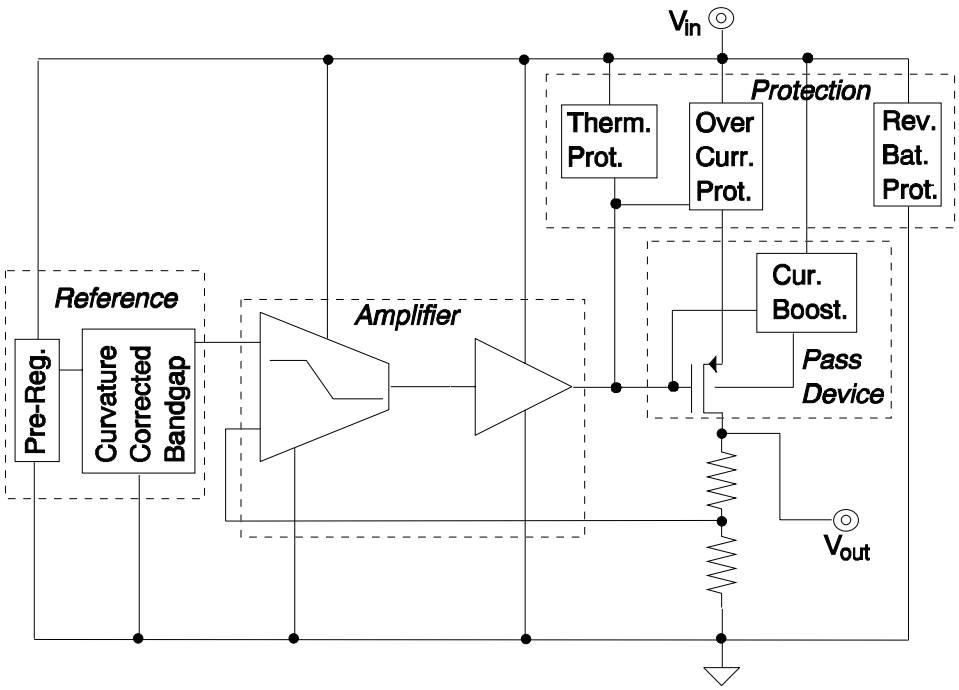

Figure 7.1. Complete system block level diagram.

7.2 Physical Design Issues

The effects of parasitic devices inherent in the layout could prove to be catastrophic for the overall performance of the system. This is especially true when considering the current density, the power dissipation, and the generated heat associated with power supply circuits. Furthermore, stray capacitance, parasitic resistance, and lead inductance can affect the system by altering the frequency response behavior and possibly causing spurious oscillations [21]. As a result, the layout should be compact and

lead lengths should be kept short. Moreover, ground loops must be avoided [19]. Their effects can be mitigated by careful element placement and by ensuring that ground contacts and interconnect paths are low resistance. Heat distribution, especially throughout the area where the power transistor lies, also deserves attention. This is to prevent "hot spots" from being generated on the power device that could cause second breakdown. Moreover, reliability issues with current density in the input and the output terminals of the regulator are intrinsic to the life of the circuit.

The output noise of the system can be significantly degraded by poor layout techniques, especially in mixed-signal integrated circuits. Digital functions in mixed-signal chips are significant sources of noise for analog circuits. They exhibit large momentary surges of current that produce noise on the supply lines and the substrate. Two techniques that are appropriate for minimizing this injected noise are separation of power supply lines and physical layout isolation of circuits. The digital and analog supply lines can be separated throughout the chip and connected externally or at the package level [19]. This is to prevent most of the noise voltage generated by the large surges of current flowing through stray inductors and parasitic resistors from appearing in the analog lines. Isolation can be used to relieve the noise injected through the substrate. This can be realized by placing a deep diffusion ring around the analog circuits and by placing the analog traces as far away as possible from any digital line. Noise at the load is also negatively affected by series lead inductance and resistance. This noise manifests itself in the form of voltage drops across the line resulting from dc and transient load-current changes ($\Delta I_{Load}R_{Lead} + L_{Lead}\partial I_{Load}/\partial t$). Thus, this type of noise is reduced by keeping the output lead to the load short and by reducing its resistance [19].

Almost all parasitic devices in the power pass device serve to degrade the overall performance of the low drop-out regulator. Series source and drain resistance associated

with the metal traces, diffusion links, and contacts increase the drop-out voltage; in other words, they increase the "on" resistance of the transistor. Thus, low resistive paths for the source and drain terminals are necessary. The parasitic capacitance of the gate of the power PMOS is especially important for system stability. The result of increased capacitance can be spurious oscillations. Consequently, unnecessary gate area should be eliminated. The parasitic effects of the bipolar transistors inherent in the power PMOS transistor are especially apparent when the source to bulk junction is forward biased, which is done for current boosting. Therefore, a highly doped buried layer, if available, should be placed underneath the whole device to decrease the current gain of the parasitic bipolar transistors as well as decrease the bulk resistance. Well contacts should be placed throughout the device to aid in reducing bulk resistance. Lower bulk resistance prevents excessive bulk to source forward biasing conditions thereby minimizing the parasitic effects of the bipolar devices. Furthermore, the size of the schottky diode used to forward bias this junction needs to be large enough to exhibit a voltage drop that is well below a base-emitter voltage, i.e., $V_{schottky} \approx 0.3$ V. This leads to a reduction in unnecessary ground current. Consideration must also be given to thermal symmetry of the overall physical layout. The power device may be divided in two and the other circuit blocks may be placed in the center. Moreover, current densities must be equally distributed throughout the pass device to prevent "hot spots" from developing.

The placement and particular layout of the reference and error amplifier also require scrutiny. The reference circuit should be close to the input of the amplifier. This is especially true for the output capacitor of the reference. This is to reduce the noise content generated by the reference circuit and parasitic trace resistance, which is seen by the input of the amplifier and reflected to the output of the regulator. The location of the reference with respect to the overall chip also merits consideration. This influences the

package induced drifts. The variation of the reference voltage is degraded by the physical stresses exerted on the chip by the package. These effects can be minimized if post-package trimming is allowed. The input pair and the mirror load of the amplifier's gain stage should be well matched to minimize input offset voltages, which degrade overall accuracy performance. The integrated capacitors utilized throughout the chip can be stacked to minimize area overhead. These capacitors are implemented by using three parallel plates (poly 2, poly 1, and p-base diffusion) isolated by an n-well. The bottom plate (p-base diffusion) and the top plate (poly 2) are electrically shorted together and constitute one terminal of the capacitor; the other terminal is the middle plate (poly 1). The terminal composed of the extreme plates should be connected to the lowest impedance node to minimize the effects of the innate parasitic capacitance to the n-well. The output of the gain stage and the input of the buffer should be as close as possible. This is to reduce stray capacitance that could pull the respective parasitic pole to low frequencies. Similarly, the buffer should be placed as close as possible to the power PMOS pass device. This not only affects stability by pole movement but also affects maximum output voltage variation arising from transient load-current steps by degrading slew-rate performance. It is important to keep in mind, however, that the gate capacitance associated with the power transistor usually overwhelms the interconnect capacitance between the buffer and the pass device.

The location and the layout of the protection circuits should reflect minimal effects on regulator performance. The current sensing device associated with the overload current protection is typically a series element. Thus, its associated voltage drop must be minimized to prevent it from significantly increasing drop-out voltage. As a result, low resistive terminals capable of handling large current densities should be implemented for the current sense device. Lastly, the temperature sensing element

associated with thermal shutdown protection should be placed as close as possible to the power device to ensure proper operation of the protection circuit.

7.3 Protection

An important aspect to consider when designing regulators is protection against undesirable factors that are inherent to the working environment of the application. Since the power pass device dissipates the most power, protection usually revolves around its operating conditions. The operating limits of the device are defined by power dissipation, output current range, breakdown voltage, temperature rating, and second breakdown effects [1]. Second breakdown results from the presence of "hot spots" or large thermal gradients, a consequence of uneven distribution of current densities throughout the power transistor. Protection circuitry is typically inactive during safe operating conditions and becomes active only if a safety limit is violated. The most common forms of protection include overload current protection, reverse battery protection, thermal shutdown protection, and electrostatic discharge (ESD) protection. The safety limits of output current and voltage drop across a transistor are combined to describe the safe operating area (SOA), typically illustrated by a graph of $V_{ec}[V_{sd}]$ versus $I_c[I_d]$ [21]. Protection against overheating, current overloading, and extreme voltages constitute the "watchdog" circuitry otherwise known as SOA protection. In other words, SOA protection ensures that the power transistor works within safety limits. Most of these circuits are realized easily and in a cost efficient manner. However, caution must be exercised not to significantly degrade the performance of the regulator during normal conditions by the mere presence of the protection. For instance, current limiting typically requires a current sense resistor in series with the power transistor. As

a result, the drop-out voltage of the regulator is deteriorated by the load dependent voltage drop across the resistor.

Overload Current Protection

Overload protection ensures that the current through the power transistor stays within a specified range. A violation of this could result in damage or destruction of the device. The simplest form of overload current protection is a fuse-link [49]. When the load-current exceeds the rated current of the fuse, the heat generated melts the metallic link thereby causing an open circuit. The drawback of this method is that replacement of the link is necessary once the fuse is blown, which is not acceptable for most integrated power supply applications. Figure 7.2 (a) illustrates a more appropriate structure for integrated circuits [1, 2, 3, 6]. The maximum current is defined by the bipolar transistor and the resistor, $I_{o\text{-}max} = V_{be} / R_s$. Transistor Qn1 [Qp1] is off during normal operating conditions. However, when the load-current increases to the point where the voltage drop across R_s is roughly 0.7 V (equivalent to one V_{be}), then the transistor conducts current.

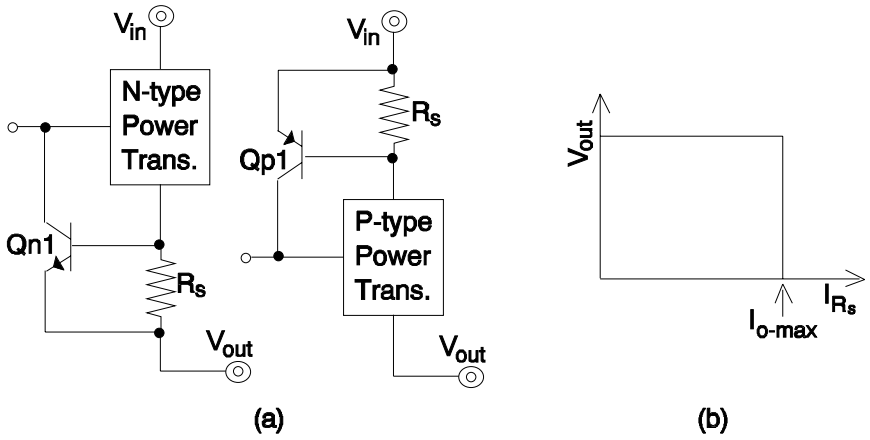

Figure 7.2. Current limiting circuit protection.

The device pulls down [pulls up] the input terminal of the power device to prevent it from conducting more current. The resulting voltage to current relationship is illustrated in Figure 7.2 (b). The maximum power dissipation of the power transistor occurs when the output is short circuited to ground, which corresponds to a voltage drop across the device equal to the input voltage,

$$P_{o-max} = \left[V_{in} + V_{out}\right] I_{o-max} = V_{in} I_{o-max}, \tag{7.1}$$

where the terminology of the figure is adopted. One disadvantage of this configuration is the deterioration of the drop-out voltage by the voltage drop across the resistor R_s.

The drop-out voltage loss can be minimized by implementing the circuit of Figure 7.3 (a) [6, 50]. In this case, R_s can be small because the threshold voltage (voltage across R_s, $V_{threshold}$) needed to activate the protection circuit can be defined to be small by appropriately proportioning resistors R_1 through R_4,

$$V_{threshold} = V_{in}\left\langle 1 - \frac{R_2\left[R_3 + R_4\right]}{R_4\left[R_1 + R_2\right]}\right\rangle. \tag{7.2}$$

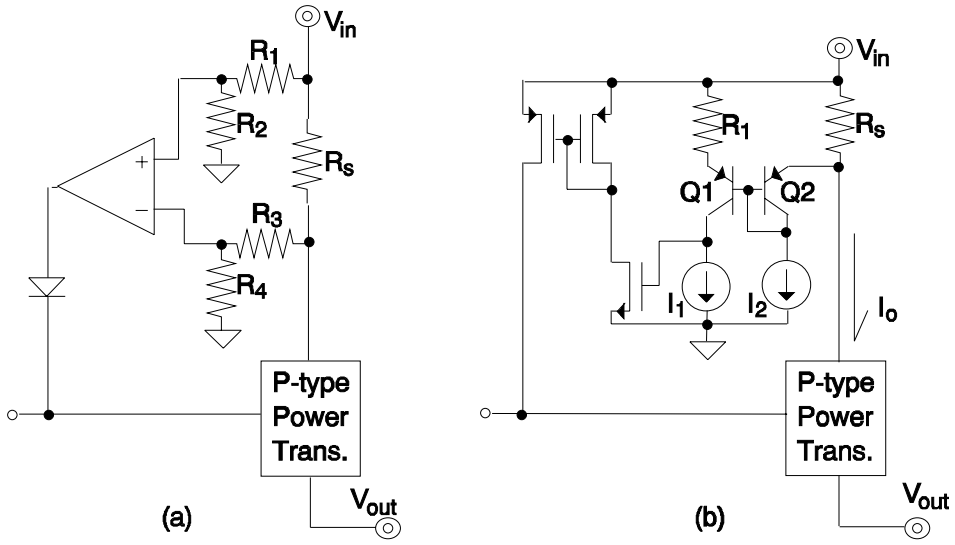

Figure 7.3. Low voltage current limiting circuit protection.

The drawback of this low voltage circuit is the additional quiescent current flow and chip area associated with the amplifier and the resistors. Figure 7.3 (b) illustrates one somewhat simpler form where quiescent current flow is appreciably low, approximately $I_1 + I_2$. Circuit elements Q1, Q2, and R_1 constitute a comparator whose threshold voltage is defined by I_1R_1 and triggered by I_oR_s.

The maximum power dissipation rating for a power transistor, constrained by the input voltage and the maximum output current ($V_{in}I_{o\text{-}max}$) for the case of Figures 7.2 and 7.3, determines the maximum output current capability of the regulator ($I_{o\text{-}max}$). This restriction could be relaxed, however, if a foldback current limiting scheme is implemented, as illustrated in Figure 7.4 [2]. The idea is to make the maximum allowed output current, during overload conditions, a function of the output voltage. Consequently, the maximum current permitted (current through R_s, I_{R_s}) is reduced as the output voltage is decreased. The resulting relationship can be expressed as

$$I_{R_s} = \frac{V_{be}[R_a + R_b]}{R_b R_s} + \frac{V_{out} R_a}{R_b R_s} = I_1 + \frac{V_{out} R_a}{R_b R_s} \tag{7.3}$$

and graphically illustrated in Figure 7.4 (b) where I_1 is the maximum current allowed when the output is electrically shorted to ground. The worst-case power dissipation can be designed to be $V_{in}I_1$ as opposed to the higher $V_{in}I_{o\text{-}max}$ of the non foldback configuration. Consequently, the maximum output current only occurs when the output voltage is at its nominal value and not when the output is short circuited to ground. In other words, the maximum power dissipation for a given maximum output current is lower for a foldback current limiting scheme than other common realizations. Figure 7.4 (c) shows another implementation of the foldback technique adopting the low voltage concept of the circuit illustrated in Figure 7.3 (a). The corresponding threshold voltage for this configuration is a function of the output voltage and is expressed as

$$V_{threshold} = V_{out}\left\langle \frac{R_4[R_1 + R_2]}{R_2[R_3 + R_4]} - 1 \right\rangle. \tag{7.4}$$

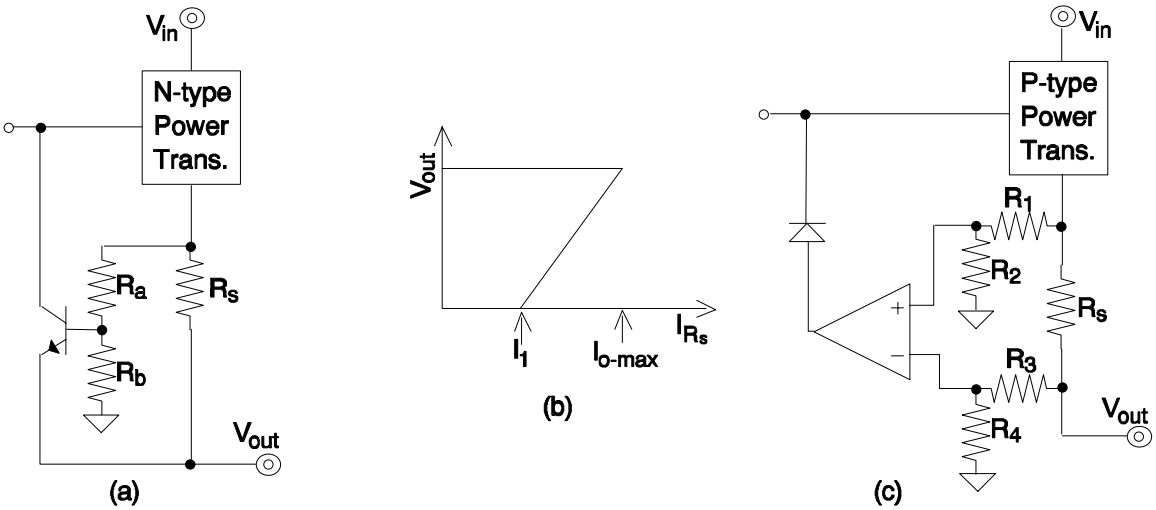

Figure 7.4. Foldback current limiting circuit protection.

Reverse Battery Protection

The backward installation of batteries is a common occurrence that could irreparably damage a chip if precautions are not taken. Figure 7.5 illustrates different forms of circuit protection against battery reversal [49]. The first one is a diode in series with the battery, Figure 7.5 (a). When the battery is reversed, the diode is reversed biased and therefore discontinues to conduct current. The drawback of this circuit, however, is the diode voltage loss during normal operation; in other words, the voltage seen by the circuits is V_{in} - V_{be} instead of V_{in}. This is especially detrimental to low drop-out regulators. The second version uses a shunt diode between the terminals of the battery, Figure 7.5 (b). In this case, there is a large amount of current flowing through the diode when the battery is reversed. Though this is an effective method of protection, the battery could be totally drained during prolonged periods of reverse battery operation. On the other hand, the input voltage is not degraded during normal operating conditions.

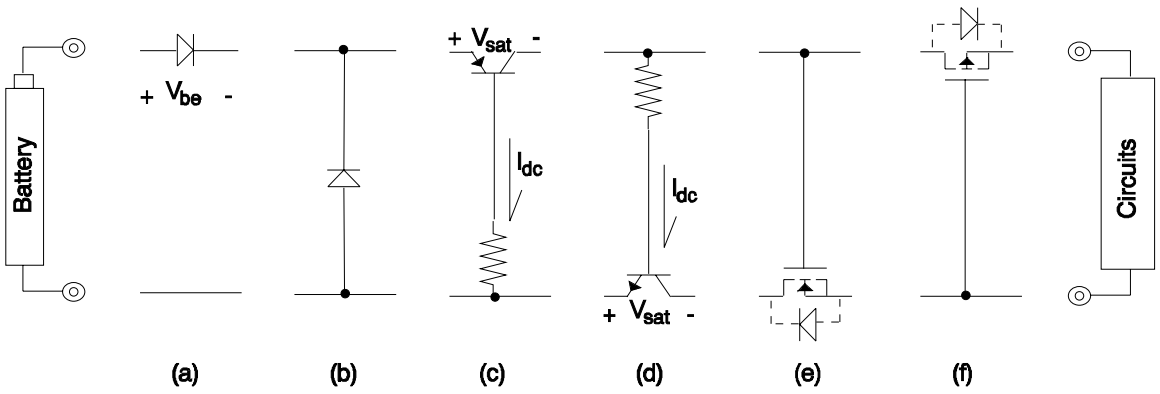

Figure 7.5. Reverse battery protection circuits.

Other forms of reverse battery protection include the use of three terminal switches, such as bipolar and MOS transistors. Figure 7.5 (c) shows a high side PNP

transistor switch. During normal operation, the transistor is in the forward active region exhibiting a small voltage loss equal to one V_{sat}. During reverse battery operation, the emitter-base junction is reversed biased and the transistor discontinues current flow. The voltage loss across the transistor during normal conditions, though small, can be notable in a low voltage environment. Furthermore, the current flow through the resistor during proper operating conditions may be significant enough to increase the quiescent current overhead. As a result, the current efficiency of the loading circuits is decreased thereby reducing battery life. A low side version of the PNP configuration is implemented in Figure 7.5 (d). The advantage of the low side circuit, is that the forward current gain (β) of the power NPN transistor is typically larger than that of the PNP counterpart, which leads to lower quiescent current flow. This, however, comes at the expense of a non-zero voltage for the ground terminal of the loading circuits.

Figures 7.5 (e) and (f) show the MOS versions of reverse battery protection. It is noted that the bulk terminals are connected to the drains instead of the sources. This is done to prevent any current from flowing through the intrinsic diode (formed by the p-bulk and the n+ diffusion) to the loading circuits during reverse battery operation. If this was not the case, current could still flow through the switch. The advantage of the MOS configurations over the bipolar versions is that there is no net current loss during normal operating conditions thereby leaving quiescent current flow and battery life intact. However, MOS devices need to be large to exhibit low resistance, in other words, low saturation voltage at high currents. This is especially cumbersome in a low voltage environment where gate drive is diminished. This could be alleviated by the use of a charge pump at the cost of complexity, quiescent current flow, and chip area. Consequently, the low side version using the NMOS device is more appropriate because of its inherently lower "on" resistance.

The series diode, bipolar switches, and MOS switches are not well suited for a low voltage, low drop-out regulator. The series diode and the high side switches of Figures 7.5 (a), (c), and (f) exhibit voltage losses that degrade the drop-out voltage of the regulator by a V_{be}, a V_{sat}, or a $V_{sd\text{-}sat}$ respectively. The low side switch versions, Figures 7.5 (d) and (e), similarly exhibit voltage losses on the ground terminal. For instance, if the minimum input voltage of the regulator is 1 V, then the battery voltage must be greater than 1 V + V_{sat} [$V_{ds\text{-}sat}$], which can be approximately 1.1 - 1.2 V. Furthermore, the dc current loss in the bipolar switch versions of Figures 7.5 (c) and (d) are inappropriate for a low quiescent current environment. As a result, the most appropriate circuit for current efficient, low voltage, low drop-out regulators is the shunted diode of Figure 7.5 (b). The only disadvantage of this circuit is that its current flow during reverse battery operation is large. However, this would only drain the battery considerably if the reverse battery condition persists for a prolonged period of time.

Thermal Shutdown Protection

Environmental or loading conditions can cause the regulator and most specifically the power transistor to operate under extreme temperatures that can cause damage to the circuit. Thermal shutdown protection circuits prevent such an occurrence from happening. The main concept is to sense the temperature of the chip and trigger a protective course of action only when the temperature exceeds a specified value. Figure 7.6 illustrates one such configuration where an NPN transistor is used as a sense switch, a

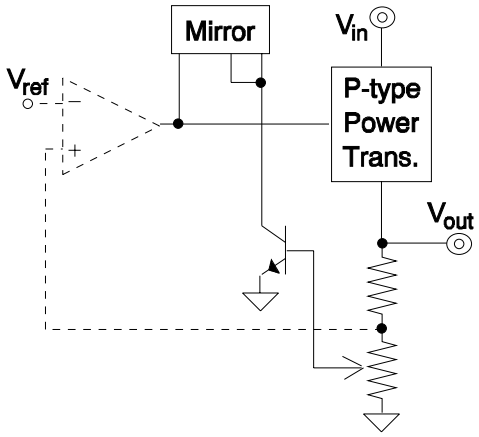

Figure 7.6. Thermal shutdown protection circuit.

modified version of [1]. The temperature dependence of the base-emitter voltage of the transistor can be approximated to be -2.2 mV/°C. Thus, if the threshold temperature is roughly 150 °C, then the base of the transistor must be biased at a voltage of approximately 400 mV. Consequently, the NPN device is off when the temperature is below 150 °C. When the temperature limit is exceeded, however, the transistor conducts current and shuts off the power device. The threshold temperature is not accurate because the bias voltage of the base may exhibit considerable temperature drift. Accurate performance is most likely specified only for a lower temperature range. Furthermore, the trigger temperature increases during drop-out conditions. This can be avoided by taking the bias voltage of the base from the reference circuit instead of the output of the regulator. Lastly, the thermal sensing transistor must be physically close to the power device. This is done to accurately sense the temperature of the device.

7.4 Experimental Performance

Figures 7.7 and 7.8 illustrate the circuit realization of the system shown in Figure 7.1 with the exception of the protection circuit. These were fabricated in MOSIS 2 μm

CMOS technology with an added p-base layer. The plots of the layout are illustrated in appendix C. The protection circuitry was not included in the circuit for two reasons: (1) it is not the focus of the research and (2) its presence could hamper the evaluation of the circuit techniques implemented in the design. However, electrostatic discharge (ESD) protection was included to ensure reliability during laboratory experiments. The passive components of the reference (Figure 7.8) and the schottky diode of the control loop (Figure 7.7) were implemented discretely for greater testing and trimming flexibility.

Figures 7.9 through 7.23 describe the performance achieved by the system designed. Figure 7.9 illustrates the line regulation performance of the control loop, roughly 1.05 mV/V. The performance was approximately the same with and without implementing the current boosting technique. However, the minimum input voltage improved from 1.32 to 1.2 V for a maximum load-current of 50 mA by using the current boosting technique, corresponding to an improvement of roughly 10 %. Figure 7.10 shows the minimum operating voltage of the control loop. The circuit works down to a voltage of approximately 1 V while generating an output current of 19 mA. The minimum input voltage for the non current boosted version was approximately 1.125 V. The drop-out voltage performance is depicted by Figure 7.11. The circuit achieved a drop-out voltage of 232 mV at 60 mA of load-current, which corresponds to an improvement of roughly 17 % over its non current boosted counterpart. In other words, the pass device exhibited an "on" resistance of 3.9 Ω.

The circuit achieved a load regulation performance of roughly 0.38 mV/mA, which is illustrated in Figure 7.12. The figure shows the performance at 1 and 1.2 V as well as with and without implementing the current boosted technique. The maximum load-current for an input voltage of 1 and 1.2 V is 18 and 50 mA respectively. This is approximately a 67 to 85 % improvement over its non current boosted version. Figure

7.13 shows the quiescent current flow as a function of load-current. Quiescent current at zero load-current was 23 μA whereas it peaked at 230 μA during maximum load-current conditions. The increase in current is expected because of the load-dependent current flow of the buffer and the schottky diode. The maximum quiescent current without implementing the current boosting technique was approximately 50 μA. The non current boosted circuit's quiescent current flow started dropping at a load-current of 30 mA, which corresponds to its maximum output current capabilities. The large difference in maximum quiescent current flow between both circuit versions results from the parasitic ground current flowing through the vertical bipolar devices inherent in the layout of the power PMOS transistor. This was considerable because the schottky diode was not large enough to exhibit lower diode voltage drops, $V_{diode} \approx 0.45$ - 0.5 V. The absence of a buried layer also aggravated the phenomenon by not degrading the current gain of the parasitic bipolar devices.

Figure 7.14 illustrates the transient performance of the circuit upon a load-current step transition. The load-current was stepped from 0 to 50 mA and vice versa. The maximum output voltage variation of the circuit was 19 mV, shown by trace B. The same circuit but without the aid of load dependent biasing in the current efficient buffer showed a variation of 148 mV. Therefore, the benefits of the current efficient buffer in the LDO for a given amount of quiescent current flow can be roughly quantified to yield an improvement of 87 %. In other words, the quiescent current flow at low load-currents for a given output voltage variation is significantly reduced by utilizing the current efficient buffer. Figure 7.15 shows the output noise voltage of the control loop. The noise voltage peaks at roughly 3 $\mu V/\sqrt{Hz}$ at 100 Hz and continuously drops as the frequency increases. This 1/f noise behavior is typical to linear regulators and appropriate for the frequency response of the system. Table 7.1 summarizes the

parameters that were affected by the current boosting technique and the load dependent biasing of the current efficient buffer. The only drawback to the enhancing techniques developed is the large quiescent current flow during high load-current conditions. Its effect on battery life, however, is negligible because the total current drain is dominated by the large load-current, $I_{drain} = I_{Load} + I_{quiescent} \approx I_{Load}$ (high current efficiency).

The behavior of the temperature dependent current components of the reference are shown in Figure 7.16. The nonlinear component (I_{NL}) performs as expected, off during the first part of the temperature range and on during the latter part. The resulting, untrimmed temperature drift performance is roughly 32 μV/°C, as illustrated in Figure 7.17. This was improved to approximately 8.6 μV/°C after the trimming procedure was implemented, as shown in Figure 7.18. The resulting performance was not as good as theoretically predicted by simulations. This may be attributed to the temperature effects of the start-up circuit. The effect of the temperature drift of the input offset voltage of the error amplifier could have been diminished by trimming the reference to compensate for it. As is, trimming for the bandgap reference did not take this into account. This would have improved the overall temperature drift performance of the system. Figure 7.19 shows the proper functioning of the start-up circuit. The input voltage was slowly ramped from 0 to 1.3 V and the reference voltage reached its specified value at an input voltage of approximately 1.1 V.

Figure 7.20 shows the line regulation performance of the reference, which was approximately 204 μV/V. Figure 7.21 shows a close-up to demonstrate the corresponding minimum input voltage of roughly 1.1 V. Line regulation performance exhibits the worst degradation as the input voltage approaches 1.1 V. This was expected because the voltage of the pre-regulated supply within the reference is defined to be between 1.1 and 1.2 V. As a result, the pre-regulator goes into drop-out when the input

voltage reaches 1.1 V. Figure 7.22 shows the quiescent current of the reference as a function of input voltage. The current peaks at 14 μA, which corresponds to an input voltage of 1.1 V. It peaks at this value because the pre-regulator goes into drop-out. This current does not include the current incurred by the JFET in the circuit. The JFET was implemented discretely but its realization in MOSIS can be made by a p-base channel, an n+ diffusion top gate, and an n-well bottom gate. The p-base can be laid out as a resistor exhibiting high resistance. The p-channel JFET can be designed to define a current between 0.5 and 3 μA in the configuration shown in the schematic of the reference. Consequently, the maximum quiescent current flow of the reference including the JFET is approximately 17 μA.

Figure 7.23 shows the output noise voltage performance of the reference. The circuit shows some 1/f noise as well as significant thermal noise. The 1/f noise comes from the PMOS transistors defining the temperature dependent currents flowing through the output. Appreciable thermal noise results from the use of large resistors at the output of the reference. The noise bandwidth is defined by the load capacitor of the reference. The resulting output noise voltage starts to drop at a frequency between 6 and 10 kHz and at a rate of roughly 20 dB/dec. The overall noise content can be improved by simply reducing the noise bandwidth, which is achieved by increasing the load capacitance of the reference.

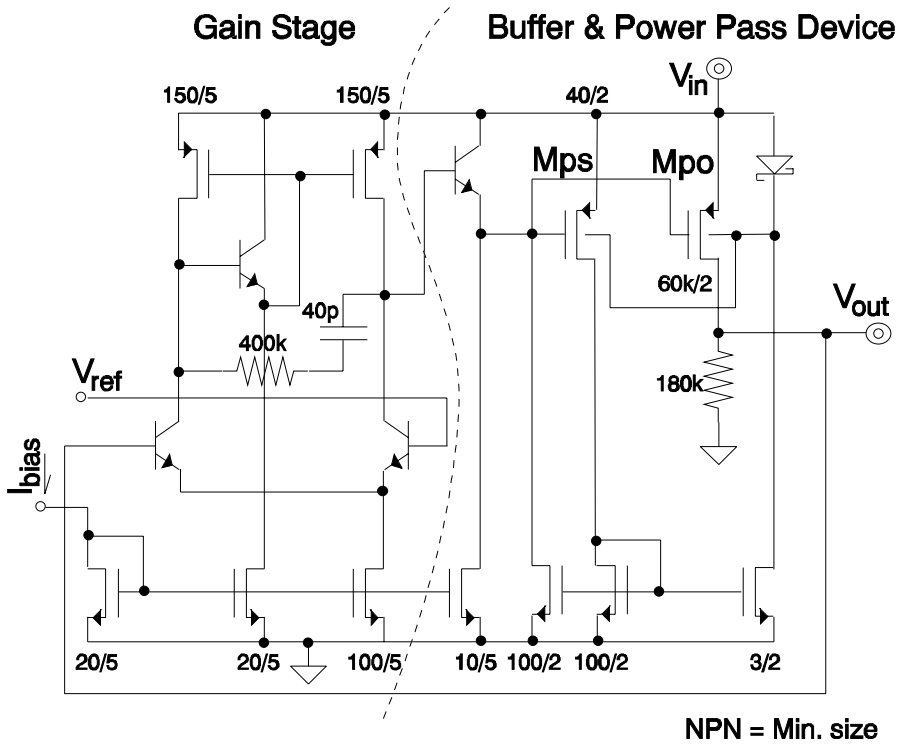

Figure 7.7. Schematic of the control loop circuit.

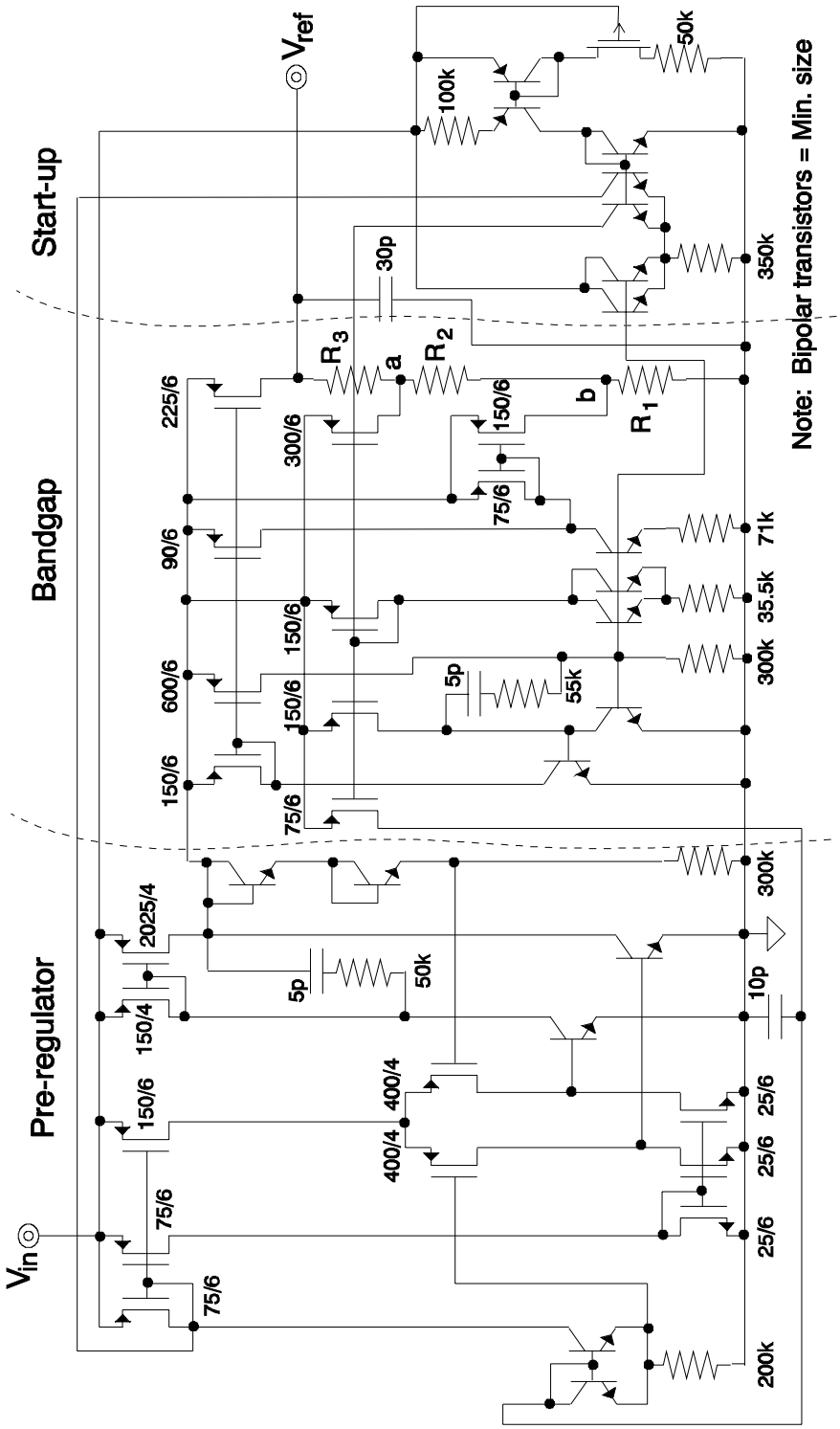

Figure 7.9 Schematic of the reference circuit

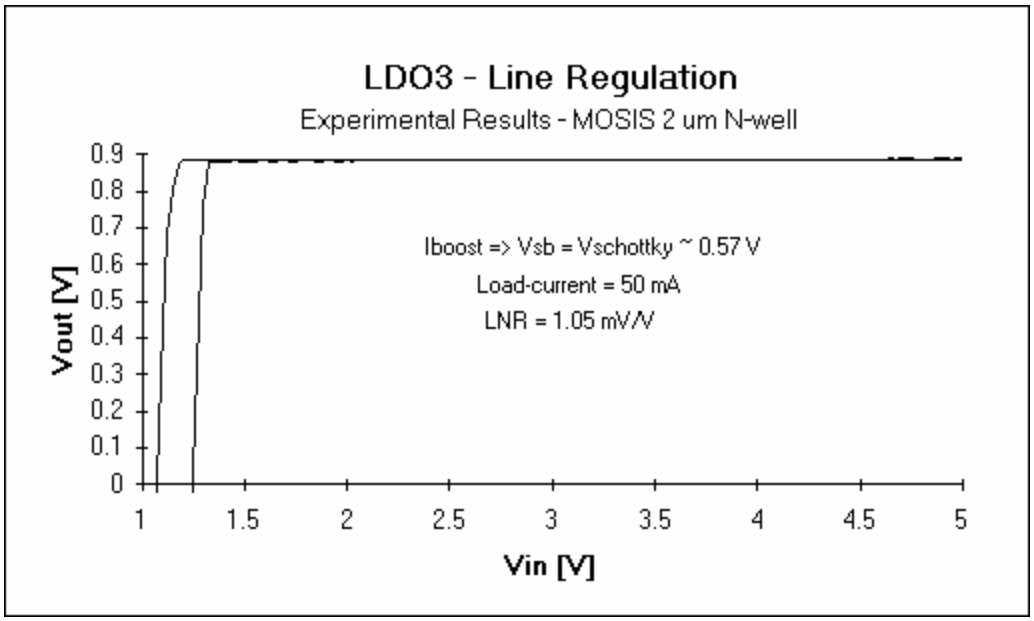

Figure 7.9. Line regulation performance of the control loop.

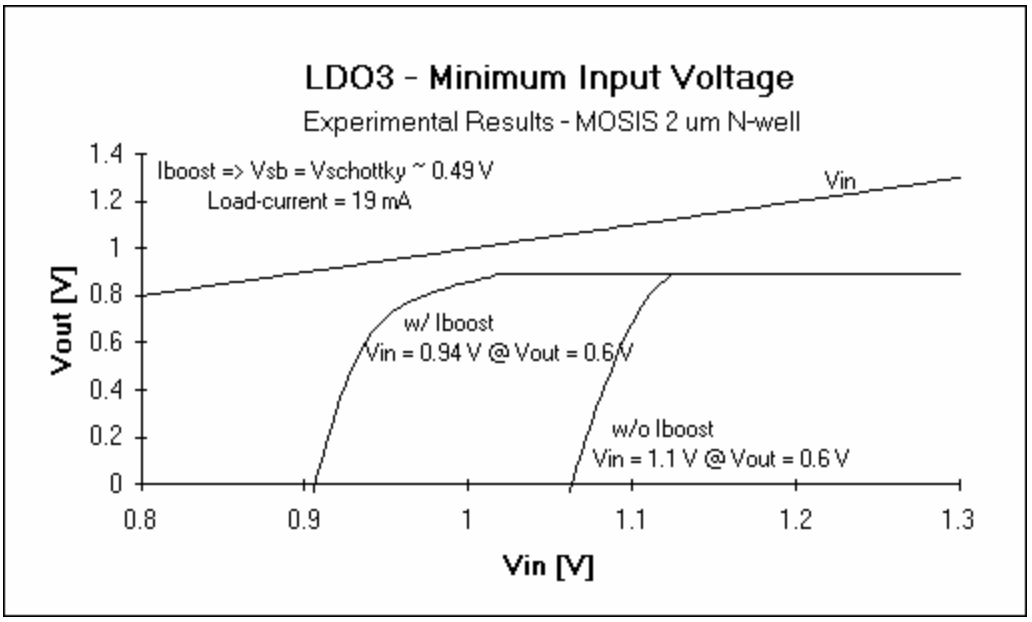

Figure 7.10. Minimum input voltage of the control loop.

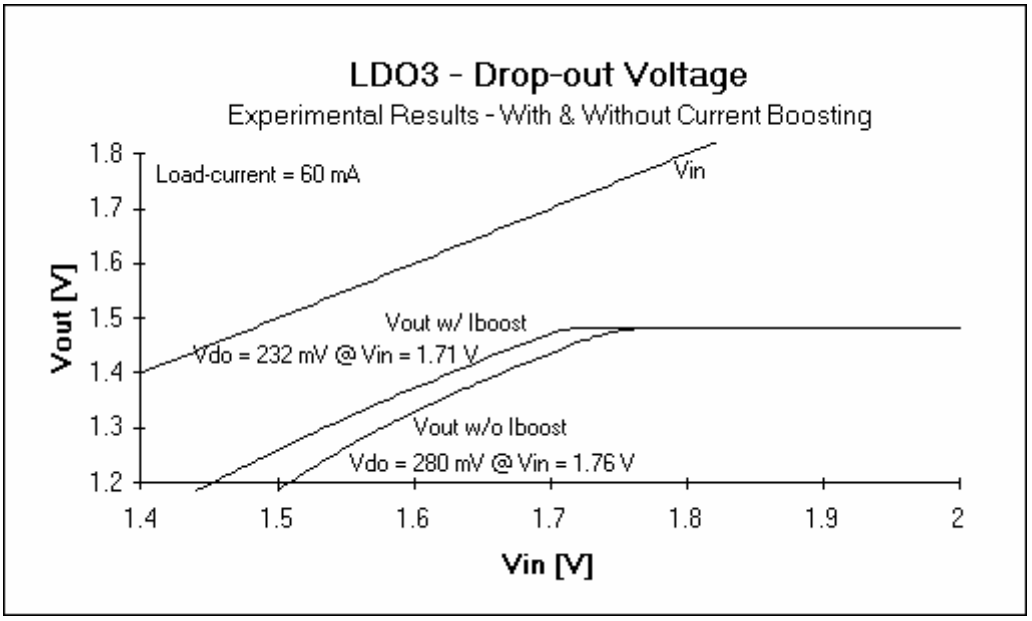

Figure 7.11. Drop-out voltage performance.

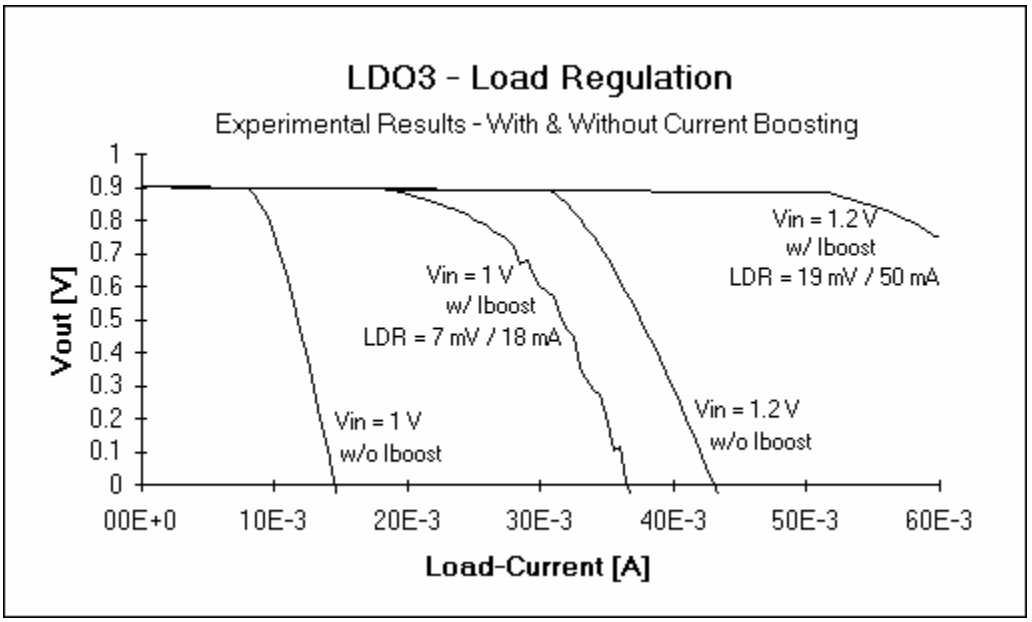

Figure 7.12. Load regulation performance.

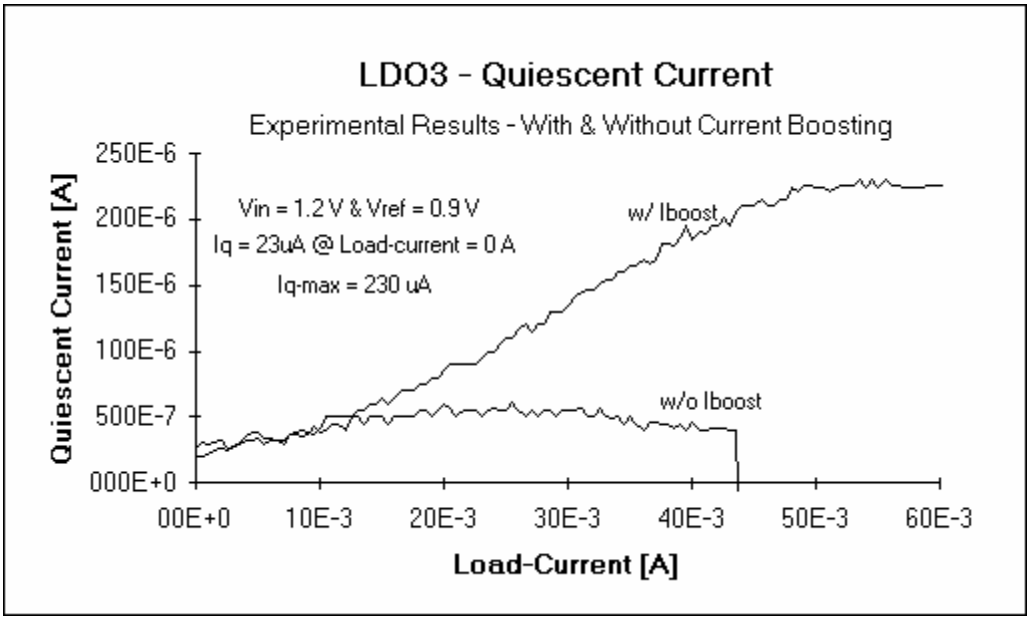

Figure 7.13. Quiescent current flow of the control loop.

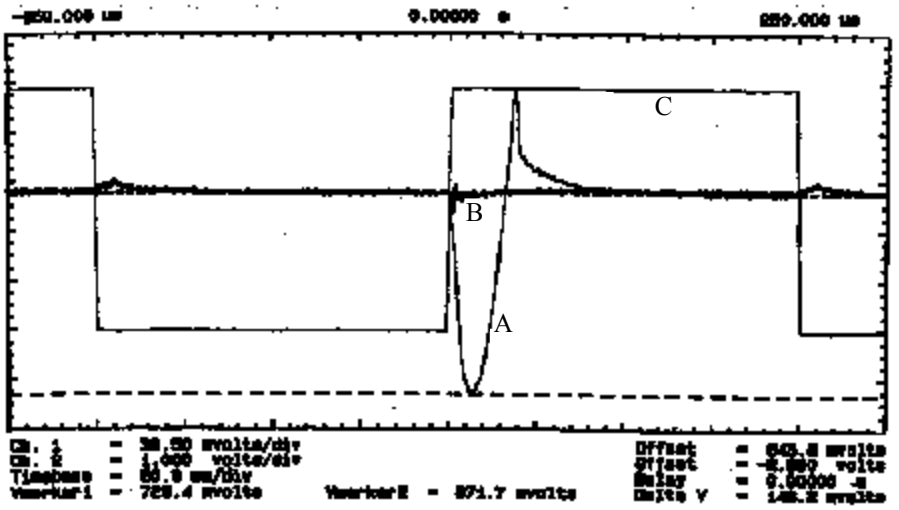

Figure 7.14. Transient response to a full range load-current step (A) with and (B) without the aid of load dependent biasing in the current efficient buffer.

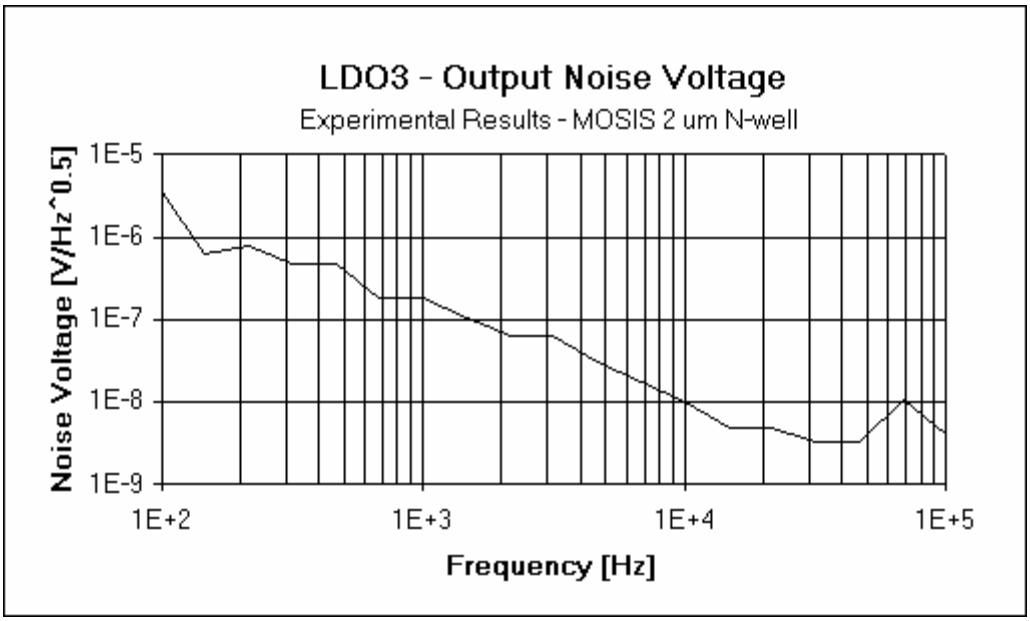

Figure 7.15. Control loop output noise voltage performance.

Table 7.1. Table of parameters affected by the current boosted pass device and the current efficient buffer.

Specification	**LDO**	**LDO w/o Current boost**	**LDO w/o Load dependent biasing**
$I_{quiescent}$ @ no-load	23 µA	23 µA	23 µA
$I_{quiescent\text{-}max}$	230 µA	50 µA	200 µA
$I_{o\text{-}max}$ @ V_{in}= 1.2V	50 mA	32 mA	50 mA
@ V_{in}= 1V	18 mA	8 mA	18 mA
$V_{drop\text{-}out}$ @ 60mA	232 mV	280 mV	232 mV
R_{on}	3.9 Ω	4.7 Ω	3.9 Ω
$\Delta V_{o\text{-}Transient}$	19 mV	19 mV	148 mV

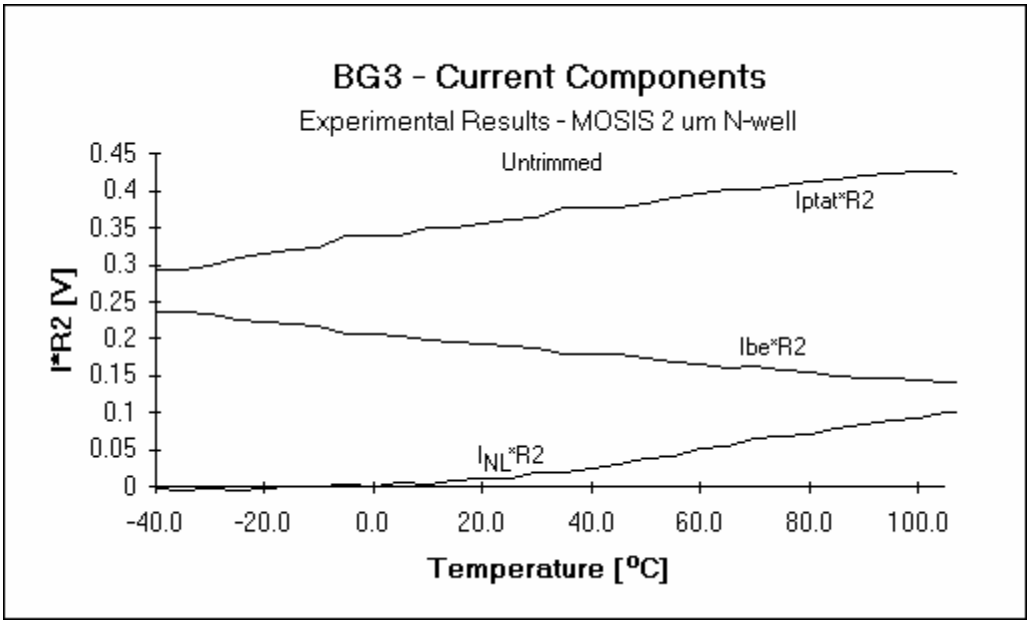

Figure 7.16. Temperature dependent currents in the reference.

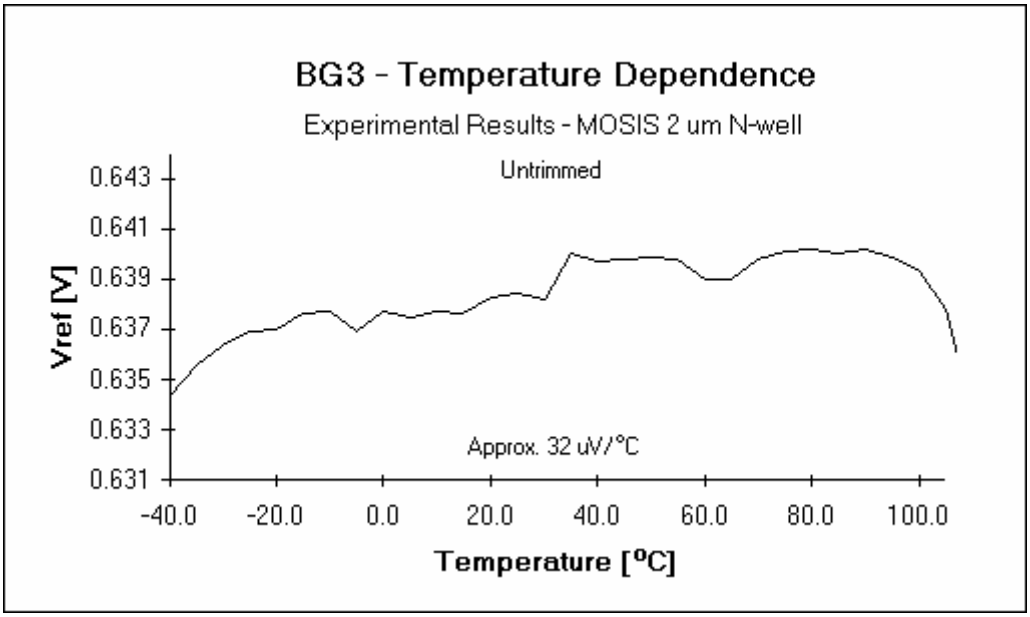

Figure 7.17. Temperature drift performance of the untrimmed reference.

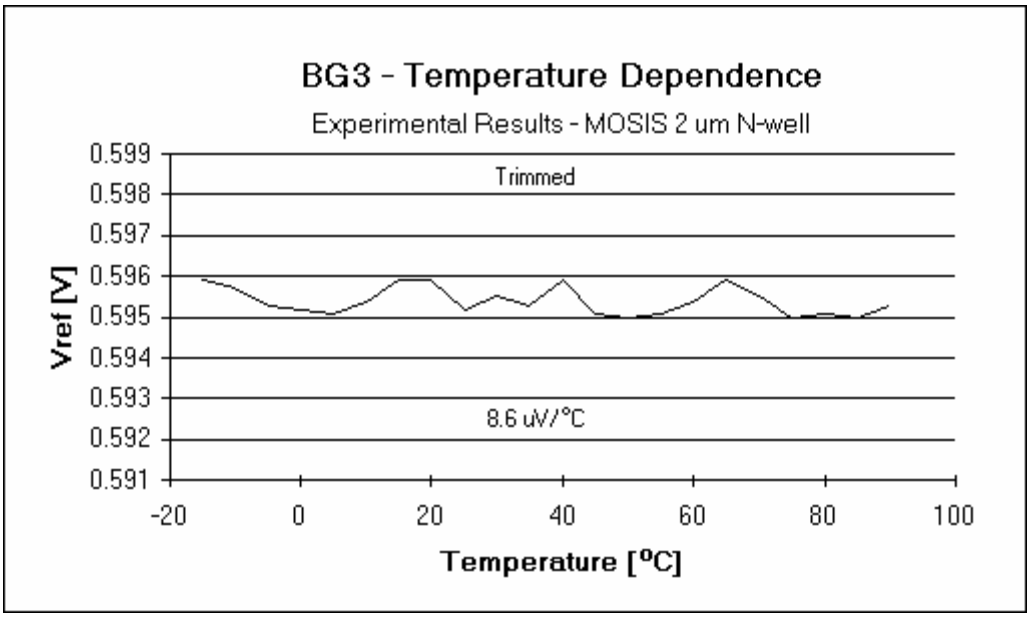

Figure 7.18. Temperature drift performance of the trimmed reference.

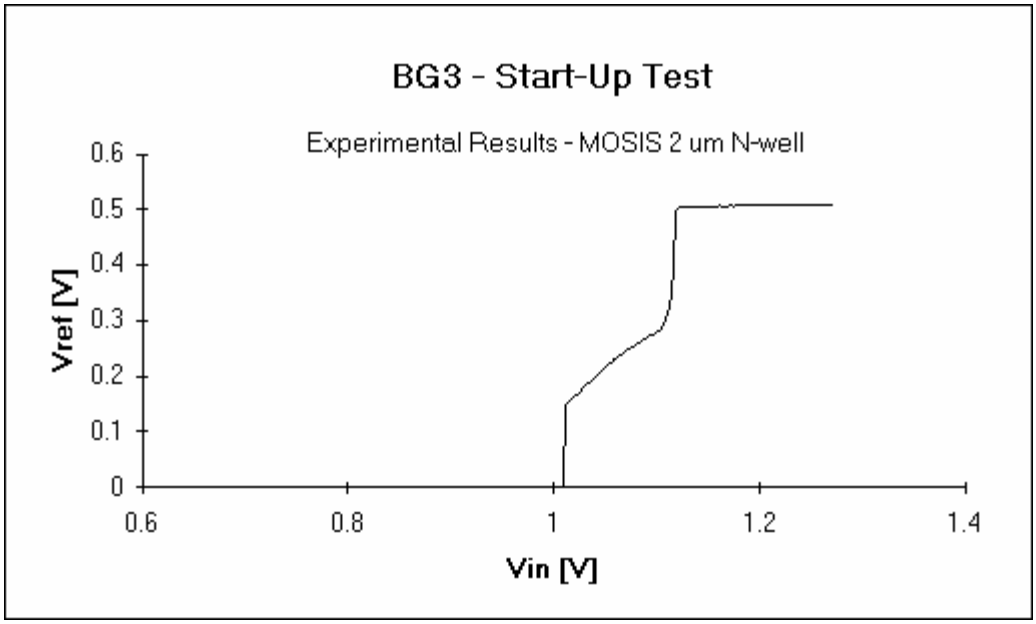

Figure 7.19. Reference start-up test.

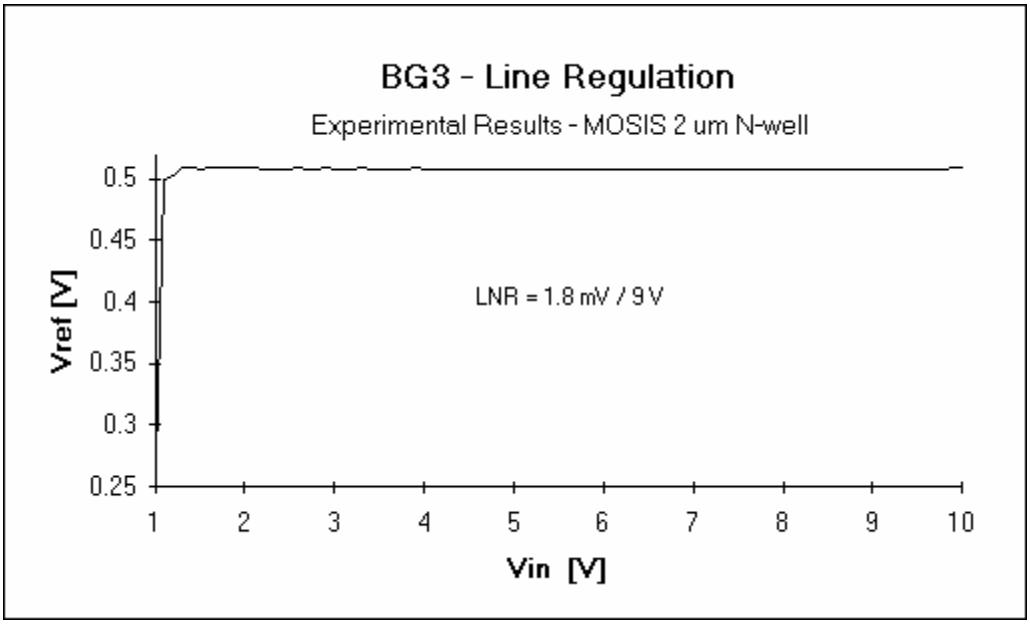

Figure 7.20. Line regulation performance of the reference.

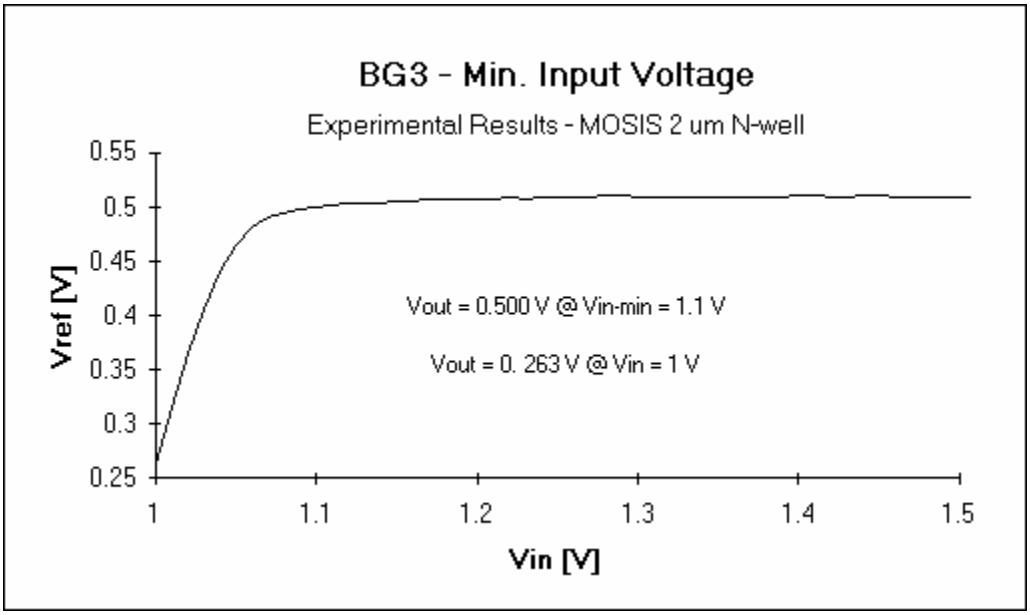

Figure 7.21. Minimum input voltage of the reference.

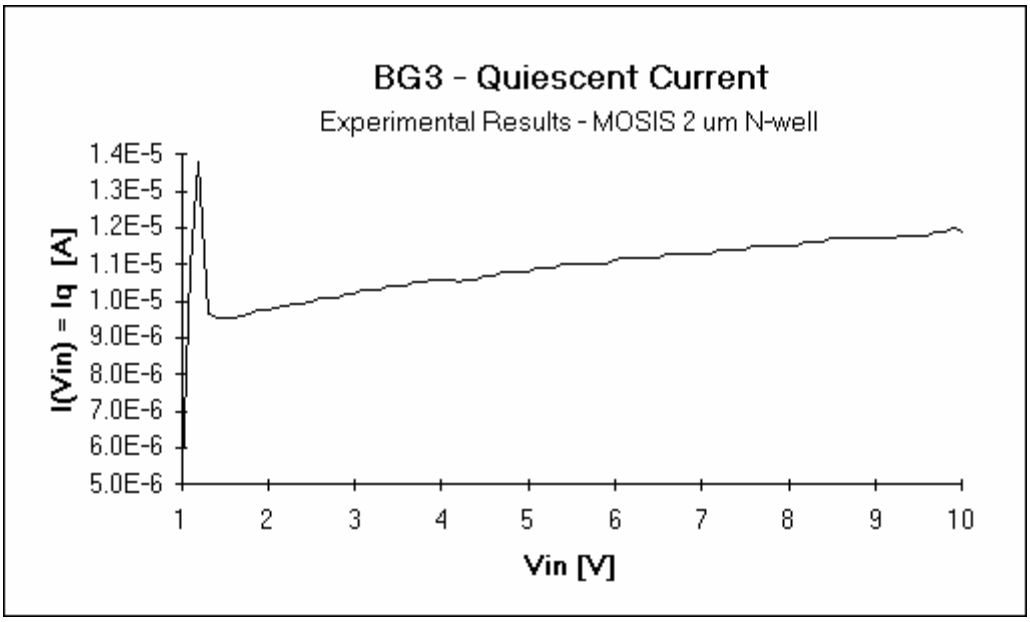

Figure 7.22. Quiescent current flow of the reference.

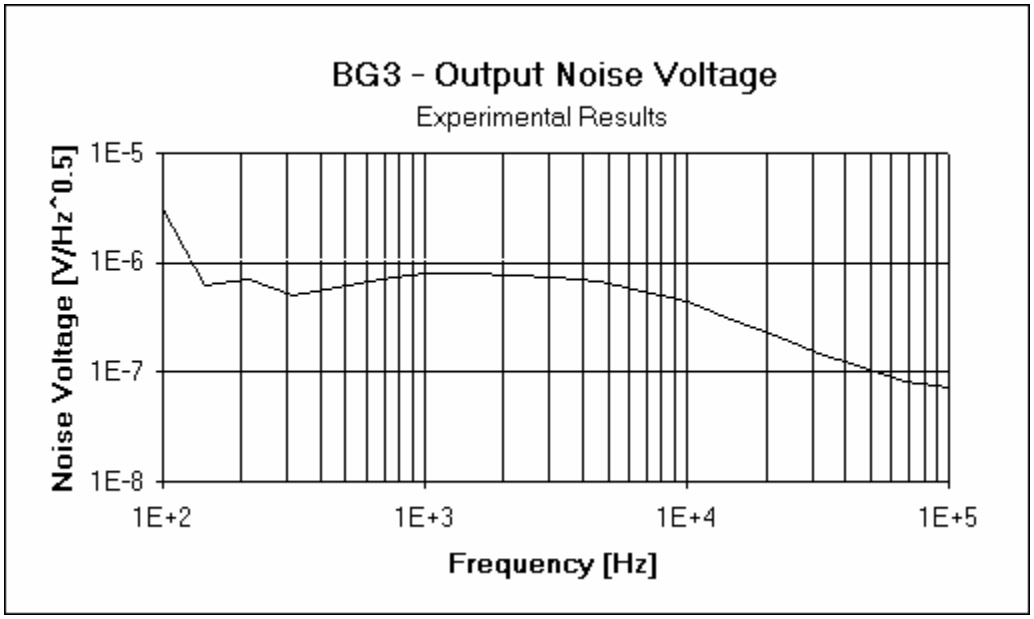

Figure 7.23. Reference output noise voltage performance.

7.5 Summary

This chapter has demonstrated the system design issues in assembling a low drop-out regulator circuit. It started by exploring the different circuit blocks and continued to discuss the physical layout characteristics and requirements of the system. Particular attention was given to those layout issues that affect performance and reliability. A description of the protection circuits followed. The discussion included overload current protection, reverse battery protection, and thermal shutdown protection. Lastly, the chapter concluded with the results of a prototype circuit fabricated in MOSIS 2 μm CMOS technology with an added p-base layer. The results verified the appropriateness of the enhancing techniques and the low voltage circuits developed in the previous chapters. Table 7.2 shows the resulting performance parameters of the system relative to the target specifications defined in chapter 1. Overall accuracy was met while minimum input voltage, quiescent current flow at zero-load current, and drop-out voltage performance requirements exceeded the original projections.

Table 7.2. Performance summary.

Specification	Control Loop	Reference	System	Target
V_{in}	≥ 1 V	≥ 1.1 V	≥ 1.1 V	≥ 1.2 V
$I_{quiescent}$ (no load)	23 μA	17 μA	40 μA	≤ 65 μA
$I_{quiescent}$ (I_o=50mA)	230 μA	17 μA	247 μA	-
$V_{drop\text{-}out}$ (I_o=60mA)	232 mV	n/a	232 mV	≤ 0.3 V
R_{on}	3.9 Ω	n/a	3.9 Ω	2 to 6 Ω
$I_{o\text{-}max}$ @ V_{in}=1V	18 mA	n/a	18 mA	-
$I_{o\text{-}max}$ @ V_{in}=1.2V	50 mA	n/a	50 mA	≥ 50 mA
C_{output}	4.7 μF	n/a	4.7 μF	4.7 μF
ESR range	0 to 10+ Ω	n/a	0 to 10+ Ω	0 to 10 Ω
Temperature	-10 to 90 °C	-10 to 90 °C	-10 to 90 °C	-10 to 90 °C
$\Delta V_{o\text{-}Transient}$	19 mV	n/a	19 mV	≤ 75 mV
Temperature Drift	16.7 μV/°C	8.6 μV/°C	25.3 μV/°C*	-
Line Regulation	1.05 mV/V	204 μV/V	1.25 mV/V	-
Load Regulation	0.38 mV/mA	n/a	0.38 mV/mA	-
V_{offset}	4 mV	n/a	4 mV	-
Accuracy	± 3 % (V_{out} = V_{ref} = 0.9 V)			± 3 to 5 %

* TC is improved by trimming the reference to compensate the control loop's TC.

CHAPTER VIII

CONCLUSIONS

On the basis of the literature survey and the results of the research, several conclusions and projections can be formulated. This chapter starts with a summary of the obstacles and the techniques developed to enable practical realizations of low drop-out regulators (LDO) appropriate for single, low voltage battery cell operation. This is followed by a discussion of the direction of technology and the consequential effects on low drop-out regulators within the context of prevailing designs and the research at hand. The chapter concludes with general comments about the research and recommendations for the continuation of this work.

8.1 Obstacles

The main objective of this research was to develop techniques that allow low drop-out regulators to work in a battery operated environment. This is driven by the market demand for portable and compact products, such as cellular phones, pagers, camera recorders, etc. As a result, low voltage and low battery current drain are intrinsic characteristics. A single, low voltage battery cell requires operation at voltages between 0.9 and 1.5 V. Furthermore, drain current must be necessarily low to prolong battery life. However, this is virtually impossible during conditions of high load-current when current drain is dominated by load-current while quiescent current flow is negligible. On the

other hand, current drain can be reduced during conditions of low load-current where quiescent current is a significant portion of the total current drain. By the way, many applications demand low load-currents for the majority of the time while high load-currents are only demanded briefly. As a result, low quiescent current at low load-currents (high current efficiency) is an important parameter that determines the longevity of a battery.

The problems associated with low input voltages manifest themselves in voltage headroom and output current capabilities. Low voltage affects the reference circuit, the error amplifier, and the pass device. Most references have output voltages of approximately 1.2 V (bandgap voltage). This forces the input voltage to be approximately 1.4 V, in other words, at least one saturation voltage above the reference voltage. Furthermore, references operating at these voltages tend to have poor line regulation performance because of the finite output impedance of uncascoded transistors. Moreover, developing a curvature corrected bandgap without incurring significant quiescent current flow at low voltage is a difficult task. The error amplifier suffers from limitations in flexible circuit architectures. The requirements of the amplifier include high gain, bandwidth, and output voltage swing. The gain affects load regulation while bandwidth influences the transient response of the system. These are laborious objectives to achieve with characteristically low quiescent current flow when considering that circuit techniques such as cascoding, voltage followers, and Darlington configurations are discouraged. Lastly, the performance of the pass device is greatly diminished when the input voltage is decreased. This results from reductions in gate drive, which decreases output current capabilities as well as increases drop-out voltages. These circuit limitations were addressed by the research and were categorized in four distinct areas, namely, current efficiency, current boosting, load regulation enhancement,

and referencing. In the implementation of the circuits developed, novel circuit techniques were designed that exploited the characteristics of the given process technology. This is not only beneficial to designs in existing technologies but also to future and more advanced processes by being fully exploited.

8.2 Enabling Techniques

Current Efficiency

The main issue with quiescent current flow revolves around the control loop of the regulator. In particular, the limitation has been identified to be the buffer of the error amplifier. This is because during transient load-current step transitions the buffer needs to drive quickly the parasitic gate capacitance of the pass device. This capacitance, unfortunately, is characteristically high because the size of the pass element is created large to generate low drop-out voltages and high output currents. Consequently, the slew-rate current of the buffer and therefore the quiescent current flow of the overall amplifier is limited by the transient specification of the system. Thus, a slew-rate dependent boost is developed. The idea is to aid the circuit only during transient conditions. The boost circuit essentially uses a unity gain buffer with low threshold bypass switches. The buffer is still required but its demands are driven by the frequency response and not the slew-rate requirements of the system. Further scrutiny showed that the ac demands of the system were dependent on load-current. As a result, a minimized quiescent current design was developed that not only met the requirements of stability but also aided the slew-rate current demands during transient load-current transitions. The resulting architecture was the current efficient buffer.

Current Boosting

The problem of output current capabilities resides in the power PMOS pass device. At low input voltages, the gate drive of the transistor is diminished and consequently so is its output current and "on" resistance. This problem is circumvented by increasing the input voltage and/or increasing the size of the transistor. The former is counterproductive for low voltage operation. The latter causes the parasitic gate capacitance to increase, which increases the slew-rate current requirements of the buffer in the amplifier. This, in turn, places a harsher limitation on quiescent current flow. The only way to improve performance without sacrificing area or low voltage performance is by decreasing the threshold voltage of the transistor thereby effectively increasing gate drive. This is achieved by the composite PMOS pass device. The main concept of the circuit is to reduce the threshold voltage of the transistor by forward biasing the source to bulk junction during conditions of high load-current, which is based on the bulk effect phenomenon.

Load Regulation Enhancement

Load regulation performance is limited by the dc open-loop gain of the control loop. This open-loop gain, in turn, is limited by the required bandwidth of the system and the frequency response implications of the loading circuits. The bandwidth is then limited by the transient response requirements and the parasitic poles of the system. The parasitic poles tend to be at lower frequencies because the circuits are designed with minimum quiescent current flow. As a result, load regulation performance is also limited. This is ameliorated by adding a pole/zero pair to the ac response of the system. The main idea is to promote the rapid drop of gain per decade of frequency. As a result, the dc gain can be increased while simultaneously maintaining the unity gain frequency below the frequencies where the parasitic poles reside. Two error amplifier topologies were developed to achieve this, namely, parallel path amplifiers and frequency shaping

gain structures. The former utilizes one amplifier to introduce the pole (dominant pole of the main amplifier) and another amplifier to introduce a zero (parallel amplifier is used as a feed forward path). The frequency shaping gain structures use a single, one stage amplifier topology to generate a frequency response exhibiting a pole/zero pair behavior. Among the two, the latter is the most appropriate for low quiescent current flow.

Low Voltage Reference

Most bandgap reference circuits utilize a voltage mode approach. They create the reference voltage by adding a base-emitter and a proportional-to-absolute temperature (PTAT) voltage. The result of this is a minimum input voltage requirement of one saturation voltage plus a bandgap voltage. Furthermore, if good line regulation performance is required, the minimum input voltage requirement is degraded by another saturation voltage. The input voltage is ultimately limited to be greater than 1.5 - 1.6 V. Thus, a mixture of a voltage-mode and a current-mode topology is developed that allows the realization of a low voltage reference with flexible temperature compensation maneuverability. An appropriate trimming procedure is also successfully developed. The only problem left to overcome was to implement a curvature correcting technique that incurs small chip area and low quiescent current flow. A technique was developed that did not incur any additional quiescent current flow, namely, the resistor ratio method. The concept is to choose two different types of resistors whose ratio yields a PTAT temperature coefficient. As a result of running a PTAT current defined by one type of resistor through another type of resistor, a PTAT squared term is generated. This constitutes one of the classical methods of curvature correction. The drawback to this circuit is actually finding two resistors with the necessary characteristics in a particular process technology. Consequently, the current subtraction scheme was developed. This method is not dependent on technology and its realization only requires one additional

transistor path to ground thereby requiring minimum additional quiescent current flow. The main concept of the circuit lies in the subtraction of a base-emitter dependent current from a PTAT current and the finite output impedance of transistors.

Table 8.1 summarizes the original contributions of this research. The overall study led to several paper submissions. Two of these were indirectly related to the research but necessary and appropriate for the successful development of the same. They are titled (1) "A 1V CMOS op amp using bulk-driven MOSFETs" and (2) "Low-Voltage Analog Circuits Using Standard CMOS Technologies" and they were published in *IEEE International Solid-State Circuits Conference Digest* and *Proc. International Symposium on Low Power Design* respectively. Four other papers were submitted and whose

Table 8.1. Summary of original contributions.

Concept	Technique
Current Efficiency	Slew-rate dependent boost
	Current efficient buffer
Current Boosting	Composite output PMOS transistor
Load Regulation Enhancement	Parallel amplifier topology
	Frequency shaping amplifier
Low Voltage Reference	IV-mode output structure & associated trimming procedure
	Resistor ratio curv. corr. method
	Current subtraction curv. corr. method
Low voltage circuit practices (amplifier and reference topologies)	

content had a direct impact on LDOs. Their titles are (1) "Study and Design of Low Drop-out Regulators," (2) "Optimized Frequency Shaping Circuit Topologies for LDOs," (3) "A Low Voltage, Low Quiescent Current, Low Drop-out Regulator," and (4) "A Novel Low Voltage, Micro-Power Curvature Corrected Bandgap Reference." The first two papers were submitted to *IEEE Transactions on Circuits and Systems* and the other two were submitted to *IEEE Journal of Solid-State Circuits*.

8.3 Direction of Market Demand

Technology

Process technologies are driven by the digital and the mixed-signal markets, which demand higher packing densities [7]. As a result, lithography is reduced and associated breakdown voltages are decreased [8, 9]. In other words, the technology trend is forcing circuits to operate at lower power supply voltages. In fact, 0.14 μm process technologies are expected to be in effect by the year 2004 and the operating voltage range is expected to be as low as 0.9 V [9, 12]. The thrust of the market has been driven in the recent past by digital applications. Consequently, vanilla CMOS processes have become relatively inexpensive and associated threshold voltages are being reduced. The threshold voltage, however, is not expected to decrease below 0.5 or 0.6 V. This is a characteristic imposed by digital circuits. Pure bipolar processes will still be demanded for specific applications but they will not drive the market.

Fully integrated products, on the other hand, are currently launching a more vociferous campaign that is affecting the demands on technology. Mixed-signal products are the result of complete circuit integration. A peaceful coexistence of analog and digital circuits is possible in a purely CMOS environment but with degraded analog performance. The use of bipolar devices, though extinct in prevailing digital designs, is

still prevalent in many analog circuits for enhanced performance. As a result, the demand on technology is slowly being shifted towards biCMOS processes. The high demand will eventually reduce costs to the level of current CMOS technologies. The bipolar features that will most likely be demanded are a p-base layer, a buried layer, and a deep highly doped well plug for the creation of decent quality NPN transistors. Some of the current and relatively inexpensive versions have modified a vanilla CMOS process to include an additional p-base layer thereby offering NPN transistors with high saturation voltages.

LDO Implications

The consequence of lower breakdown voltages in future technologies will force regulator design to work with lower input voltages. This is aggravated by the growing demand for single, low voltage battery cell operation. Furthermore, quiescent current flow and drop-out voltage will be demanded to decrease as well. The demand for higher packing densities will also require low drop-out regulators (LDOs) to occupy less chip area. Low drop-out regulators can be and have been designed in purely CMOS and bipolar process technologies. However, performance can be significantly enhanced by designing in a biCMOS environment. The simple and relatively inexpensive addition of a p-base layer to a CMOS process offers the capability of vertical bipolar devices, which enhance the frequency response and the circuit topology characteristics of the LDO. This is corroborated by the low quiescent current flow demands of MOS pass devices, which are voltage driven in nature. In conclusion, the push towards biCMOS technologies with finer fabrication lithographies will be beneficial for the circuit design of LDOs. At the same time, however, more stringent requirements will be bestowed upon regulators, such as operation with lower input voltages, lower quiescent current flow, smaller chip area, and lower drop-out voltages.

8.4 Conclusion and Recommendations

Circuit techniques have been developed and verified that permit the practical realizations of low drop-out regulators in a single, low voltage battery cell environment to be feasible in current existing technologies. These are also pertinent techniques for higher voltage, high performance LDO designs. Furthermore, switching regulators and other applications can also use these contributions to enhance their performance. For instance, the current boosting technique can be readily utilized for boosting the output current drive of amplifiers or for enhancing the switch performance of dc-dc converters. The research has demonstrated the effectiveness of the concepts by designing and testing circuit prototypes through MOSIS 2 μm CMOS technology with an added p-base layer, a relatively inexpensive process.

The research has focused primarily on developing concepts that make low voltage and low quiescent current operation possible. However, the effects of the protection circuitry, though discussed, were not tested or measured. Thus, the next logical step is to study, develop, implement, and experimentally test the effects of overload current protection, thermal shutdown protection, and reverse battery protection on the overall performance of the LDO. The temperature dependence of the input offset voltage of the error amplifier should be included in the trimming procedure to yield improved overall accuracy. Moreover, reliability issues should be investigated such as performance over hours of operation (burn-in tests). Work can also be done to characterize the effects of current boosted transistors on switching regulators and amplifier output stages. Switching regulators can use complementary current boosted devices if realized in a biCMOS environment. The bulk of the PMOS transistor is extracted by an n-well while that of the NMOS device can be extracted through a p-base or an isolated p-epi region.

The p-base layer used for NPN transistors can be used as a p-well. The p-epi region can be isolated by using the buried layer as vertical isolation and a deep n+ collector plug ring as horizontal isolation. Amplifier output stages can also use the complementary structure with expected higher harmonic distortion levels and parasitic ac effects.

APPENDIX A

V_{BE} TEMPERATURE DEPENDENCE

The collector current of a bipolar transistor exhibits an exponential relationship to the base-emitter voltage and is nominally expressed as

$$I_c = I_s \exp \frac{V_{be}}{V_t}, \tag{A.1}$$

where I_c is the collector current, I_s is the saturation current in the forward-active region, V_{be} is the base-emitter voltage, and V_t is the thermal voltage. The effects of early voltage are neglected for this derivation. Consequently, V_{be} is derived to be

$$V_{be} = V_t \ln \frac{I_c}{I_s}. \tag{A.2}$$

The saturation current I_s is defined by the electron charge q (1.6 x 10^{-19} coulomb), the intrinsic carrier concentration n_i (approximately 1.5 x 10^{10} cm^{-3} at 300° K for silicon), the diffusion constant for electrons D_n, the emitter cross-sectional area A_e, the effective width of the base W_B, and the base doping density N_A (assumed to be constant) [3],

$$I_s = \frac{q\, n_i^2\, D_n A}{W_B N_A} = \frac{q\, n_i^2\, \overline{D_n} A_e}{Q_B}, \tag{A.3}$$

where Q_B is the number of doping atoms in the base per unit area of emitter and $\overline{D_n}$ is the average effective value of the electron diffusion constant in the base. In turn, the temperature dependence of the intrinsic carrier concentration and the average electron diffusion constant can be described by [51]

$$n_i^2 = AT^3 \exp\frac{-V_{go}}{V_t}, \tag{A.4}$$

and

$$\overline{D_n} = V_t \overline{\mu_n}, \tag{A.5}$$

where A is a temperature independent constant, T is temperature, V_{go} is the extrapolated bandgap voltage at 0° K, and $\overline{\mu_n}$ is the average mobility for minority carriers in the base,

$$\overline{\mu_n} = BT^{-n}, \tag{A.6}$$

where B and n are temperature independent constants. The relationship for the saturation current I_s is more explicitly expressed by substituting equations (A.4) - (A.6) in (A.3) and resulting in

$$I_s = \frac{q\left\langle AT^3 \exp\frac{-V_{go}}{V_t}\right\rangle \cdot \left\langle V_t BT^{-n}\right\rangle A_e}{Q_B} \tag{A.7}$$

or

$$I_s = CT^{(4-n)} \exp\frac{-V_{go}}{V_t} = CT^{(4-n)} \exp\frac{-V_{go}}{V_t}, \tag{A.8}$$

where C is a temperature independent constant defined by all the constants in equation (A.7), such as q, A, B, A_e, Q_B, and k/q from the thermal voltage term (V_t = kT/q where k is Boltzmann's constant, 8.62 x 10^{-5} eV/°K). Lastly, the collector current can be assumed to have a temperature dependence whose behavior can be described by

$$I_c = DT^x, \tag{A.9}$$

where D is a constant and x is an arbitrary number defined by the temperature dependence of the current forced through the collector, i.e., x is one for a proportional-to-absolute temperature (PTAT) current, $I_c \propto T^1$. Consequently, the temperature dependence of the base-emitter voltage can be re expressed by substituting equations (A.8) - (A.9) in (A.2) and resulting in

$$V_{be} = V_t \ln\left\langle \frac{D}{C} T^{[x-(4-n)]} \exp\frac{V_{go}}{V_t} \right\rangle = V_{go} + V_t \ln\frac{D}{C} - [(4-n)-x] V_t \ln T. \tag{A.10}$$

However, a more appropriate form of the base-emitter relationship, for the purpose of design, is its temperature dependence as a function of a reference temperature (T_r). This can be done by obtaining the relation of the base-emitter voltage (V_{be}) at a reference temperature (T_r), solving for a constant, and substituting it back in equation (A.10). The relation of V_{be} at T_r is

$$V_{be}(T_r) = V_{go} + V_{tr} \ln\frac{D}{C} - [(4-n)-x] V_{tr} \ln T_r, \tag{A.11}$$

where V_{tr} is the thermal voltage evaluated at the reference temperature (T_r). At this point, the constant can be derived to be

$$\ln\frac{D}{C}=\frac{V_{be}(T_r)-V_{go}+[(4-n)-x]V_{tr}\ln T_r}{V_{tr}}. \tag{A.12}$$

Now, equation (A.12) can be substituted back in (A.10) to yield the well-known temperature dependence relationship of the base-emitter voltage,

$$V_{be}=V_{go}+\frac{T}{T_r}\left[V_{be}(T_r)-V_{go}\right]-[(4-n)-x]V_t\ln\frac{T}{T_r}. \tag{A.13}$$

It is sometimes useful to develop the Taylor series expansion for the logarithmic term and substitute it back in equation (A.13). The purpose for this is to more accurately design the curvature correcting component of the bandgap reference. The process dependent constant (4 - n) is sometimes expressed as η with an approximate value between 3.6 and 4 [40].

APPENDIX B

IV-MODE BANDGAP TRIMMING PROCEDURE

The output structure of an IV-mode curvature corrected bandgap reference is illustrated in Figure B.1. Magnitude trimming is done at room temperature while temperature compensation is achieved by trimming throughout the specified temperature range. The following procedure illustrates how trimming, in general, can be done for this circuit architecture.

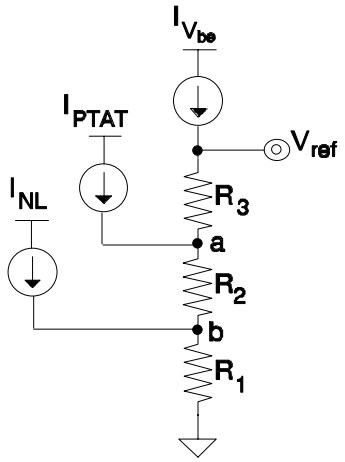

Figure B.1. IV-mode bandgap output structure.

Step 1: The reference voltage (V_{ref}) for this topology can be expressed as

$$V_{ref} = I_{V_{be}}[R_1 + R_2 + R_3] + I_{PTAT}[R_1 + R_2] + I_{NL} R_1, \qquad \text{(B.1)}$$

where I_{Vbe}, I_{PTAT}, and I_{NL} are the base-emitter voltage, proportional-to-absolute temperature (PTAT), and nonlinear temperature dependent currents respectively. Alternatively, this can be re expressed as

$$V_{ref}\frac{R_{2_{initial}}}{R_1+R_2}=\left\langle I_{V_{be}}\left[R_1+R_2+R_3\right]+I_{PTAT}\left[R_1+R_2\right]+I_{NL}R_1\right\rangle\frac{R_{2_{initial}}}{R_1+R_2} \quad \text{(B.2)}$$

or

$$V_{ref}\frac{R_{2_{initial}}}{R_1+R_2}=AI_{V_{be}}R_{2_{initial}}+BI_{PTAT}R_{2_{initial}}+CI_{NL}R_{2_{initial}}, \quad \text{(B.3)}$$

where A, B, and C are the coefficients of the temperature dependent current components,

$$A=\frac{R_1+R_2+R_3}{R_1+R_2}, \quad \text{(B.4)}$$

$$B=\frac{R_1+R_2}{R_1+R_2}=1, \quad \text{(B.5)}$$

and

$$C=\frac{R_1}{R_1+R_2}. \quad \text{(B.6)}$$

The temperature coefficient of the resistors is canceled because they are ratioed and made out of the same material, i.e.,

$$\frac{R_1(T)}{R_2(T)}=\frac{R_1(T_r)\cdot\left[1+A(T-T_r)+B(T-T_r)^2\right]}{R_2(T_r)\cdot\left[1+A(T-T_r)+B(T-T_r)^2\right]}=\frac{R_1(T_r)}{R_2(T_r)}, \quad \text{(B.7)}$$

where T is temperature, A and B are the linear and the quadratic temperature coefficients of the resistor, and T_r is the reference temperature (typically room temperature).

Step 2: Data points are collected for the reference voltage (V_{ref}), node "a" (V_a), and node "b" (V_b) throughout the temperature range desired.

Step 3: Since the initial resistor ratios are known and the voltage across each resistor has been collected throughout the temperature sweep, the currents multiplied by the initial resistance of R_2 can be derived for the entire temperature range,

$$I_{V_{be}} R_{2_{initial}} = \frac{V_{ref} - V_a}{\left\langle \frac{R_3}{R_2} \right\rangle_{initial}}, \tag{B.8}$$

$$I_{PTAT} R_{2_{initial}} = [V_a - V_b] - I_{V_{be}} R_{2_{initial}}, \tag{B.9}$$

and

$$I_{NL} R_{2_{initial}} = \frac{V_b}{\left\langle \frac{R_1}{R_2} \right\rangle_{initial}} - [V_a - V_b]. \tag{B.10}$$

Step 4: Equation (B.3) is temperature adjusted via a spreadsheet by using the values derived in equations (B.8) - (B.10) and adjusting the coefficients A and C (B is pre defined to be one) to yield the lowest temperature variation performance over the desired temperature range. This is a trial and error process whose results come in the form of extracted values for coefficients A and C.

Step 5: At this point, new resistor ratios for R_1/R_2 and R_3/R_2 can be derived by manipulating equations (B.4) and (B.6),

$$\frac{R_1}{R_2} = \frac{C}{1-C} \tag{B.11}$$

and

$$A = \frac{R_1 + R_2 + R_3}{R_1 + R_2} = \frac{\frac{R_1}{R_2} + 1 + \frac{R_3}{R_2}}{\frac{R_1}{R_2} + 1} \tag{B.12}$$

or

$$\frac{R_3}{R_2} = \langle A - 1 \rangle \left\langle \frac{R_1}{R_2} + 1 \right\rangle. \tag{B.13}$$

Step 6: The values of the currents multiplied by the initial resistance of R_2 at room temperature are identified from step 3, i.e., $(I_{V_{be}} R_{2_{initial}})_{T_r}$, $(I_{PTAT} R_{2_{initial}})_{T_r}$, and $(I_{NL} R_{2_{initial}})_{T_r}$ whose values are evaluated at T_r.

Step 7: Equation (B.1) can be re expressed as

$$V_{ref} \frac{R_{2_{initial}}}{R_2} = \left\langle I_{V_{be}} [R_1 + R_2 + R_3] + I_{PTAT} [R_1 + R_2] + I_{NL} R_1 \right\rangle \frac{R_{2_{initial}}}{R_2} \tag{B.14}$$

and consequently yield the following at room temperature,

$$V_{ref}(T_r) \cdot \frac{R_{2_{initial}}}{R_2} = (I_{V_{be}} R_{2_{initial}})_{T_r} \left\langle \frac{R_1}{R_2} + 1 + \frac{R_3}{R_2} \right\rangle +$$

$$(I_{PTAT}R_{2initial})_{T_r}\left\langle\frac{R_1}{R_2}+1\right\rangle+(I_{PTAT}R_{2initial})_{T_r}\left\langle\frac{R_1}{R_2}\right\rangle. \qquad (B.15)$$

As a result, the ratio of $R_{2initial}$ and R_2 can be derived for any desired value of $V_{ref}(T_r)$.

Step 8: If the temperature drift needs further adjustment, then the process can be repeated from step 2. An additional iteration may be warranted if the magnitude of the reference is changed significantly from its non trimmed to its trimmed state. This is because the output impedance of the mirrors generating the temperature dependent current components is finite. If the only parameter that needs adjustment is the magnitude of the reference voltage at room temperature, then the process is still repeated from step 2. However, a temperature sweep and step 4 are skipped and the values of A and C from the previous iteration are maintained. As a result, all the measurements are simply made at room temperature.

Notes: Knowledge of the absolute value of the resistors is not necessary. Instead, the intrinsic parameters that require control are the ratios of the resistors. Furthermore, if only magnitude trimming at room temperature is desired, then the procedure is the same except that measurements are only obtained at room temperature and step 4 is skipped altogether. Moreover, the values of A and C for the procedure are obtained from circuit simulations.

APPENDIX C

LAYOUT PLOTS

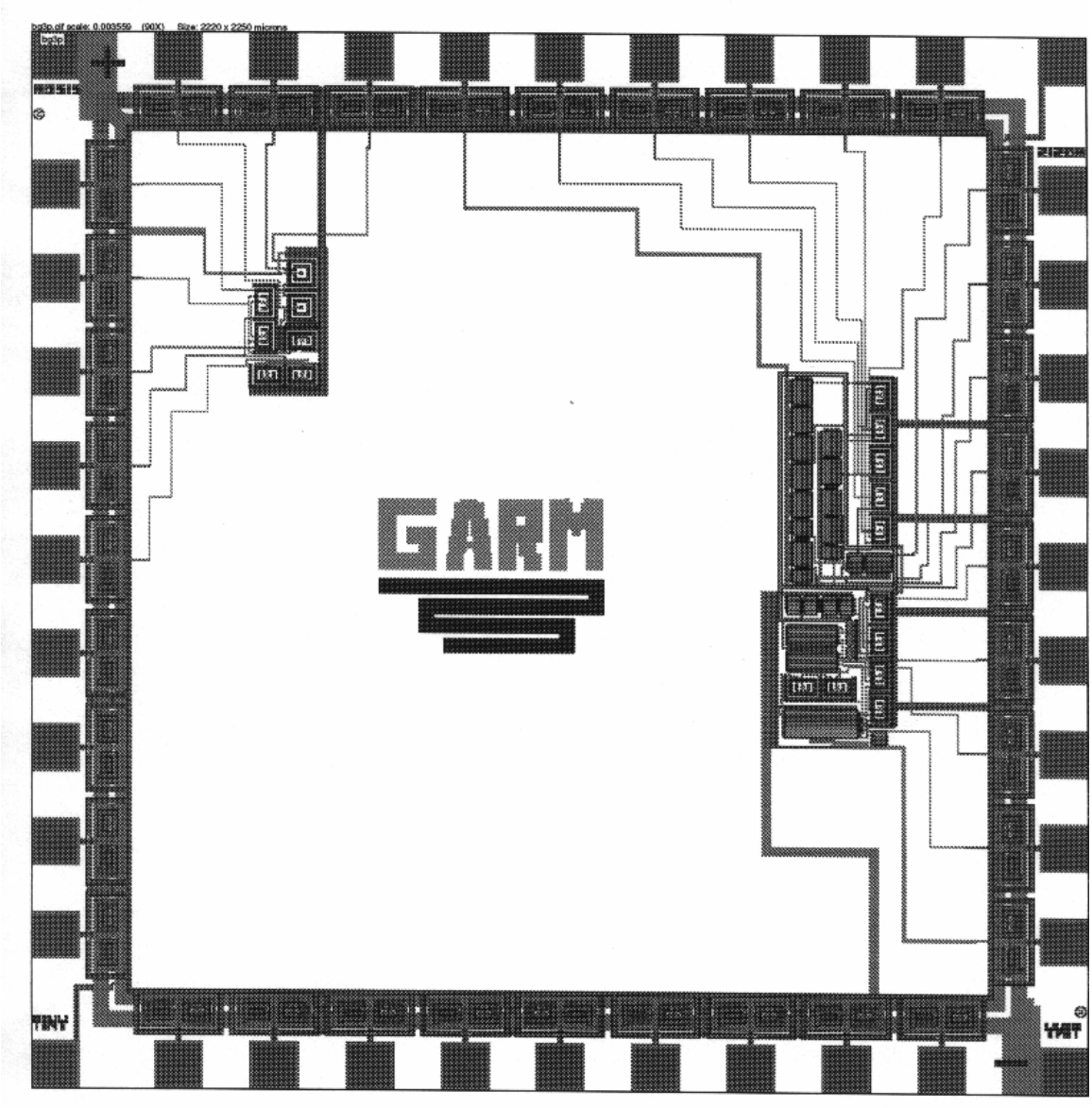

Figure C.1. Layout of the curvature corrected bandgap and associated start-up circuit.

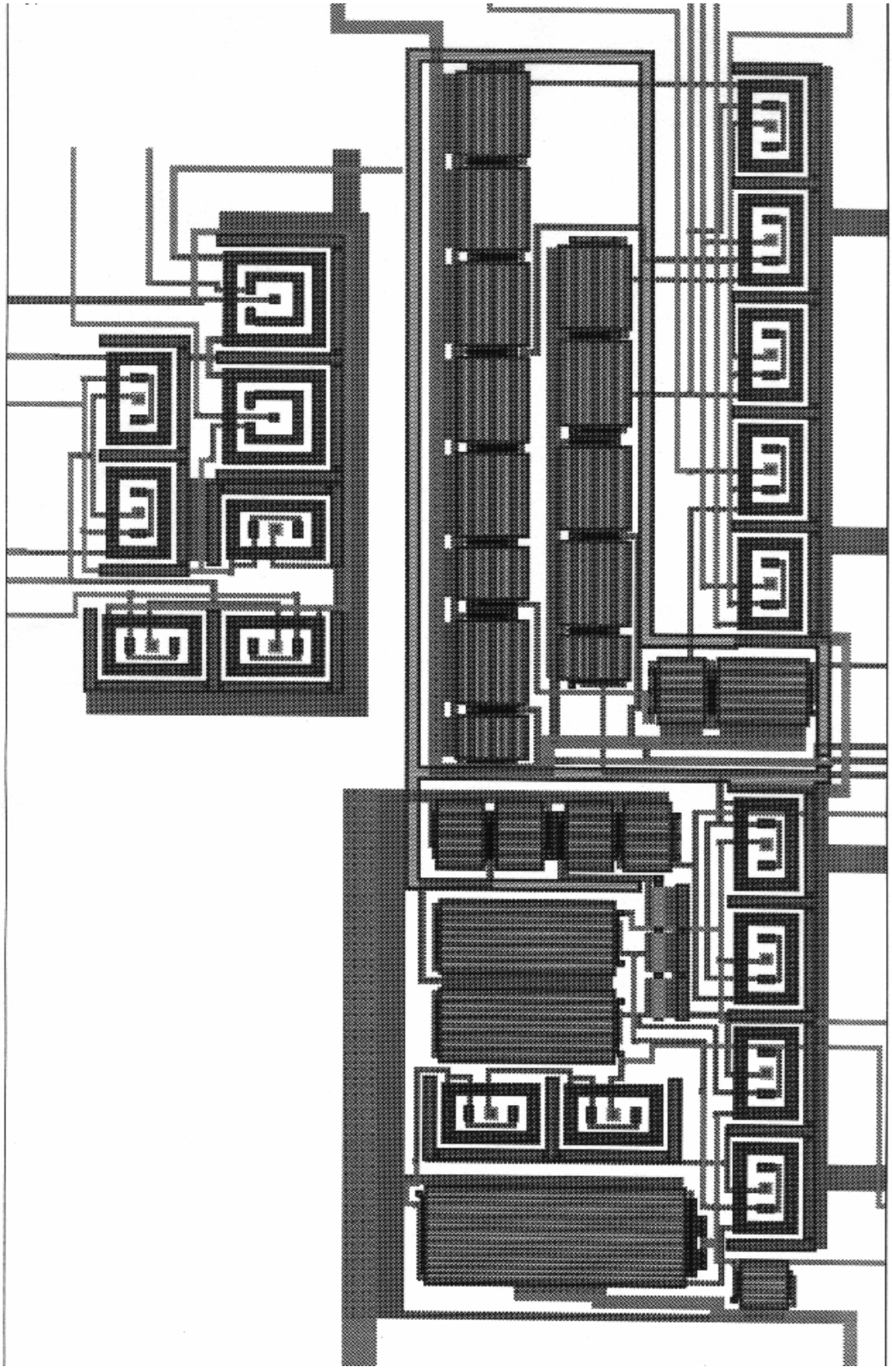

Figure C.2. Zoom-in plot of the start-up and reference (290 x 173 μm & 798 x 280 μm).

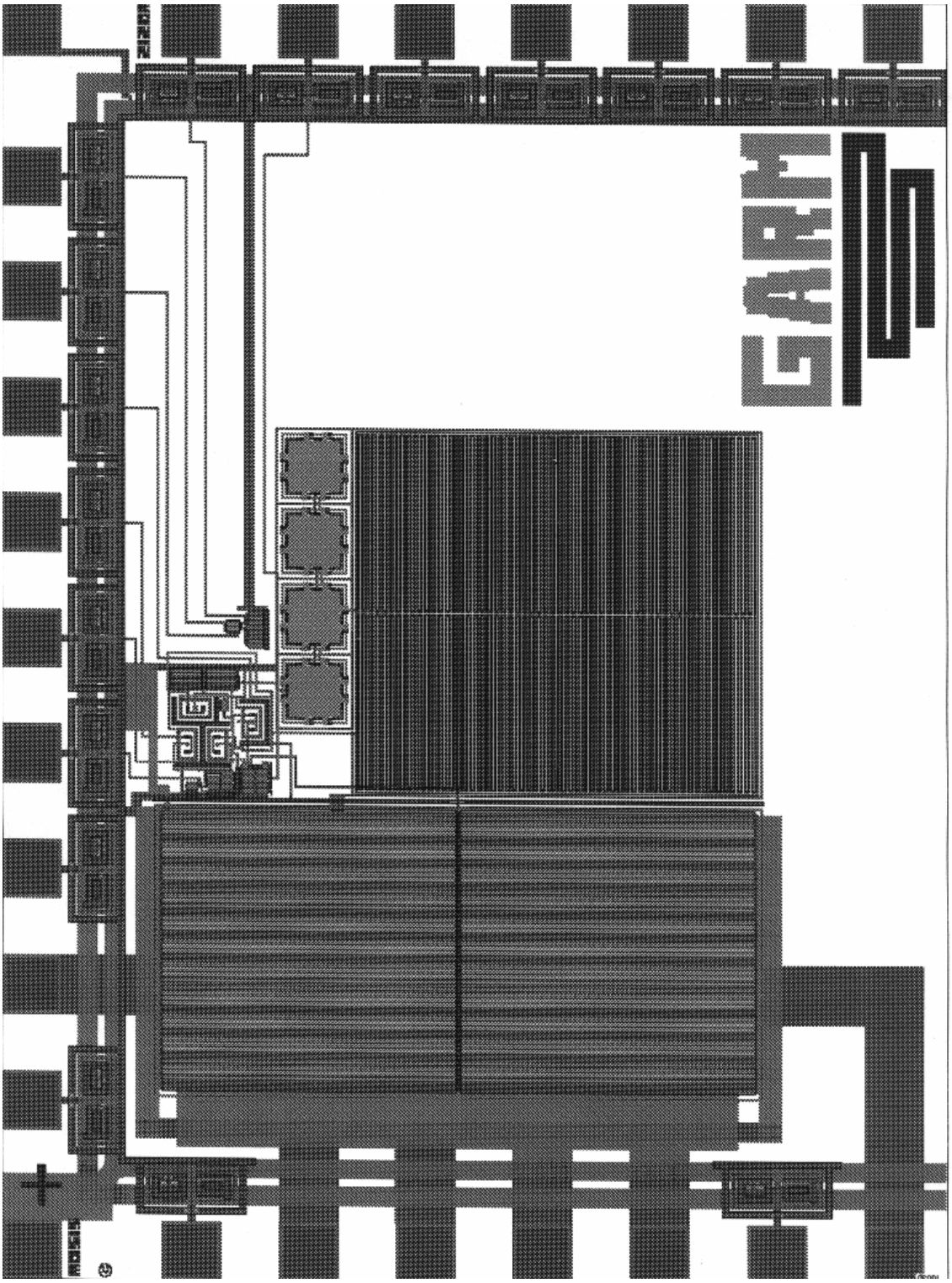

Figure C.3. Layout of the control loop (1103 x 1250 μm).

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VITA

Gabriel Alfonso Rincon-Mora was born in Caracas, Venezuela, on January 30, 1972, to Gilberto and Gladys M. Rincon. Gabriel was raised in Maracay, Venezuela after his family moved there in 1974. His family moved to the United States in 1983 and resided in North Miami Beach, Florida. He attended North Miami Beach Senior High School where he graduated in 1989 with High Honors and at the top of his class. Among other honors, Gabriel was awarded a Certificate for scholastic excellence in Mathematics, a Certificate for scholastic excellence in Science, and the Presidential Academic Fitness Award signed by President George Bush. This resulted in three scholarships to attend college, namely, Faculty Scholars' from Florida International University, Florida Undergraduate Scholars' from the state of Florida, and the Insignis Scholarship from the University of Detroit. He attended Florida International University from 1989 to 1992 where he received a Bachelor of Science in Electrical Engineering with High Honors, graduating at the top of his class. Amid the honors bestowed upon him, Gabriel was in the Florida International University Dean's List, was given Honorary Award Recognition in the National Dean's List, and was given Honorable Mention by the National Science Foundation. In 1993, Gabriel went to Georgia Institute of Technology to pursue a Master of Science in Electrical Engineering, which he received in June of 1994. He remained at Georgia Institute of Technology to pursue a Ph.D. in Electrical Engineering, which he received in December of 1996. The work at Georgia Institute of Technology resulted in the submission of seven papers to various journal publications. During his graduate program, he worked one summer for Northern Telecom and six months for Texas Instruments Incorporated, which led to the application of four patents, three of which

have been issued and one is still pending. Gabriel is a member of IEEE, Tau Beta Pi, Alpha Omega Chi, and Eta Kappa Nu, where he served as secretary of the local chapter in Florida International University. Upon graduation, Gabriel accepted a position with the standard linear design group at Texas Instruments Incorporated in Dallas, Texas.