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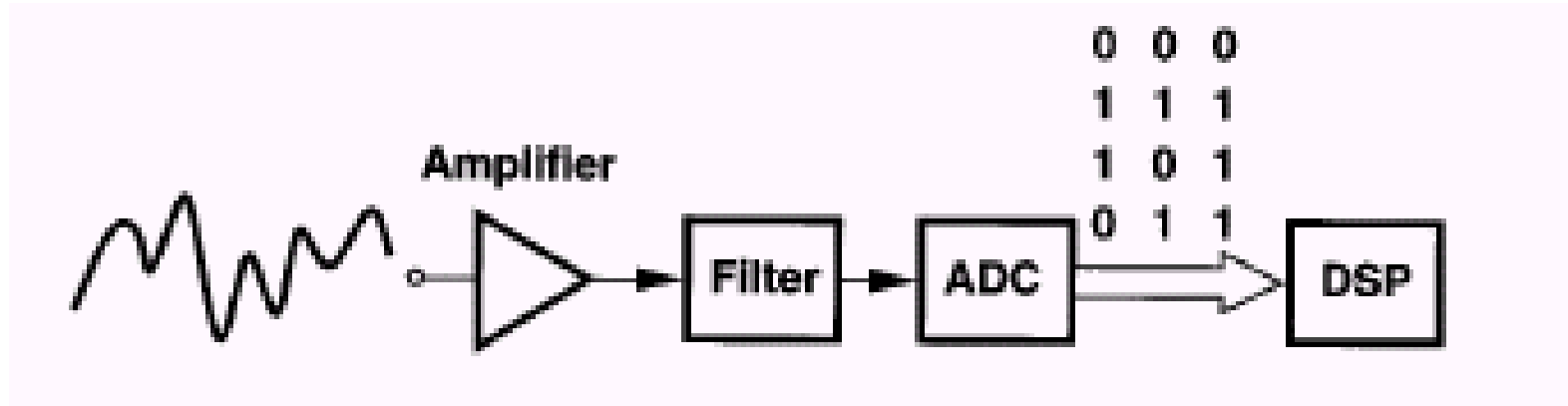
# SC схеми

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**Проектиране на аналогови интегрални схеми**

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# Аналоговият свят и цифровата обработка на сигнали



- Amplifier & Filter :

- аналогови схеми - analog (continuous-time) circuits или
- дискретни схеми - sampled data (discrete-time) circuits;

- ADC - дискретна схема;

- DSP – цифрова схема.

# Аналогови, дискретни и цифрови сигнали

## **Аналогови**

- Непрекъснати стойности във времето;
- Непрекъснати стойности на амплитудата.

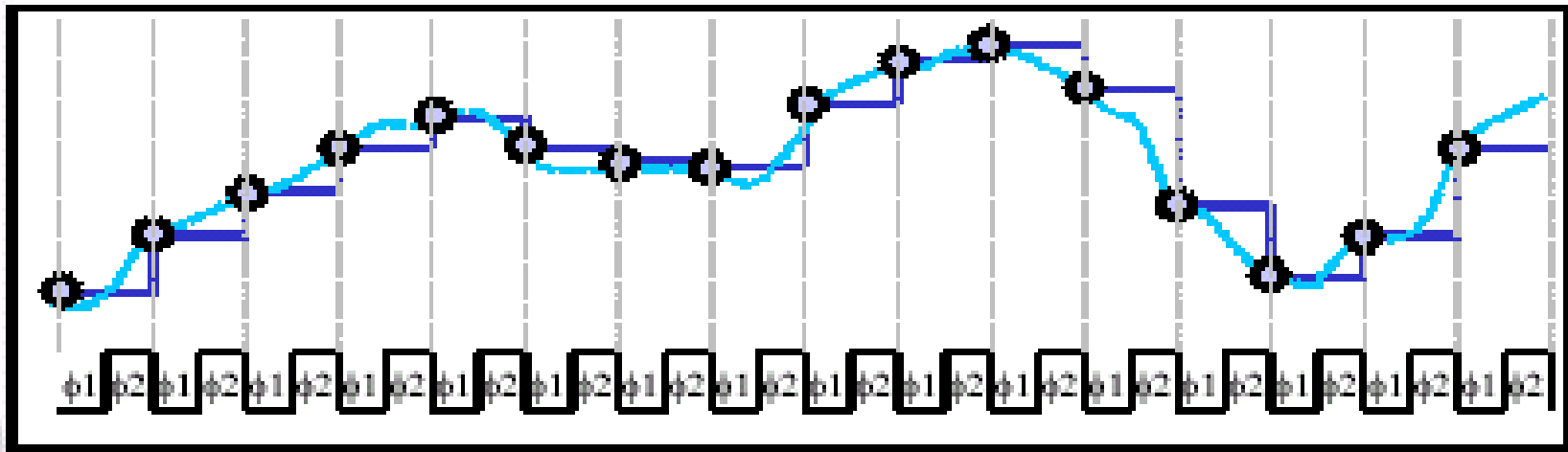
## **Дискретни**

- Дискретни стойности във времето;
- Непрекъснати стойности на амплитудата.

## **Цифрови**

- Дискретни стойности във времето;
- Дискретни стойности на амплитудата.

# Непрекъснати и дискретни сигнали



- Continuous time

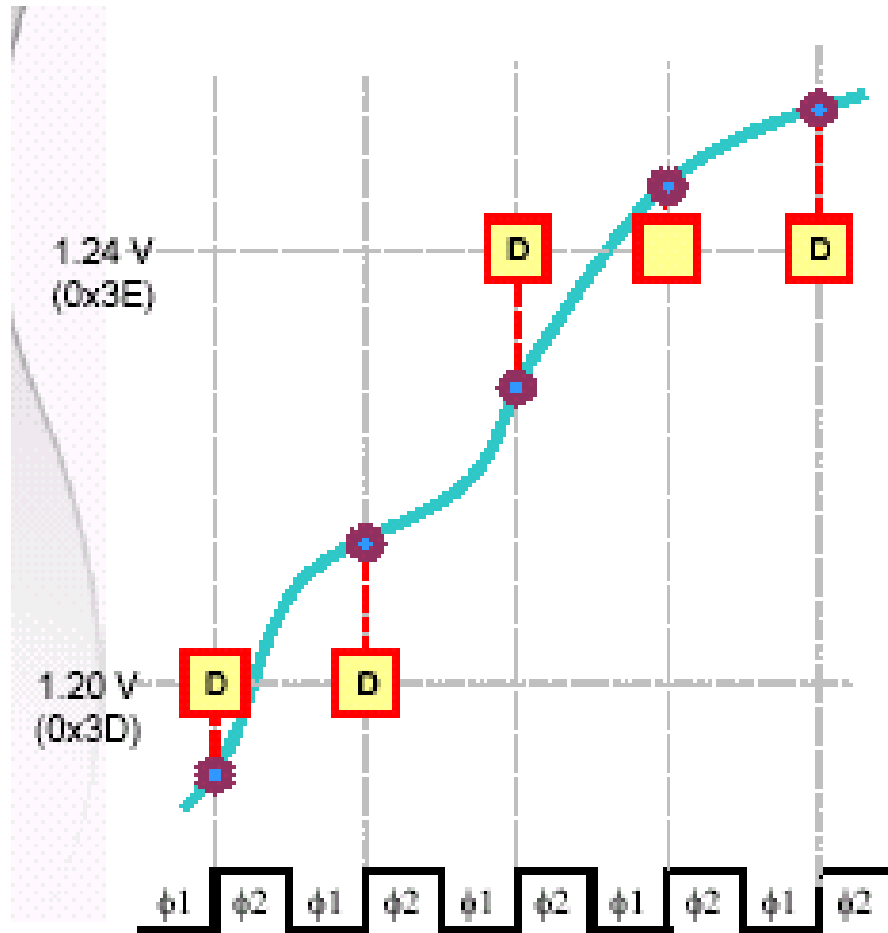
- any values, all the time



- Sampled data

- any value, discrete time intervals

# Дискретни и цифрови сигнали



- Both sampled analog and digital systems sample at discrete times, but:
- Sampled analog – can take on any voltage value
- Digital systems – capture the nearest quantized value

# Основни предимства на цифровата реализация

Цифровите блокове се реализират на основата на универсални или специализирани микропроцесори, логически схеми и/или FPGA, при което:

- Различни проекти могат да се реализират с еднакъв хардуер;
- Проектираните схеми имат много добра предсказуемост на функционирането;
- Проектираните схеми притежават възможност за програмиране и репрограмиране;
- Проектираните схеми могат да бъдат интегрирани с помощта на неособено прецизни цифрови технологии;
- Съществуват много ефективни формални методи, EDA инструменти и езици за програмиране за осигуряване на проектирането на системно ниво.

# Основни проблеми при проектирането на аналогови схеми

- Изисква високо ниво на експертиза при проектиране, реализация и тестване на схемите – добрият проект се основава на детайлно познаване на аналоговата схемотехника.
- Всеки проект започва от “нула” – пренасочването или персонализирането на съществуващ аналогов проект е тромава задача.
- Обикновено аналоговата част на проекта е отделена от системния процесор - аналоговите методи за проектиране са изолирани, докато софтуерно-ориентираните системи се разработват и проверяват с мощни и ефективни инструменти за проектиране.
- Липсата на аналогов еквивалент на FPGA и микрокомпютъра не позволява на аналоговата част да се включи в проектирането на системно ниво.

# Избягване на недостатъците на аналоговото проектиране чрез:

- Свеждане на аналоговото проектиране и изпълнение до най-високото ниво на абстракция (от компонент към функционално ниво), чрез създаване на универсални аналогови подсхеми с добра предсказуемост на функционирането.
- Опростяване на процеса на проектиране, за да се намали времето за проектиране.
- Осигуряване на взаимодействие на аналоговите периферни устройства с други части на системата, като се даде възможност за пренасочване и актуализиране в реално време на аналоговите функции в системата.



# Конфигурируеми програмируеми аналогови интегрални схеми

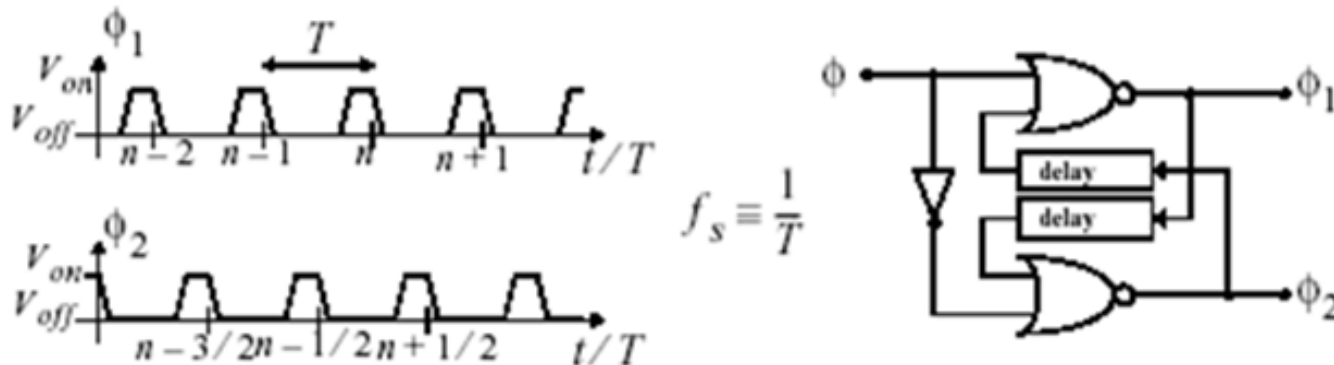
Опростяване и формализиране на аналоговите методи за проектиране чрез използване на **конфигурируеми програмируеми аналогови интегрални схеми**, които да осигуряват:

- реализацията на повторяеми и надеждни аналогови блокове;
- просто конфигуриране на функциите и програмиране на параметрите на проектираните аналогови модули чрез стандартен цифров интерфейс.

# SC схеми (Switched-Capacitor Circuits)

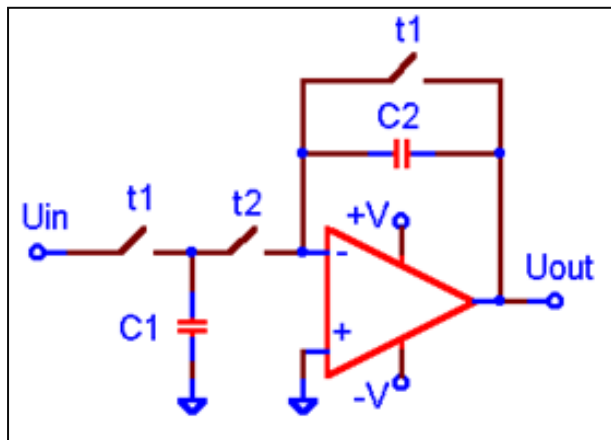
Основни принципи на изграждане:

- Базирани са на дискретната обработка на сигнали;
- Работят на принципа на прехвърляне и преразпределяне на заряд;
- Основните градивни компоненти на SC схемите са кондензаторите, операционните усилватели и аналоговите ключове, управлявани от две неприпокриващи се импулсни поредици;



- Схемите не съдържат резистори. Резисторите могат да бъдат реализирани с използване на кондензатори и аналогови ключове.

# SC инвертирац усилвател

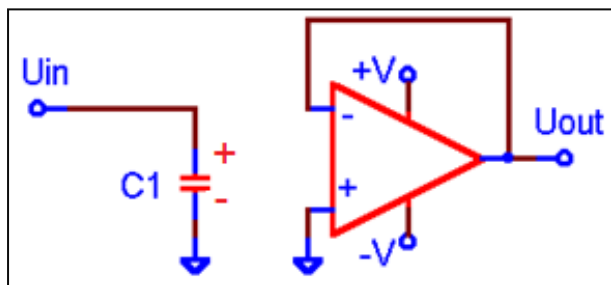


**t1** и **t2** - неприпокриващи се импулси

- **t1** е “1” (включен), **t2** е “0” (изключен) :

$$U(C1)=U_{in} \quad Q(C1)=C1.U_{in};$$

$$U(C2)=U_{out}=0; \quad Q(C2)=0$$



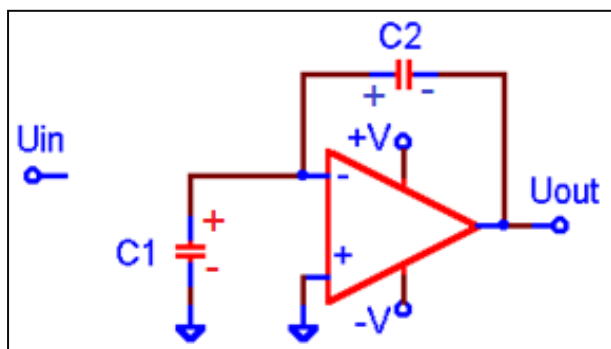
- **t1** е “0” (изключен), **t2** е “1” (включен):

Отрицателния вход на OpAmp се стреми към виртуална земя и заряда на  $Q(C1)$  се прехвърля в кондензатора  $C2$ .

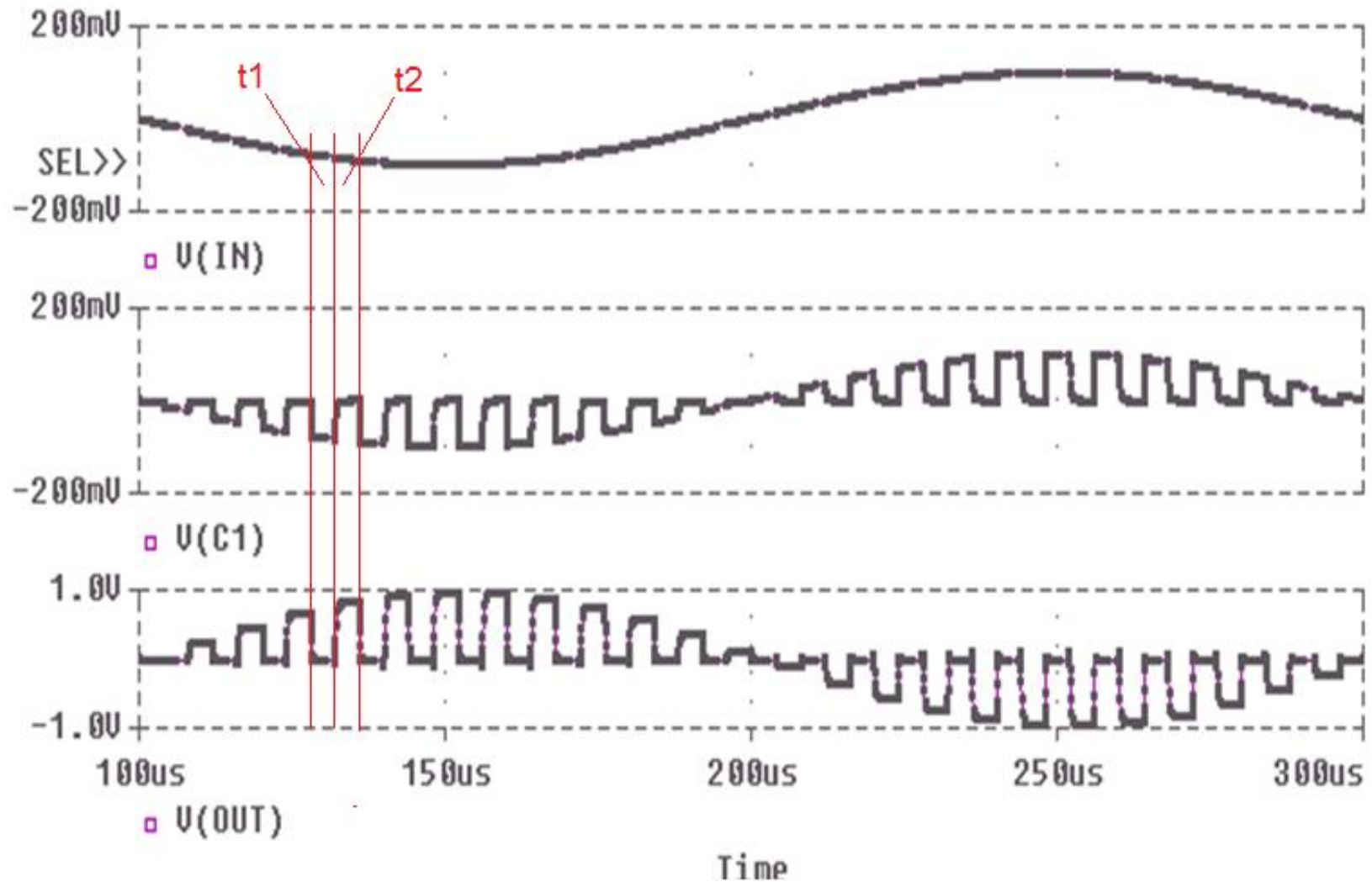
$$Q(C2)=C2.U(C2)=Q(C1)=C1.U_{in}$$

$$U(C2)=(C1/C2).U_{in}$$

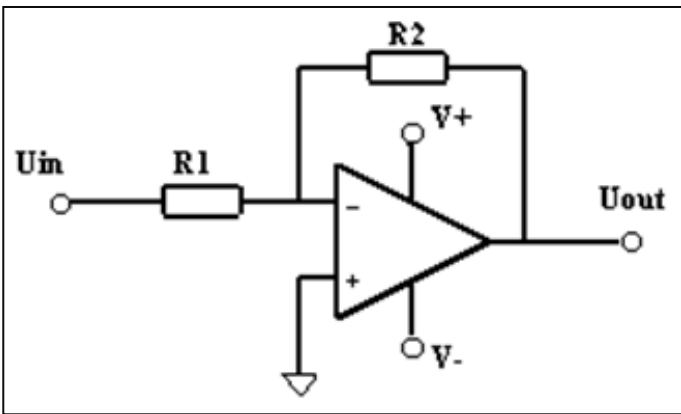
$$U_{out}= -U(C2)= -(C1/C2).U_{in}$$



# SC инвертиращ усилвател

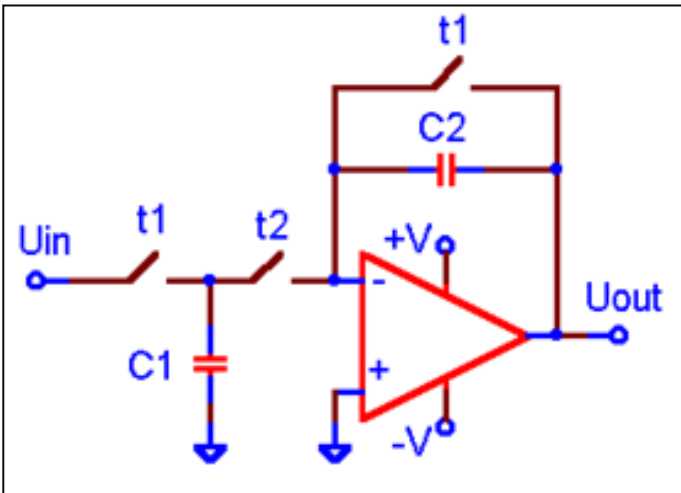


# Аналогов и дискретен инвертиращ усилвател



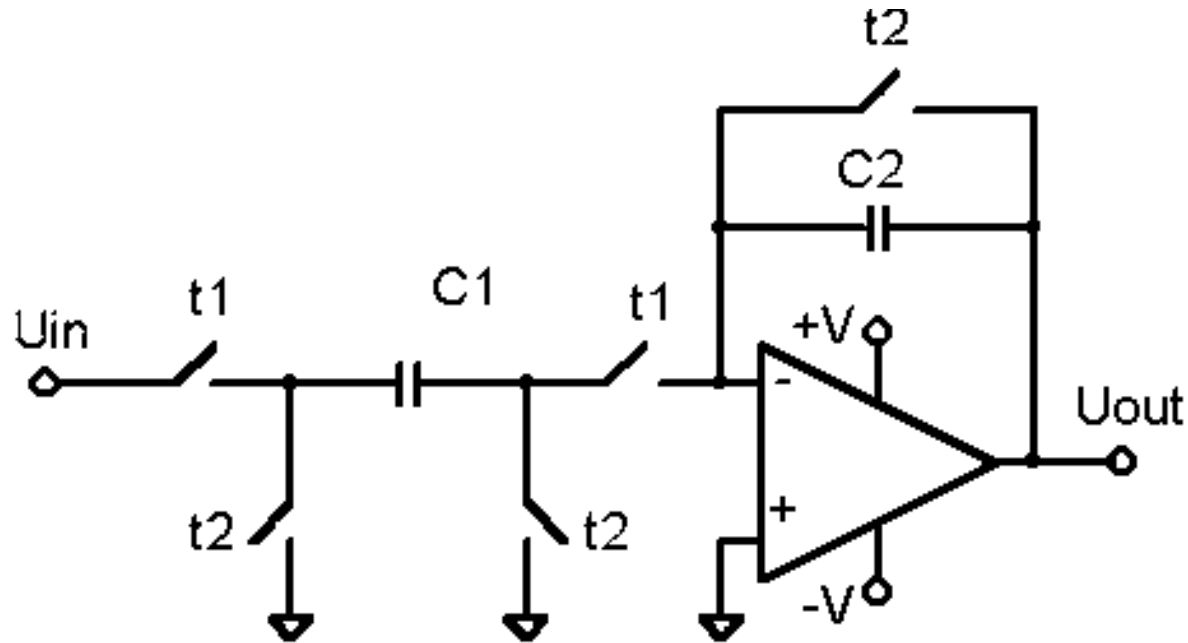
$$A_u = -\frac{R_2}{R_1}$$

SC схемотехниката реализира “еквивалентно съпротивление” чрез алтернативно превключване на входовете на кондензатор.



$$A_u = -\frac{C_1}{C_2}$$

# SC инвертирацц усилвател – втори вариант



$$C_1 U_{C1} = C_1 U_{in} = C_2 U_{C2}; \quad U_{C2} = \frac{C_1}{C_2} U_{in}$$

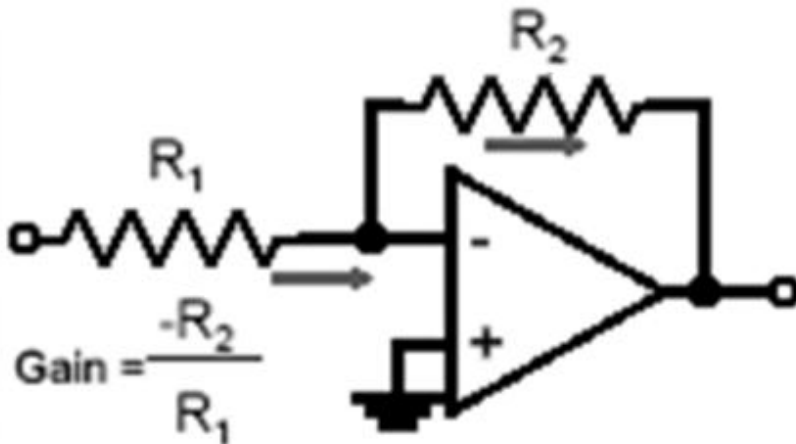
$$U_{out} = -U_{C2} = -\frac{C_1}{C_2} U_{in}$$

# Основни типове SC резистори

Switched Capacitor Resistor Emulation Circuit	Schematic	Equivalent Resistance
Parallel		$\frac{T}{C}$
Series		$\frac{T}{C}$
Series-Parallel		$\frac{T}{C_1 + C_2}$

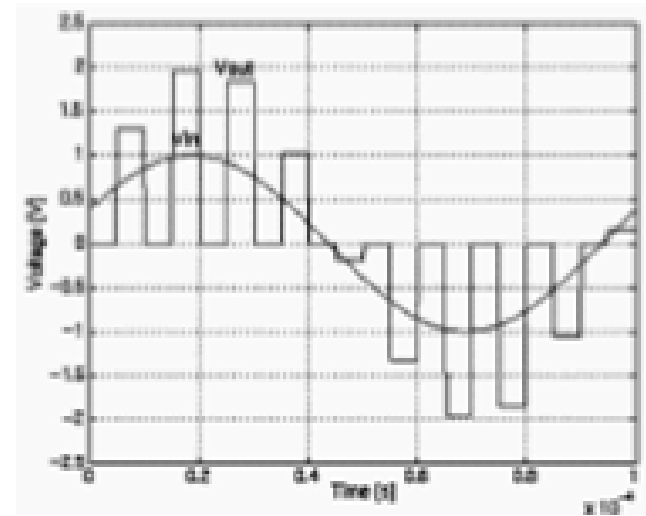
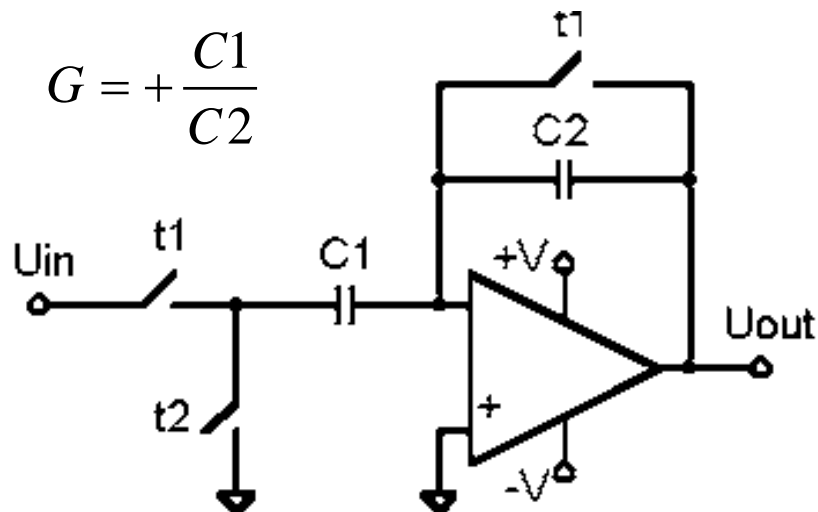
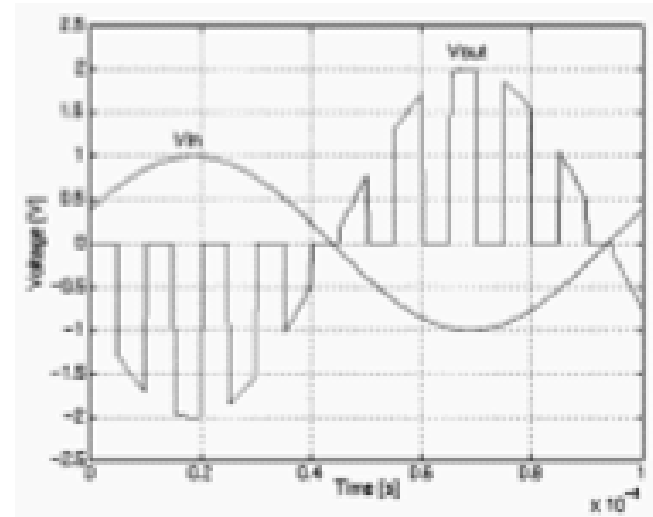
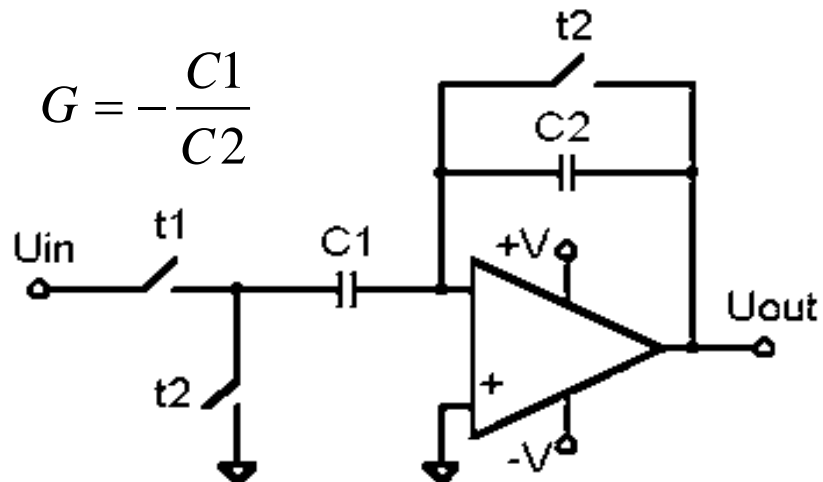
# Предимство на SC схемите – “отрицателно съпротивление”

Чрез размяна на управляващите тактови импулси може да се реализира “отрицателно съпротивление” и да се смени знака на предавателната функция.



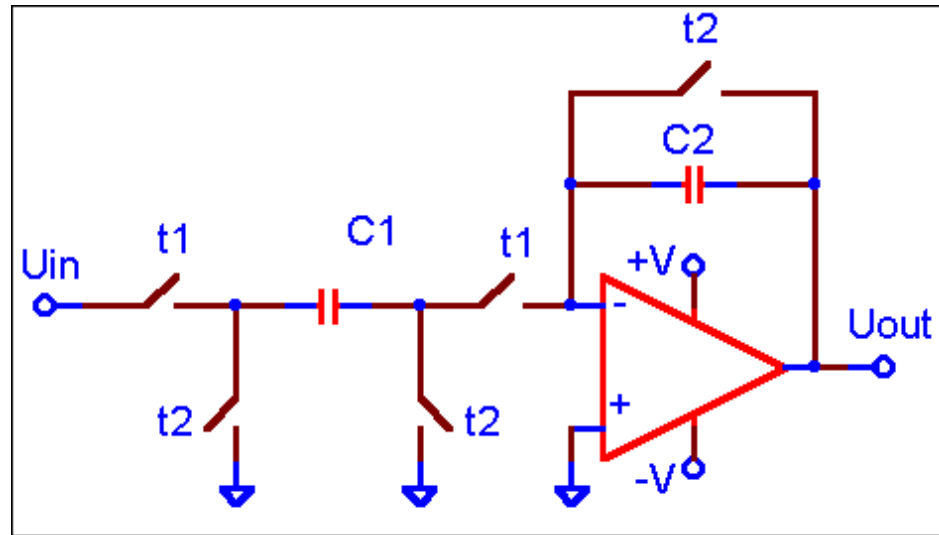


# Инвертирацц и неинвертирацц усилвател

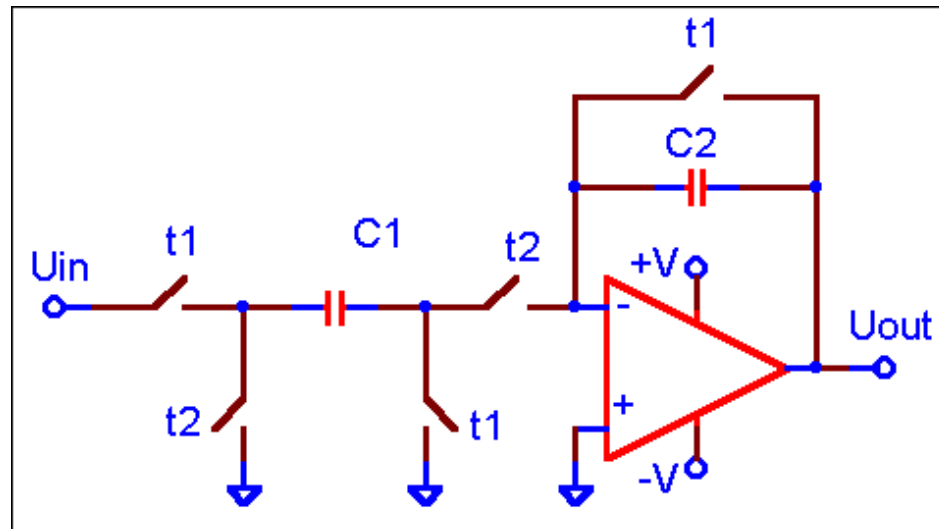


# Инвертирацц и неинвертирацц усилвател

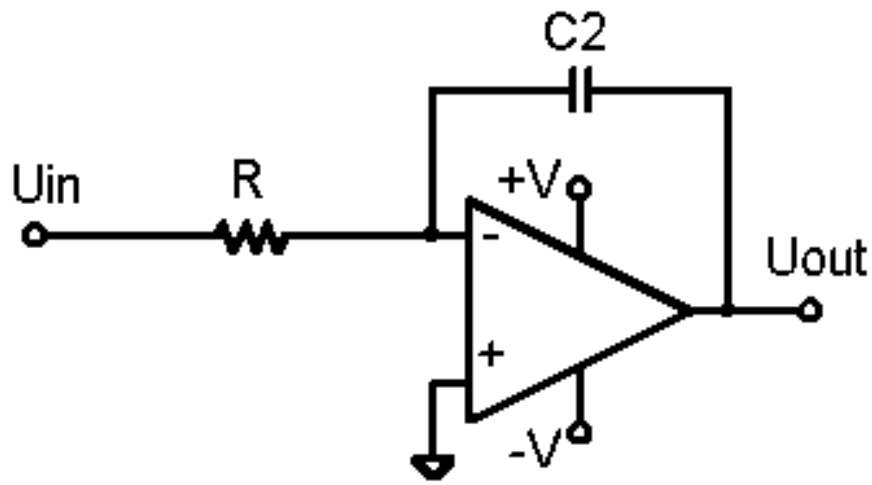
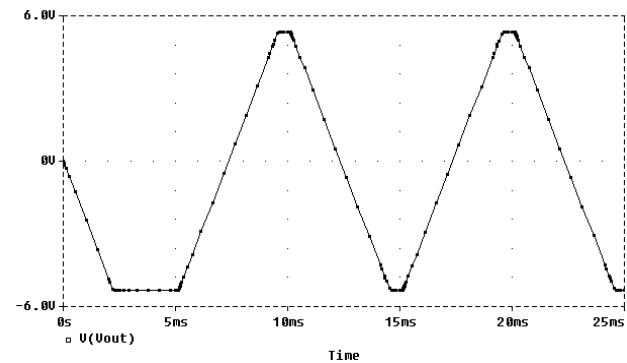
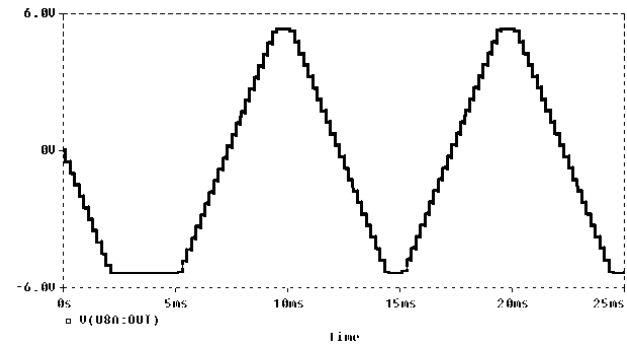
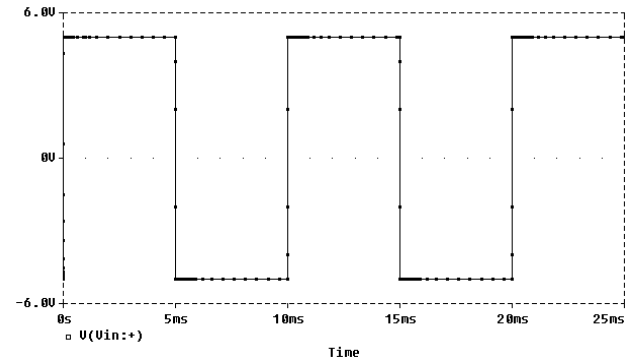
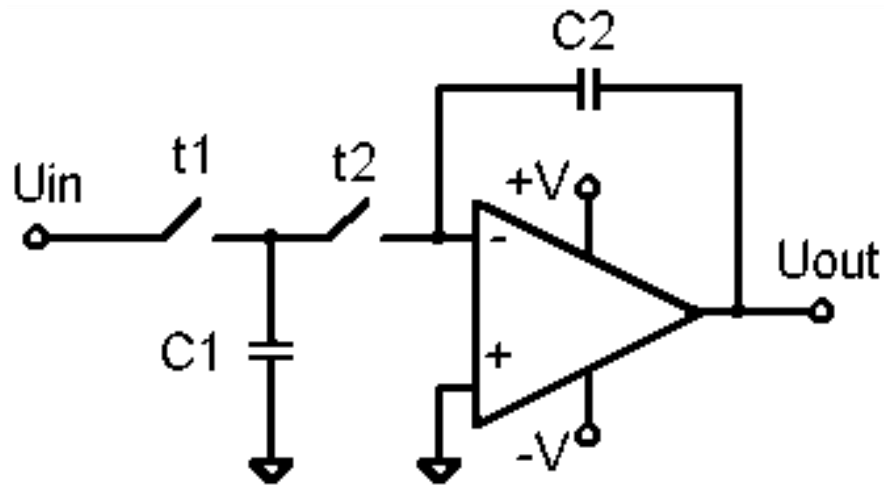
$$G = -\frac{C1}{C2}$$



$$G = +\frac{C1}{C2}$$



# Аналогов и дискретен интегратор



# Аналогов и дискретен интегратор

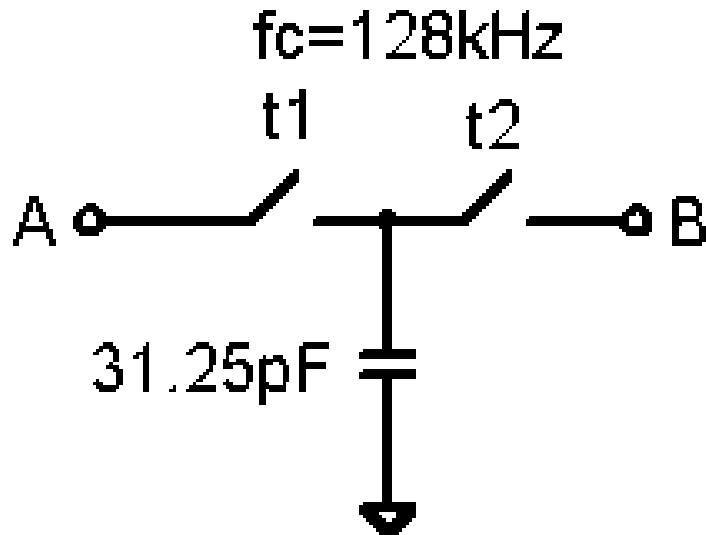
Дискретен интегратор:  $U_{out} = \Delta U \cdot n = \frac{C_1}{C_2} U_{in} \frac{t}{T_c} = \frac{C_1}{C_2} U_{in} \cdot f_c \cdot t$

Аналогов интегратор:  $U_{out} = \frac{I_R}{C_2} t = \frac{U_{in}}{RC_2} t$

$$\frac{C_1}{C_2} U_{in} \cdot f_c \cdot t = \frac{U_{in}}{RC_2} t; \quad C_1 \cdot f_c = \frac{1}{R}$$

$$R = \frac{1}{C_1 f_c} = \frac{T_c}{C_1}$$

# Предимство на SC резисторите – минимална площ



$$\text{AREA} \cong 0.115\text{mm}^2$$

$$R = \frac{T_C}{C} = \frac{1}{C \cdot f_C}$$



$$\text{AREA} \cong 5\text{mm}^2$$

# Предимство на SC схемите – реализация на прецизни времеконстанти

## Аналогов интегратор:

$$\tau = RC_2$$

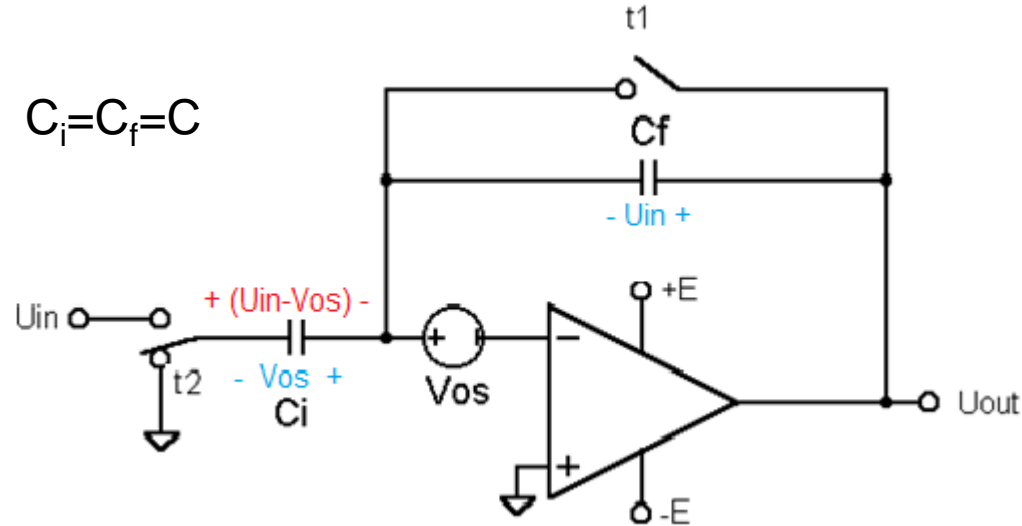
$$\frac{d\tau}{\tau} = \frac{dR}{R} + \frac{dC_2}{C_2} \rightarrow \pm 40\% \div \pm 65\%$$

## Дискретен интегратор:

$$\tau = \frac{1}{f_c C_1} C_2 = T_c \frac{C_2}{C_1}$$

$$\frac{d\tau}{\tau} = \frac{dT_c}{T_c} + \frac{dC_2}{C_2} - \frac{dC_1}{C_1} \approx \frac{dC_2}{C_2} - \frac{dC_1}{C_1} \rightarrow \pm 0,1\%$$

# Остатъчното входно напрежение при SC усилвателите



При включен  $t_1$  и изключен  $t_2$ :

$$U(C_i) = U_{in} - V_{os};$$

$$U(C_f) = 0V \Rightarrow U_{out} = V_{os}.$$

При изключен  $t_1$  и включен  $t_2$ :

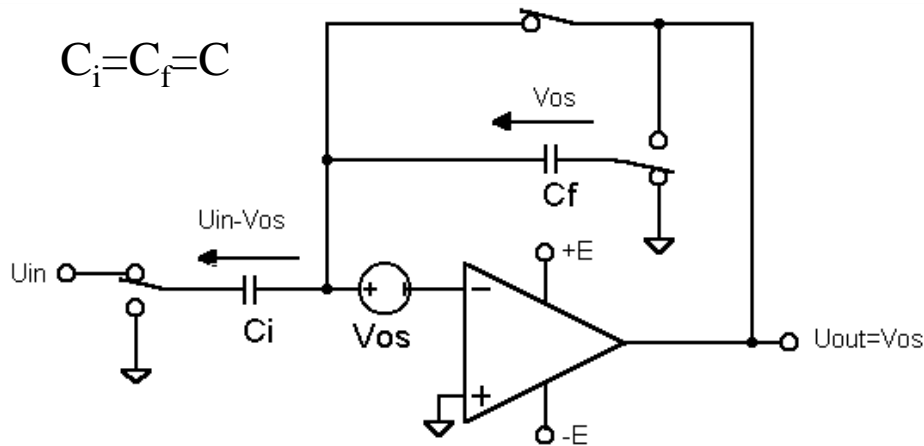
$C_i$  се разрежда от  $-(U_{in} - V_{os})$  до  $U(C_i) = V_{os}$ ;

Заряд  $\Delta Q(C_i) = C U_{in}$  се прехвърля в  $C_f$

$$U(C_f) = U_{in} \Rightarrow U_{out} = U_{in} + V_{os}$$

$V_{os}$	
0	+
$U_{in}$	
$-(U_{in} - V_{os})$	-

# Компенсация на остатъчното входно напрежение



При включен  $t_1$  и изключен  $t_2$ :

$$U(C_i) = U_{in} - V_{os}; Q(C_i) = C(U_{in} - V_{os})$$

$$U(C_f) = V_{os}; Q(C_f) = CV_{os}$$

$$U_{out} = V_{os}.$$

При изключен  $t_1$  и включен  $t_2$ :

$C_i$  се преразрежда от  $U(C_i) = -(U_{in} - V_{os})$  през нула до

$U(C_i) = V_{os}$ ; заряд  $\Delta Q(C_i) = CU_{in}$ ;

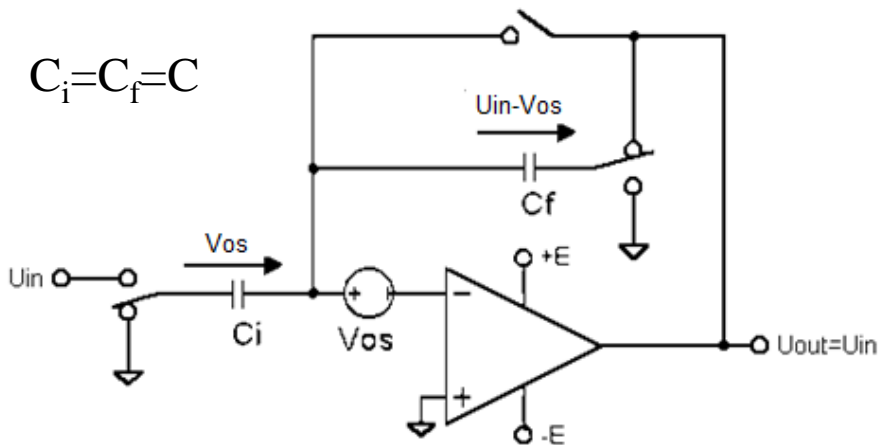
$$Q(C_f) = \Delta Q(C_i) - CV_{os} = C(U_{in} - V_{os})$$

$C_f$  се презарежда до  $(U_{in} - V_{os})$

$$U(C_f) = U_{in} - V_{os}$$

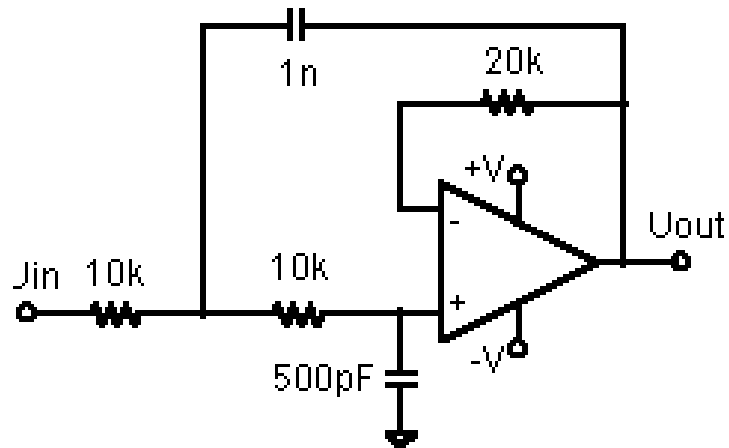
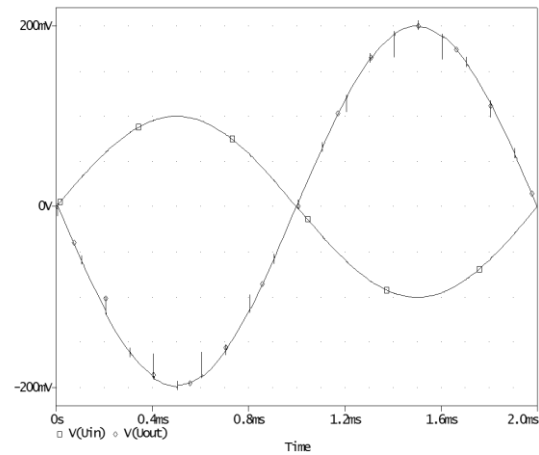
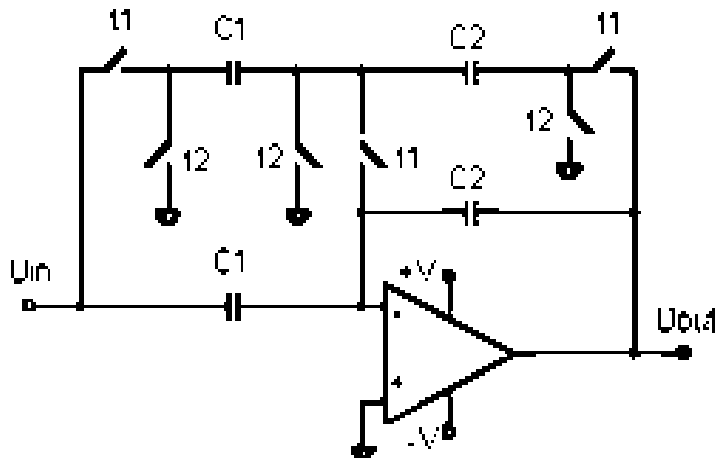
$$U_{out} = V_{os} + U(C_f) =$$

$$= V_{os} + (U_{in} - V_{os}) = U_{in}$$

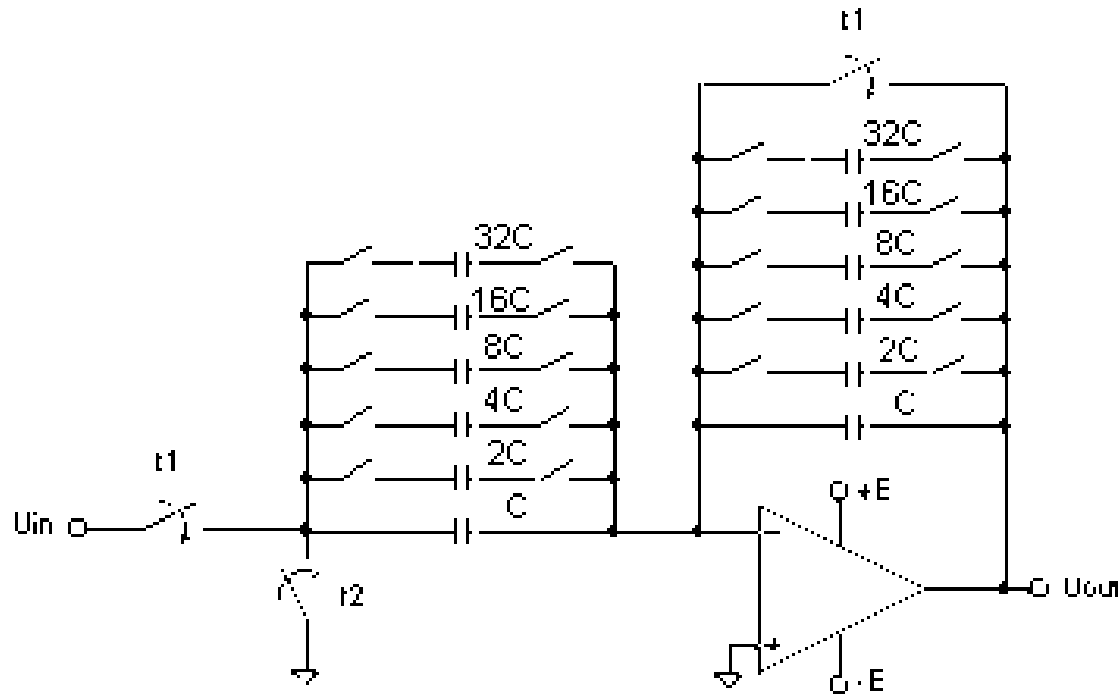




# Усилвател с пълен изходен цикъл и изглаждащ нискочестотен филтър

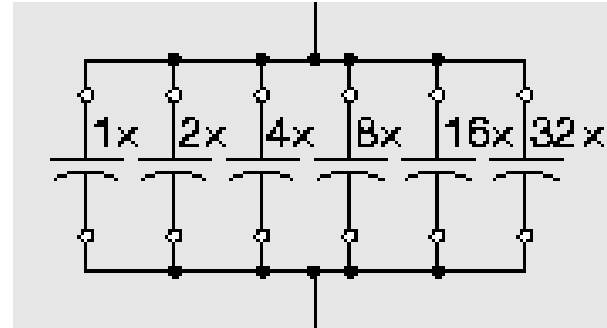
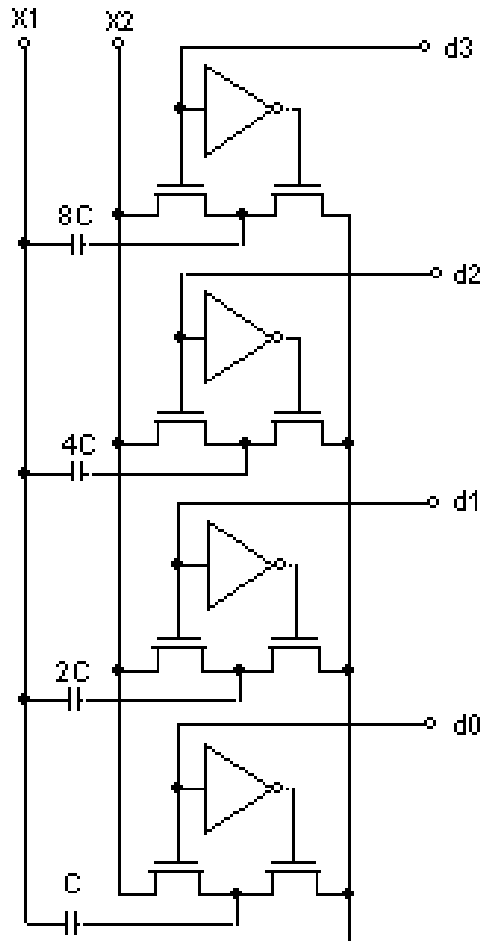


# Програмируем усилвател



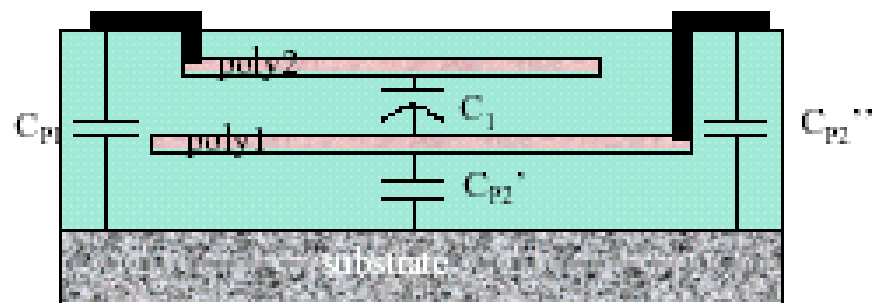
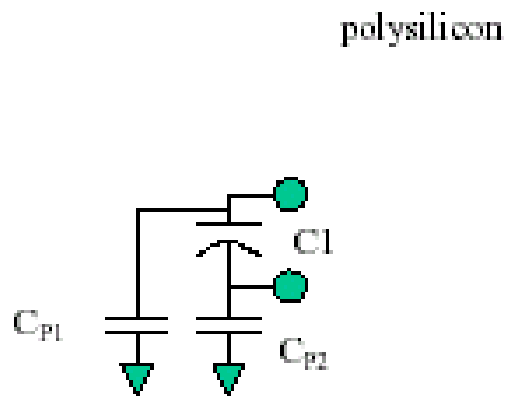
- Използва две 6-bit Programmable Capacitor Arrays (програмируеми капацитивни матрици) с  $C_{min} \approx 500 \text{ fF}$  и  $C_{max} \approx 31.5 \text{ pF}$ ;
- $G_{min} = 1/63$ ,  $G_{max}=63$ .

# Програмируема капацитивна матрица



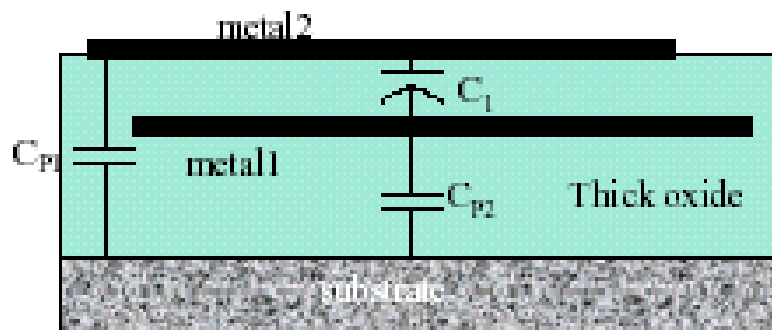
32	32	32	32	32	32	32	32
32	32	32	32	32	32	32	32
32	32	16	16	16	16	32	32
16	16	16	16	16	16	32	32
8	8	8	8	16	16	32	32
4	4	8	8	16	16	32	32
2	—	4	8	16	32	32	32
1	2	4	8	16	32	32	32

# Кондензатори



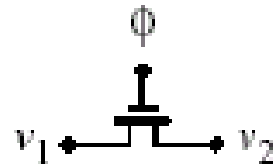
$C_{P1}$ ,  $C_{P2}''$  are very small (1-5 % of  $C_1$ )  
 $C_{P2}'$  is around 10-30 % of  $C_1$

metal1-metal2

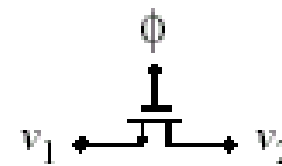


# MOS ключеве

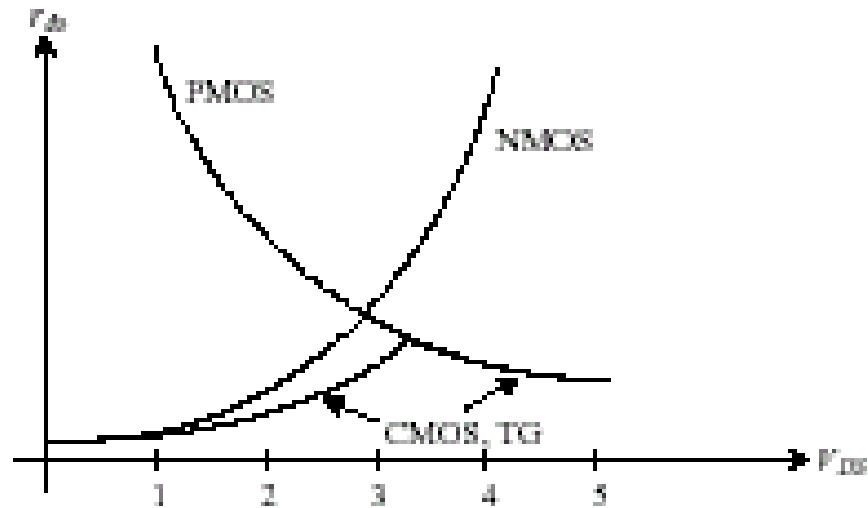
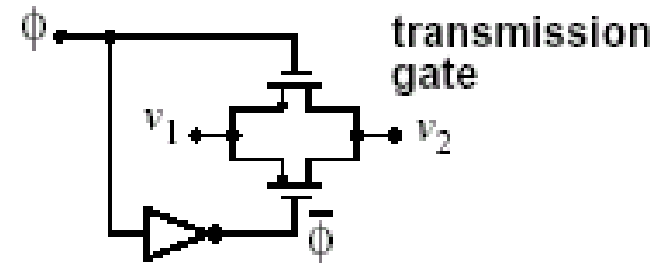
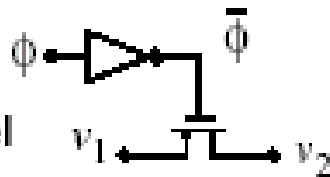
Symbol



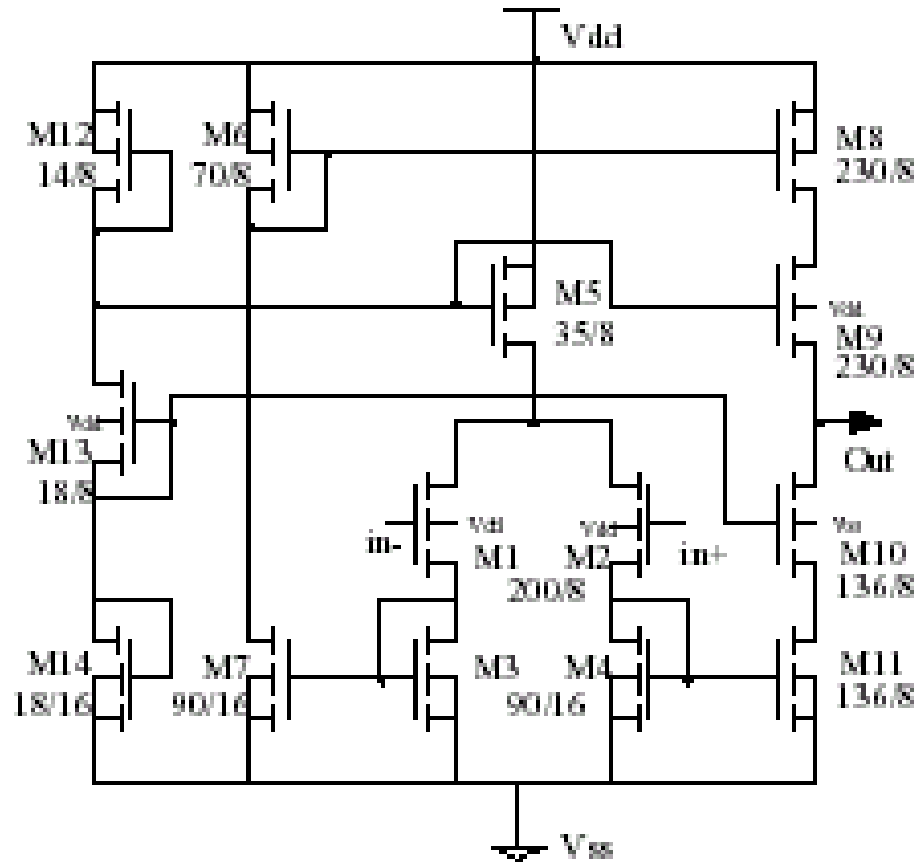
n-channel



p-channel



# Операционни усилватели

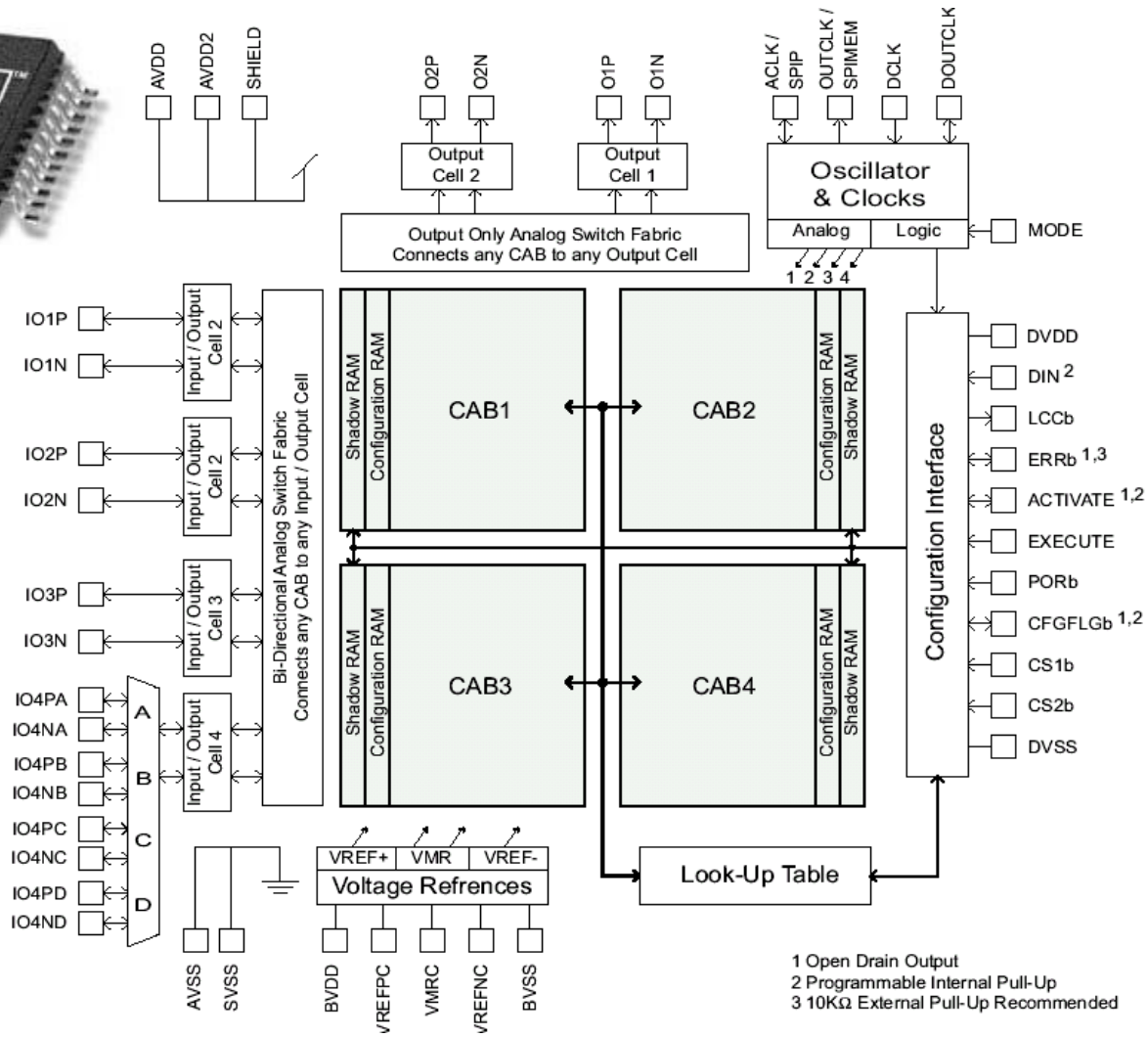


$$GBW > 5f_C$$

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# **FPAA Technology of Anadigm®**

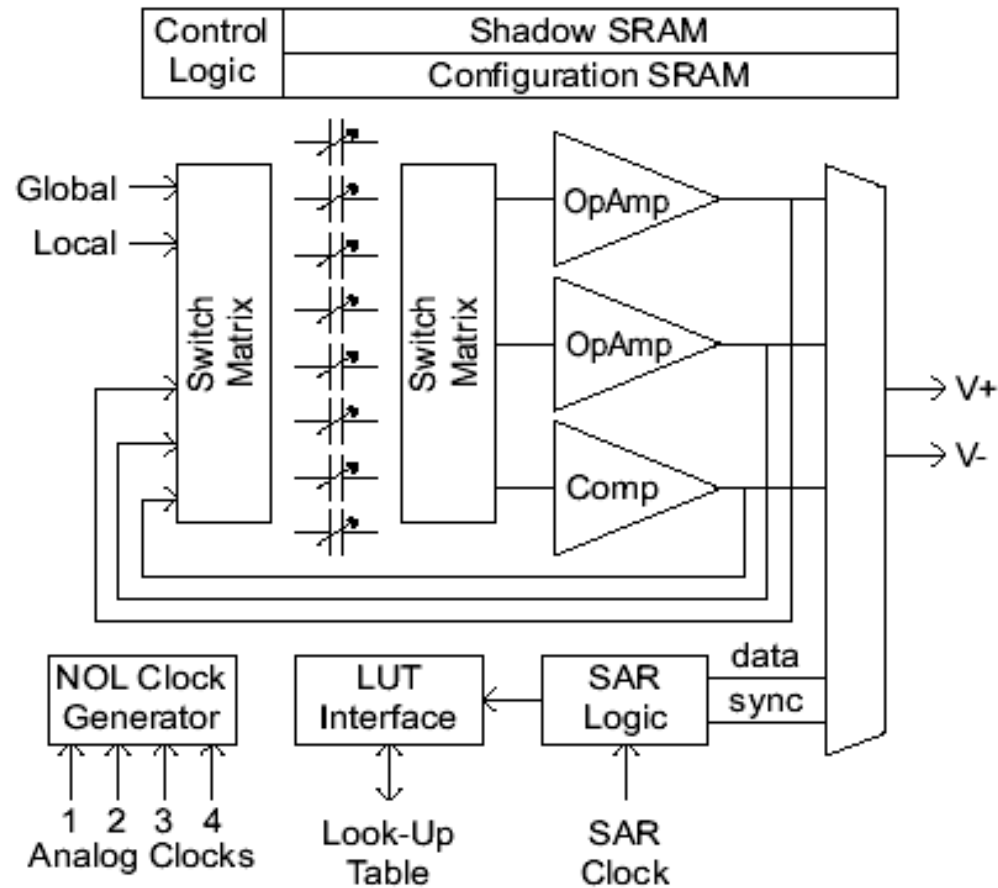
# FPAA Technology of Anadigm<sup>®</sup>





# FPAA Technology of Anadigm®

## Configurable Analog Block (CAB)



**The automation of the design of FPAA circuits is supported by specially developed CAD software tool (AnadigmDesigner2).**

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# FPAA Technology of Anadigm®

AnadigmDesigner2 contains a standard library of CAMs (Configurable Analog Modules), which includes the analog design know-how and ensures an optimal physical implementation of a circuit function and its high-level parametric setting.

To facilitate circuit design and experimentation without the need for any lab equipment, a functional simulator is included in the program. The simulator features an intuitive user interface and displays time domain results graphically.



## Examples: Programmable functions of CAB

- Inverting & Non-inverting Gain Stages;
- Half Cycle Gain Stage;
- Half Cycle Inverting Gain Stage with Hold;
- Gain Polarity Stage
- Inverting & Non-inverting Comparator;
- Inverting & Non-inverting Differentiator;
- Bilinear Filter;
- Biquadratic Filter;
- Sample and Hold;

## Examples: Programmable functions of CAB (cont.)

- Multiplier/Divider;
- Sinewave Oscillator;
- Arbitrary Periodic Waveform Generator;
- Rectifiers;
- Half Cycle Sum/Difference Stage;
- Inverting Sum Stage;
- User-defined Voltage Transfer Function;
- DC Voltage Source;
- Sum/Difference Stage with Low Pass Filter.

**Complex analog designs without having to think on the level of op amps, capacitors, resistors, transistors, or current mirrors can be developed in a “chip” simply by selecting, configuring, placing and wiring different CAMs.**

## Examples for functional blocks implemented with several CABs:

- Analog multiplexer;
- Multiplier with filter;
- Voltage controlled gain stage;
- Peak detector with hold;
- Triangle wave oscillator;
- Digital phase-shift key modulator;
- Phase comparator;
- Phase/frequency detector;
- Voltage controlled oscillator.



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# FPAA Technology of Anadigm®

By using specially developed **Anadigm Evaluation Board**, the designer can fulfill the practical verification of the projects.

This board allows AN221E04 FPAA to be programmed via the serial port of the personal computer under control of the AnadigmDesigner2 software.

The configuration data for the designed circuit is sent automatically to a programmable chip. After the chip begin functioning immediately as the constructed circuit and the real results can be seen directly by using a signal generator and an oscilloscope.

# FPAA Technology of Anadigm®



**Anadigmvortex AN221D04 Evaluation Board**

# FPAA Technology of Anadigm®

## Features of Evaluation board:

- Evaluation board comprises of a single AN221E04 device.
- FPAA can be configured from:
  - a PC running the AnadigmDesigner®2 software;
  - by using an on-board EPROM;
  - or via the user's own digital system.
- The input/output signals can be presented:
  - via SMA connectors (single-ended ground referenced signals);
  - or via a stereo jack.
- All AN221E04 FPAA input and output signals can be accessed directly via header pins.

# FPAA Technology of Anadigm<sup>®</sup>



**Anadigmvortex AN221K04 Evaluation Board**

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# FPAA Technology of Anadigm®

The described advanced and very user-friendly products offer an attractive way of reducing costs, size and complexity of the electronic circuits, as well as to simplify and formalize the analog design methods.

This imposes the development of different research and educational experiments in order to train designers in the use of this modern technology.

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# **FPAA Applications**

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# FPAA Applications

Some **typical applications of FPAA** are presented in **<http://www.anadigm.com>**.

The most attractive of them are:

- sensor interfacing and signal conditioning;
- analog control circuits;
- complex filtering;
- photodiode interfacing;
- audio signal processing;
- ultra low-frequency analog processing for medical purposes;
- programmable analog front-end;
- compression and expansion;
- laser control.

These applications can be used directly for individual self-training of the students.

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# FPAA Applications

Objects of the current presentation are some of the new experiments that were developed and applied in the research and educational practice at the Faculty of Electronic Engineering and Technology of Technical University of Sofia.



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# FPAA Applications

The developed experiments include:

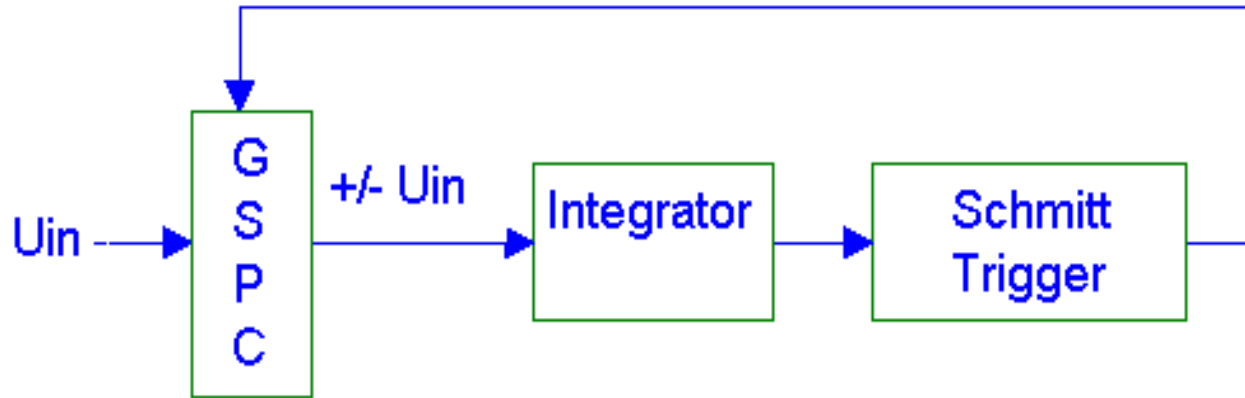
- design and examination of different pulse circuits;
- analog computational circuits;
- threshold logic and analog neuron circuits.

# FPAA Applications – Pulse Circuits

The FPAA technology proposes very appropriate resources for implementation of different pulse circuits. They have been applied in the design and investigation of:

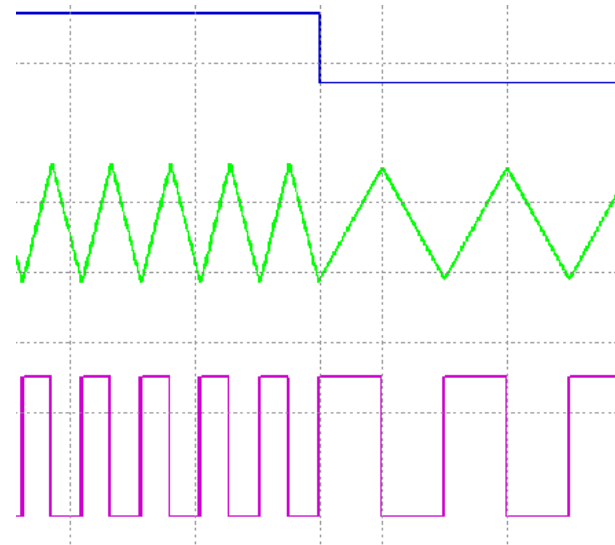
- many variants of Schmitt trigger circuits;
- square-wave generators;
- pulse width modulator circuit;
- voltage-to-frequency converter.

# FPAA Applications - V-f Converter

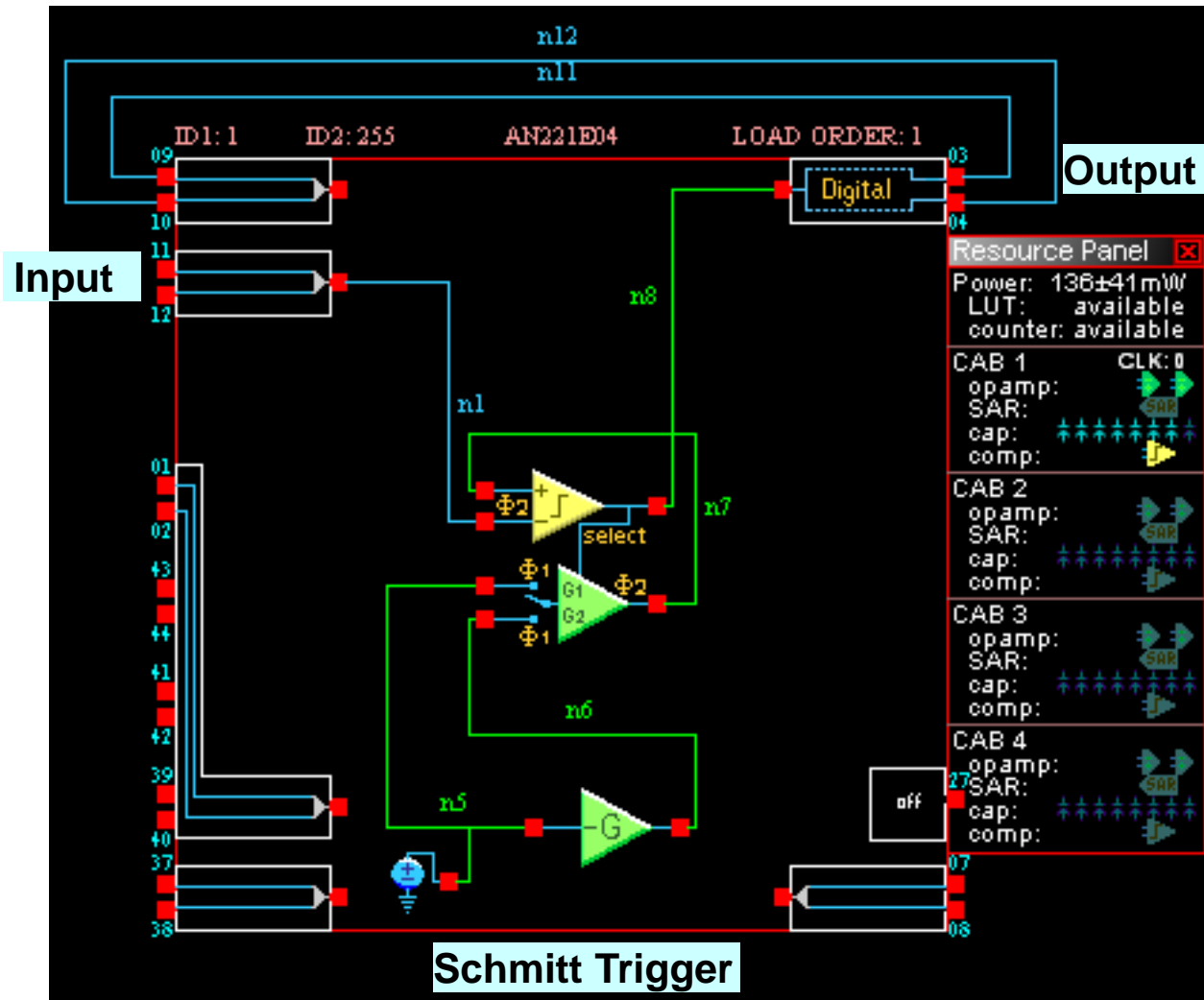


**GSPC - Gain Stage with Polarity Control**

$$T = \frac{k}{2} \frac{U_{in}}{(UTP - LTP)}$$



# FPAA Applications - V-f Converter



# FPAA Applications - V-f Converter

Sm\_Tr.ad2 - AnadigmDesigner2

File Edit Simulate Configure Settings Dynamic Config Target View Tools Help

### Set CAM Parameters

ANx21 Standard (GainSwitch 1.0.5): Gain Stage with Switchable Inputs Anadigm Approved CAM

Instance name and clock frequency  
Instance Name: GainSwitch1  
CLOCKA (kHz): 4000 0

Notes  
\*\*\*\*\*WARNING\*\*\*\*\*  
It is not recommended to route the output of this CAM to an Output Cell when this CAM's clock (CLOCKA) has a frequency greater than 2 MHz.  
\*\*\*\*\*WARNING\*\*\*\*\*

Symbol

CAM Options  
Compare Control To:  Signal Ground  Dual Input  Variable Reference  
Select Input 1 When:  Control High  Control Low  
Comparator Sampling:  Phase 1  Phase 2  
Gain Stage:  Half Cycle  Low Pass Bilinear

CAM Parameters

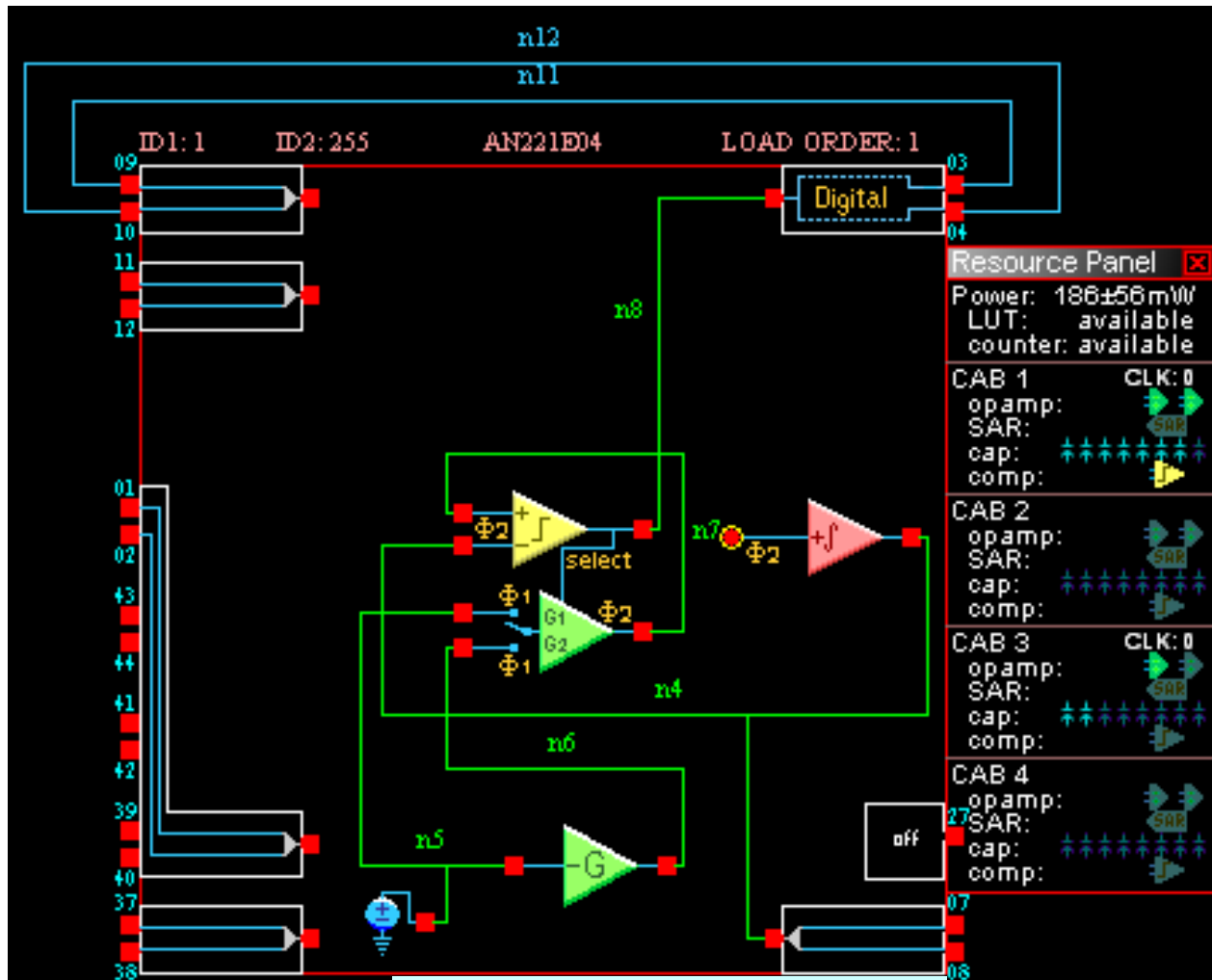
Parameter:	Value:	Limits:	Realized
Gain 1 (UpperInput)	0.5	-1.05 To 1.05	0.500
Gain 2 (LowerInput)	0.5	-1.05 To 1.05	0.500

OK  
Cancel  
Help  
Documentation  
C Code...

Use mouse to drag object in workspace

Start NOD32 Anti... Exploring... Microsoft... Microsoft... Microsoft... Stefan A... Microsoft... Sm\_Tr... 17:27

# FPAA Applications - V-f Converter



Schmitt Trigger+Integrator

# FPAA Applications - V-f Converter

**Set CAM Parameters** [?] [X]

ANx21 Standard (Integrator 3.0.5): Integrator      Anadigm Approved CAM


Instance name and clock frequency

Instance Name:

CLOCKA (kHz)

Notes

Symbol



OK

Cancel

Help

Documentation

C Code...

CAM Options

Polarity       Non-inverting       Inverting

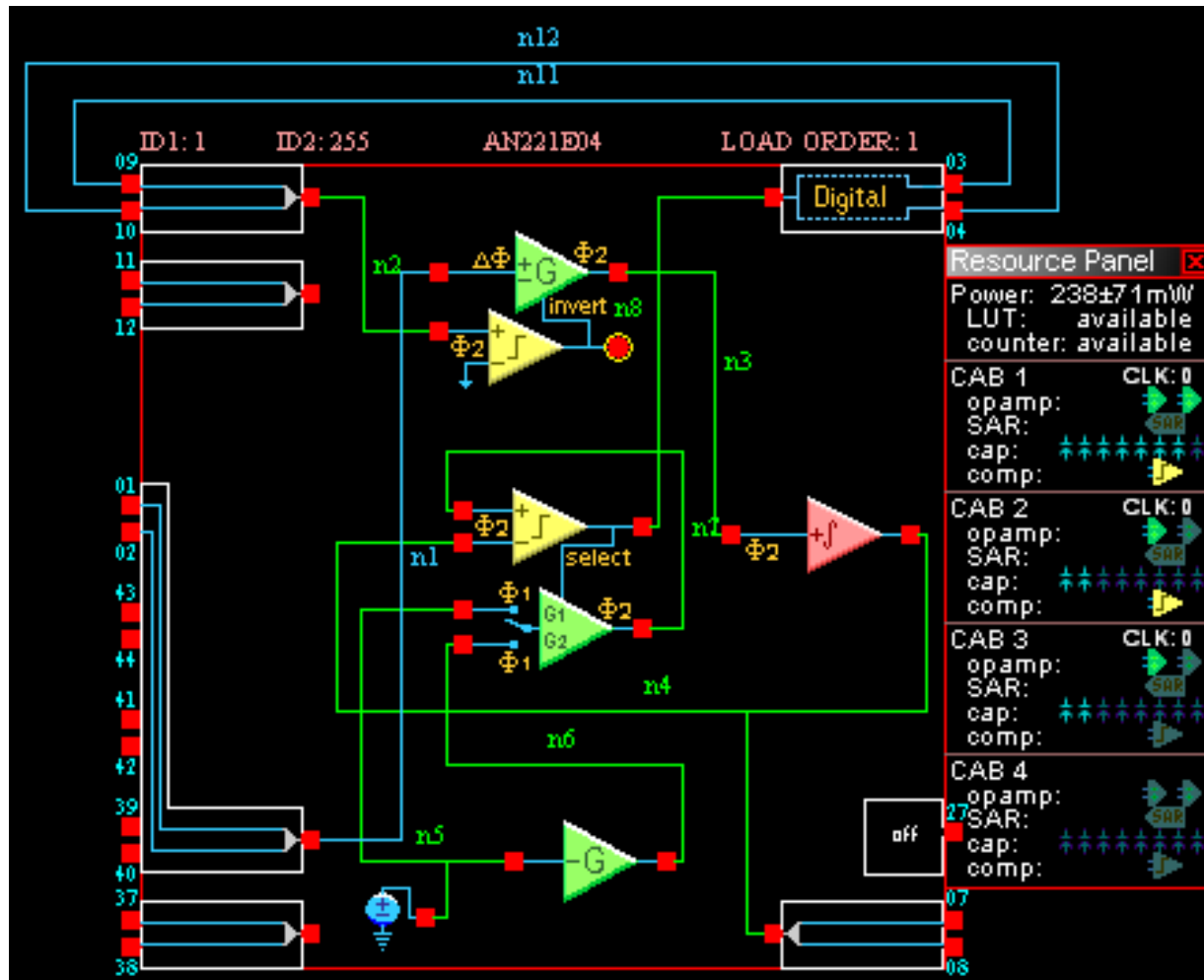
Input Sampling       Phase 1       Phase 2

Compare Control To       No Reset       Signal Ground       Dual Input       Variable Reference

CAM Parameters

Parameter:	Value:	Limits:	Realized
Integration Const. [1/us]	<input type="text" value="0.2"/>	0.0200 To 6.20	0.200

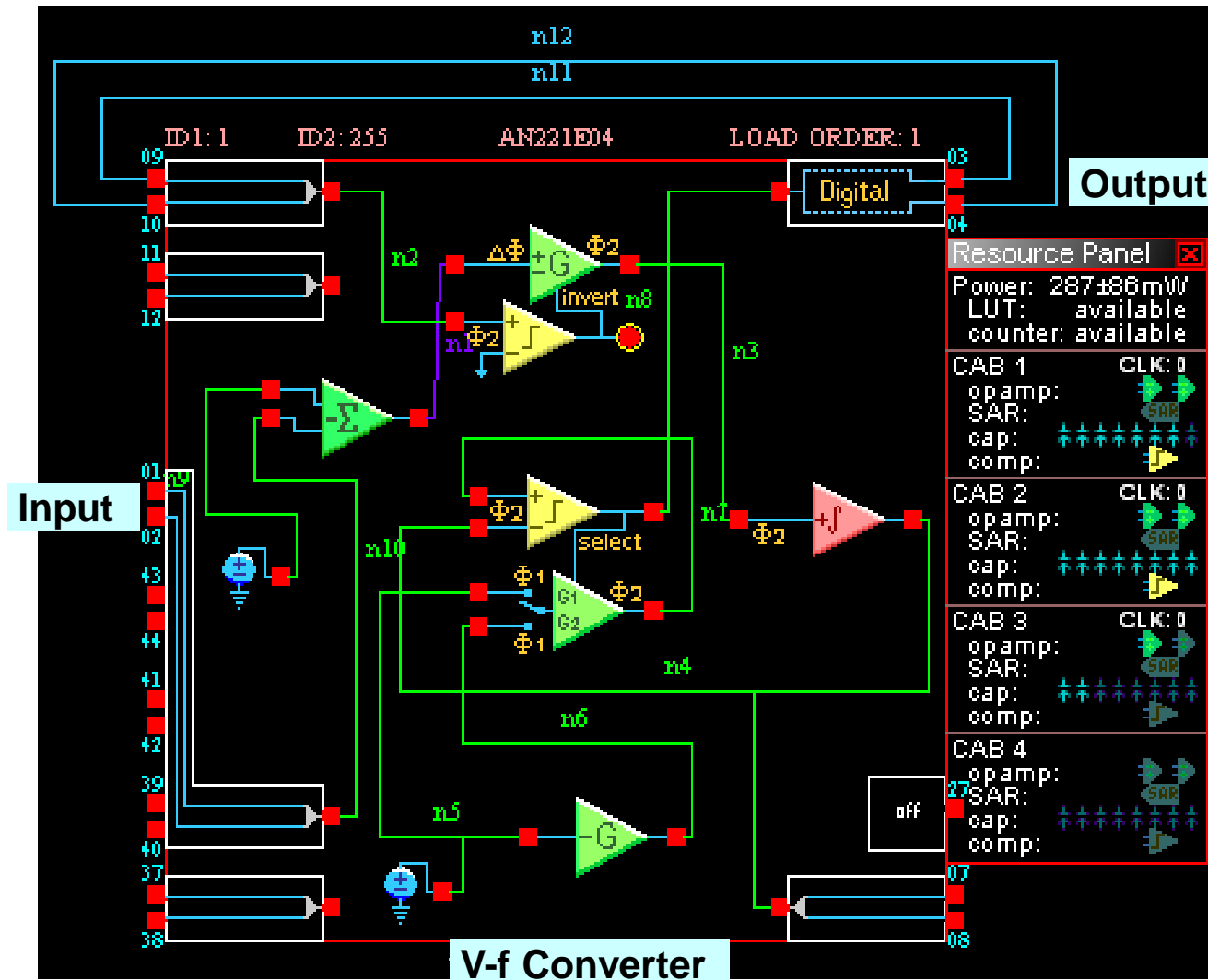
# FPAA Applications - V-f Converter



Schmitt Trigger + Integrator + Gain Stage with Polarity Control

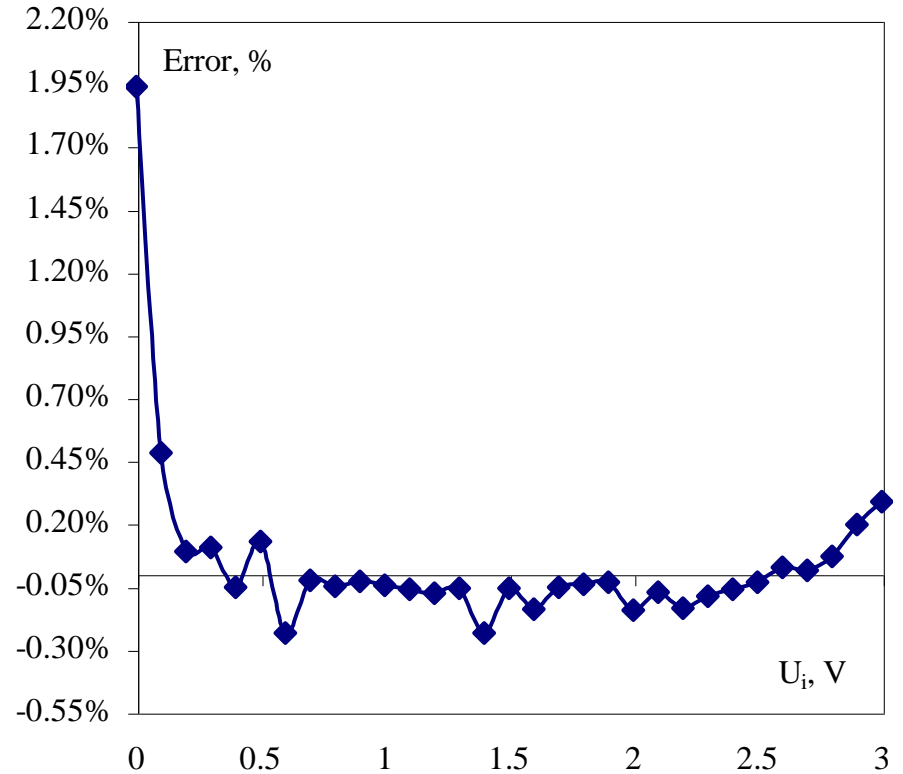
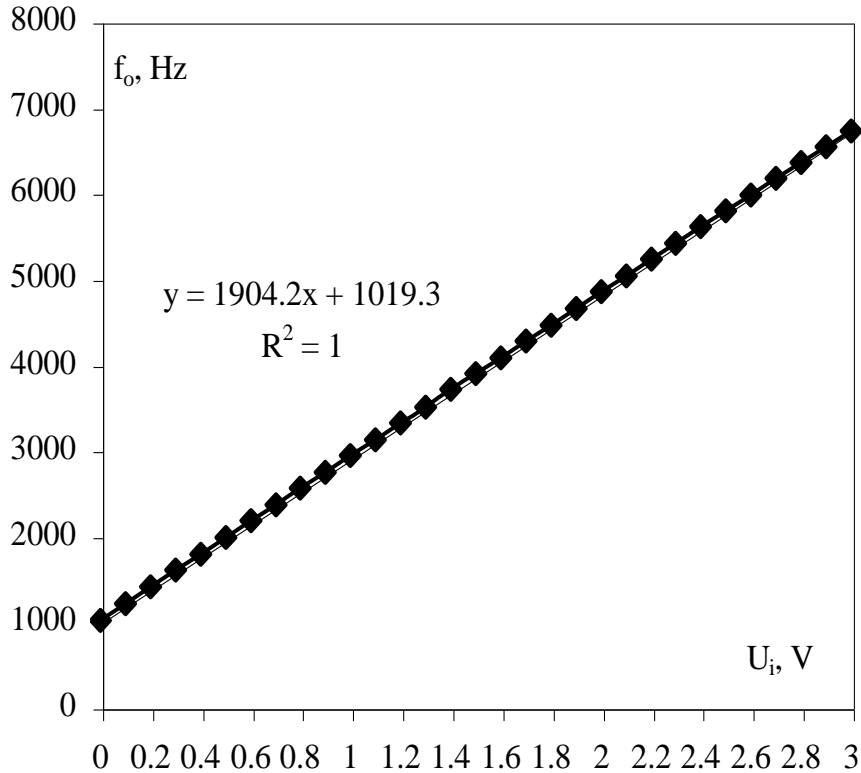


# FPAA Applications - V-f Converter



# FPAA Applications - V-f Converter

## Final Results



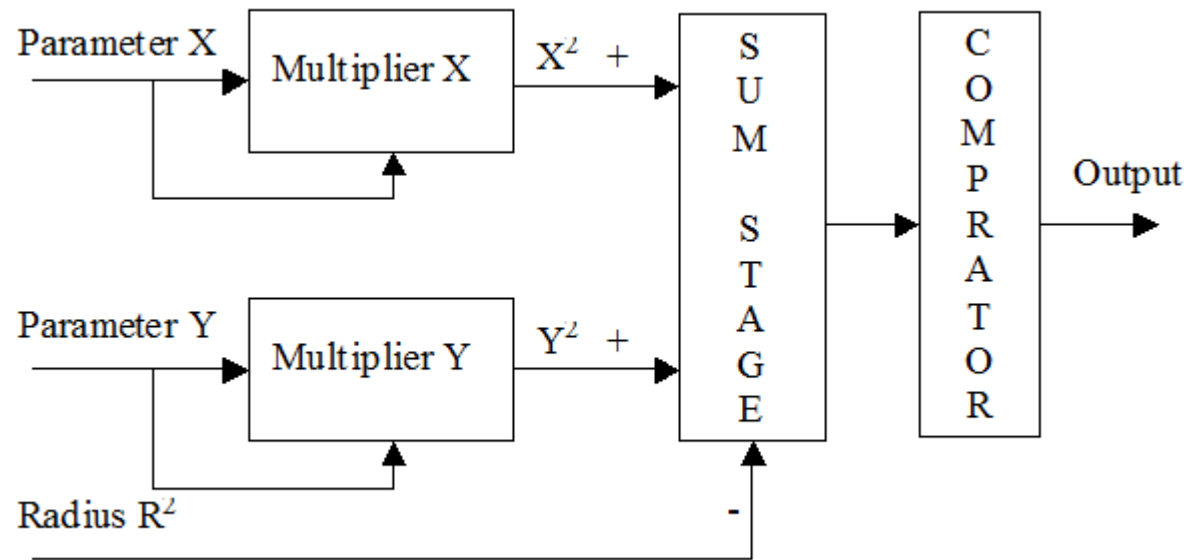
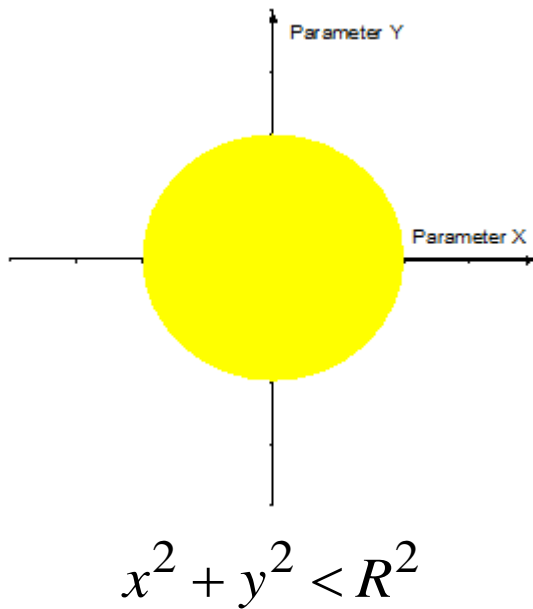
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# FPAA Applications - Computational Circuits

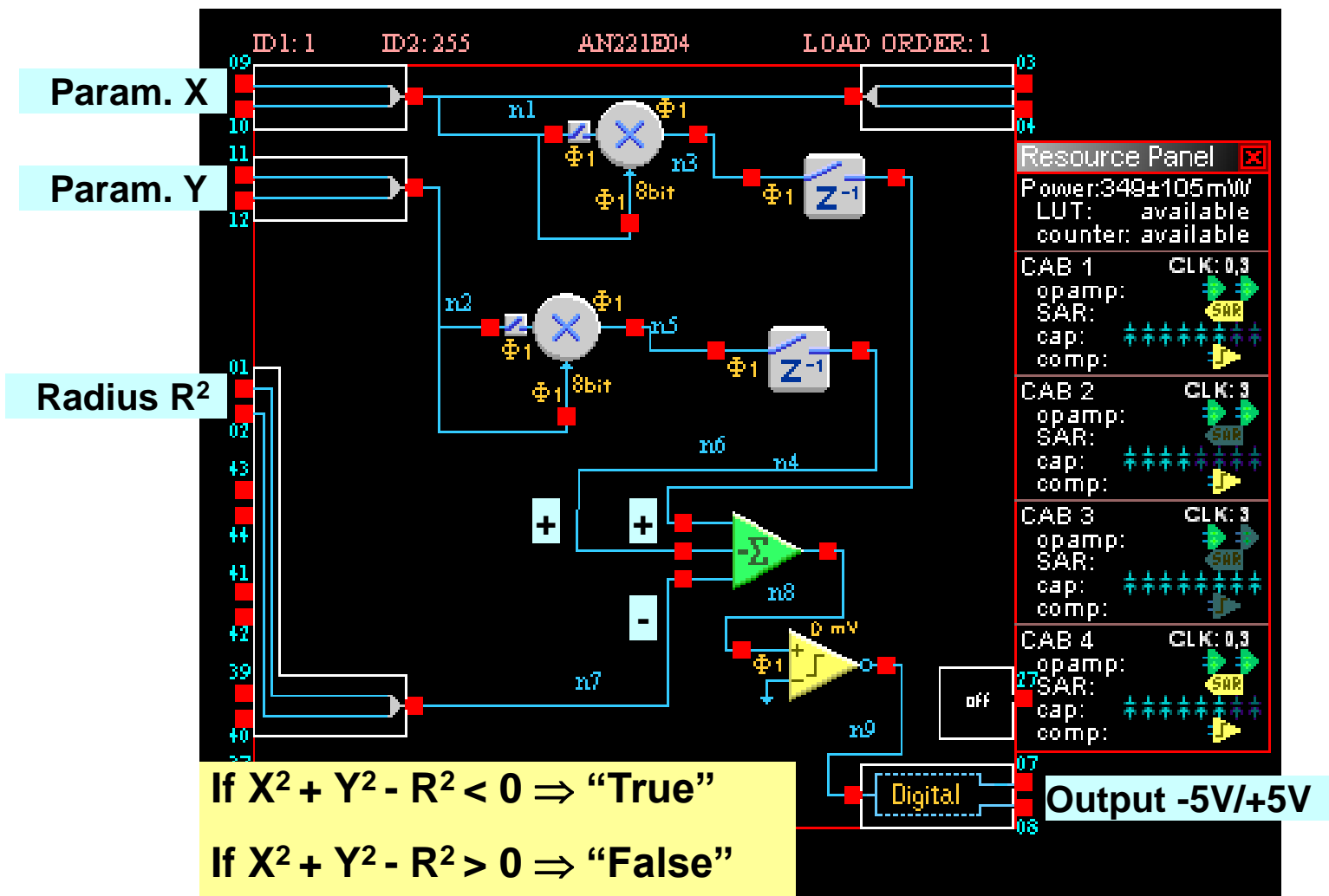
The CAM resources of AN221E04 chip include different components for linear and nonlinear computations – multipliers, dividers, square root circuit, look-up table, etc.

Different types of computational circuits - for transformation of data from polar to Cartesian coordinates, for sensor signals linearization, for generation of complex transfer function, etc. can be implemented by using mathematical CAMs.

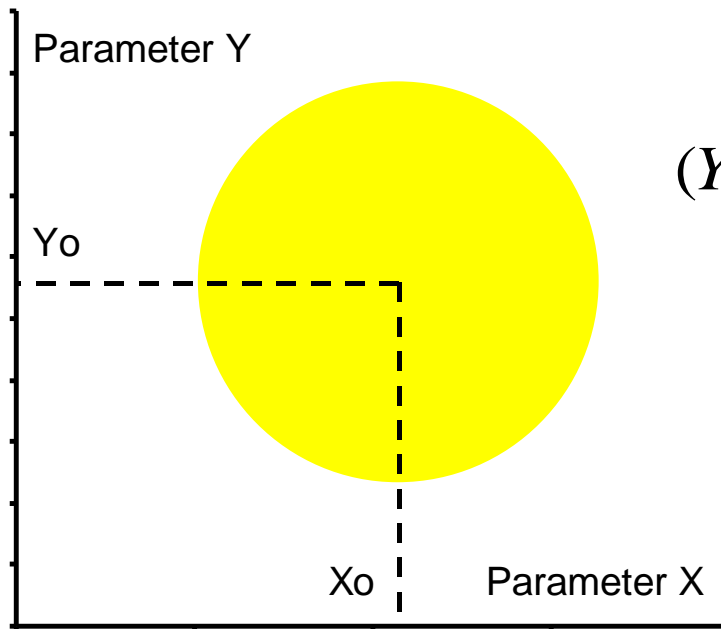
# FPAA Applications - Two-Parameter Test Circuit



# FPAA Applications - Two-Parameter Test Circuit

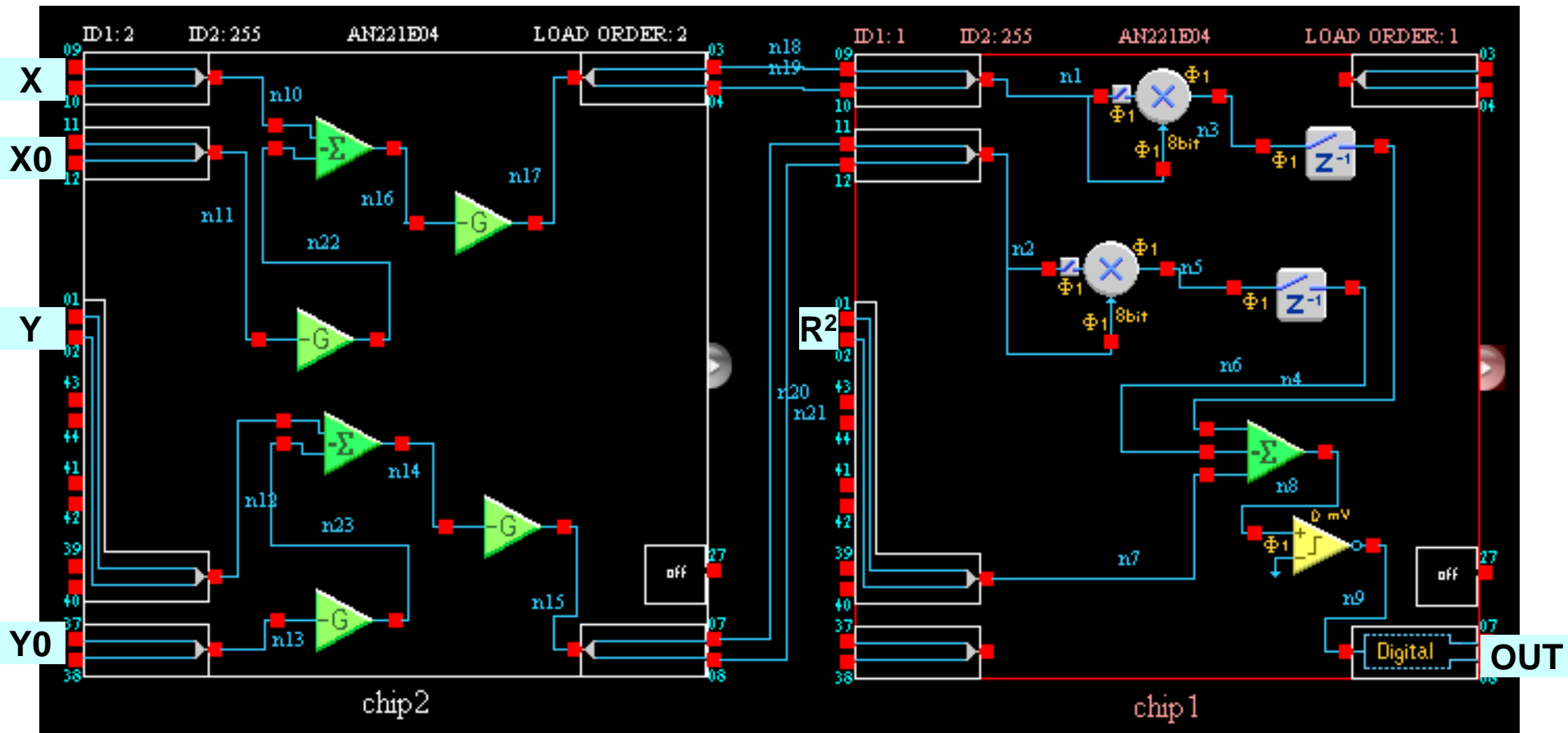


# FPAA Applications - Two-parameter Test Circuit



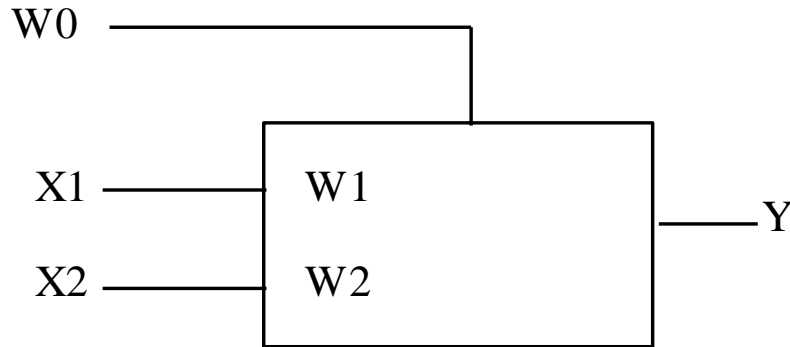
$$(Y - Y_0)^2 + (X - X_0)^2 - R^2 < 0$$

# FPAA Applications - Two-parametric Test Circuit



# FPAA Applications - Threshold Logic

## 2-Input Threshold Logic Circuit



$$Y = '1' \Rightarrow +1V, \text{ if } W_0 + \sum_{i=1}^n W_i X_i > 0$$

$$Y = '0' \Rightarrow -1V, \text{ if } W_0 + \sum_{i=1}^n W_i X_i < 0$$

$$Y = F(W_0, W_1, W_2)$$

$$F(-0.5, 1, 1) = X_1 \wedge X_2$$

$$SUM = -0.5 + X_1 + X_2$$

X1	X1,V	X2	X2,V	SUM,V	Y
0	-1	0	-1	-2.5	0
0	-1	1	1	-0.5	0
1	1	0	-1	-0.5	0
1	1	1	1	1.5	1

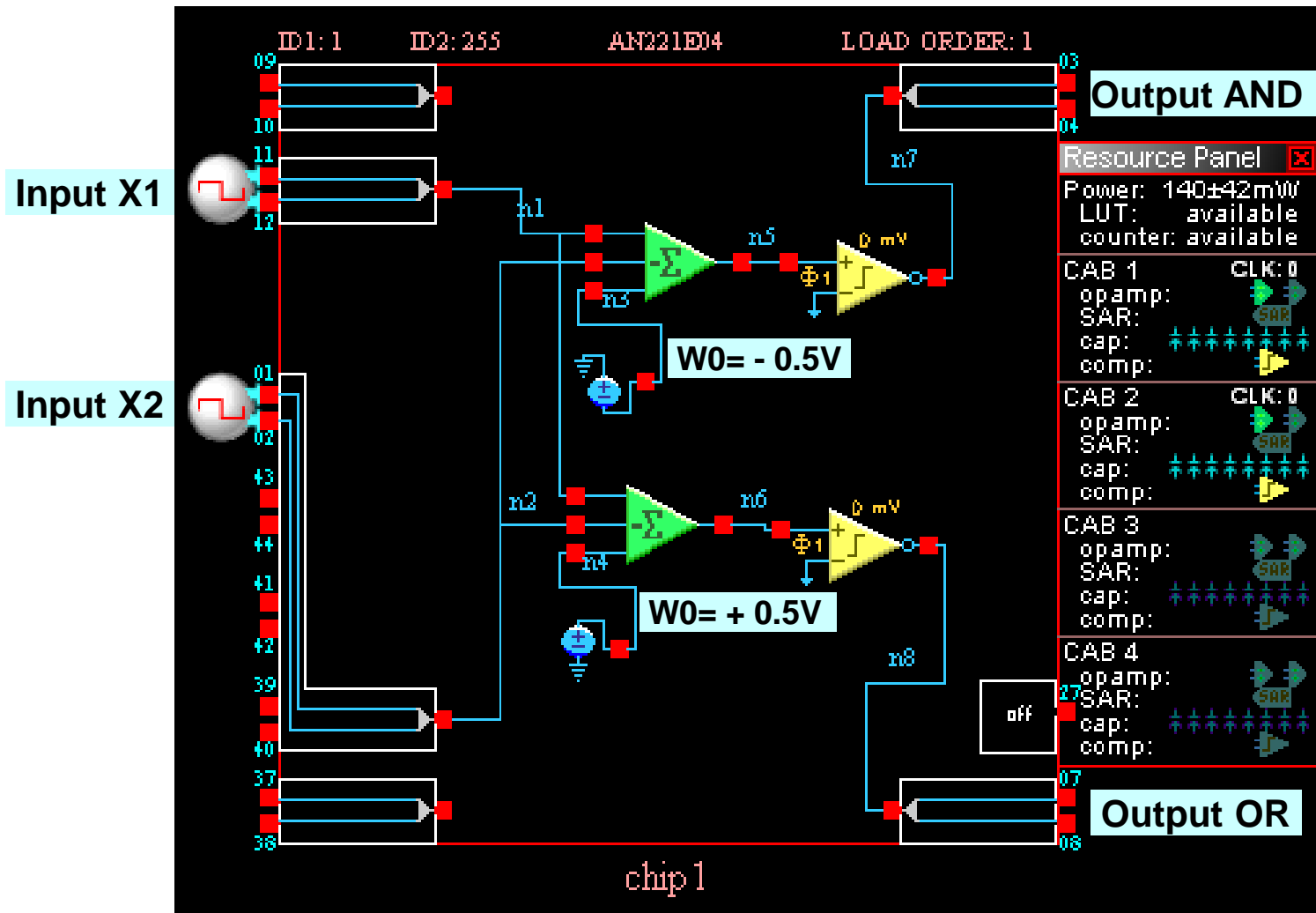
$$F(+0.5, 1, 1) = X_1 \vee X_2$$

$$SUM = +0.5 + X_1 + X_2$$

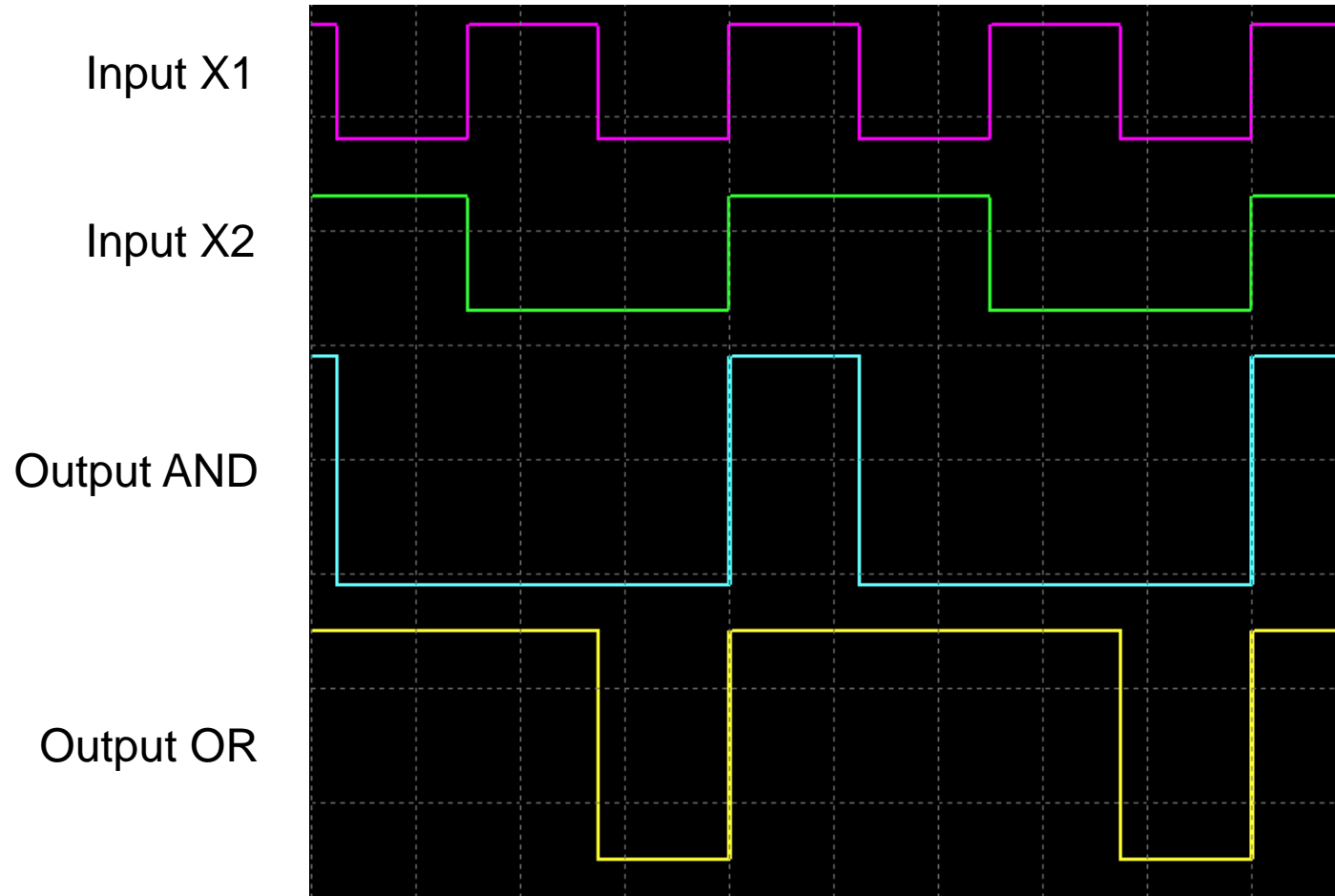
X1	X1,V	X2	X2,V	SUM,V	Y
0	-1	0	-1	-1.5	0
0	-1	0	1	0.5	1
1	1	0	-1	0.5	1
1	1	1	1	2.5	1



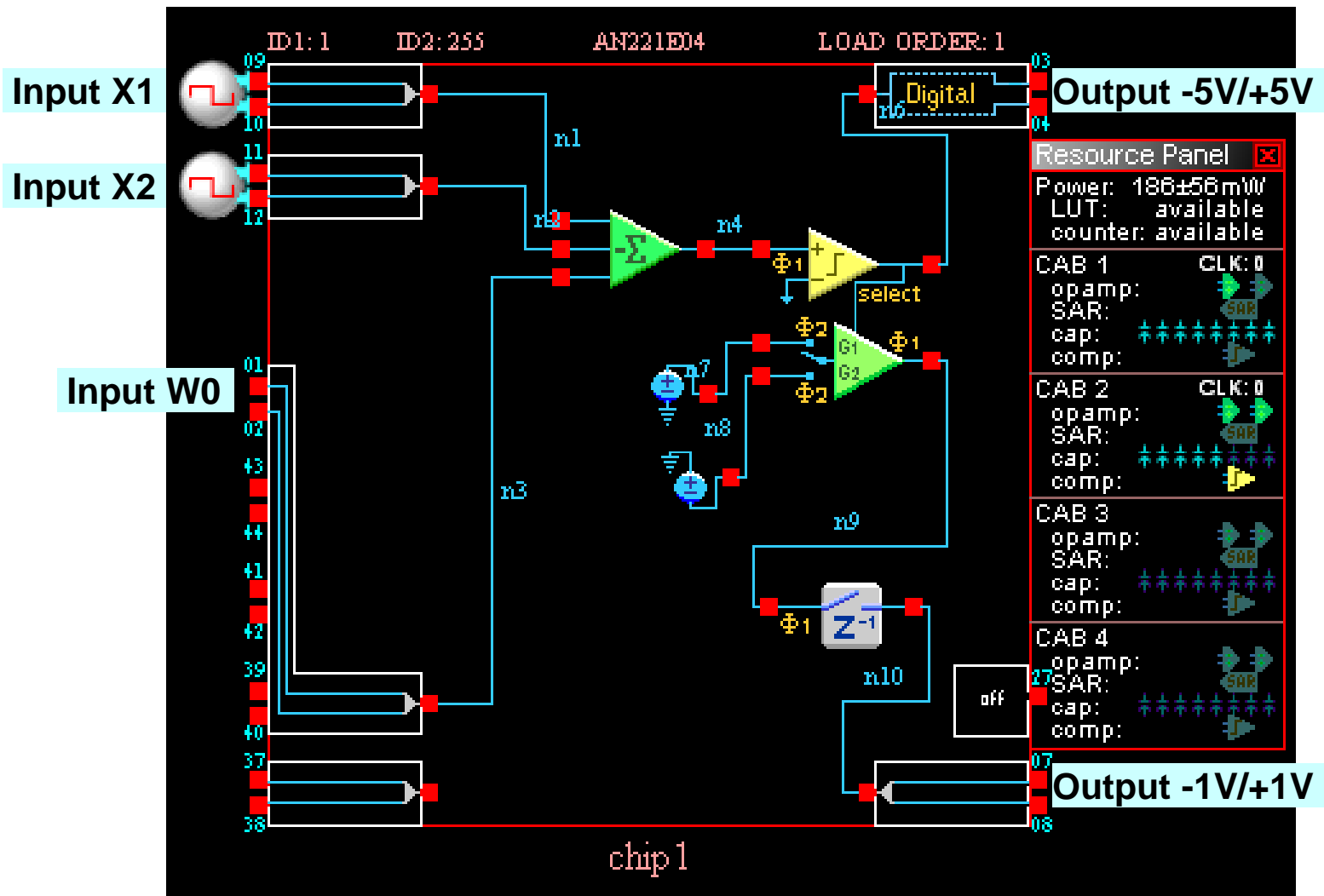
# FPAA Applications - Threshold Logic



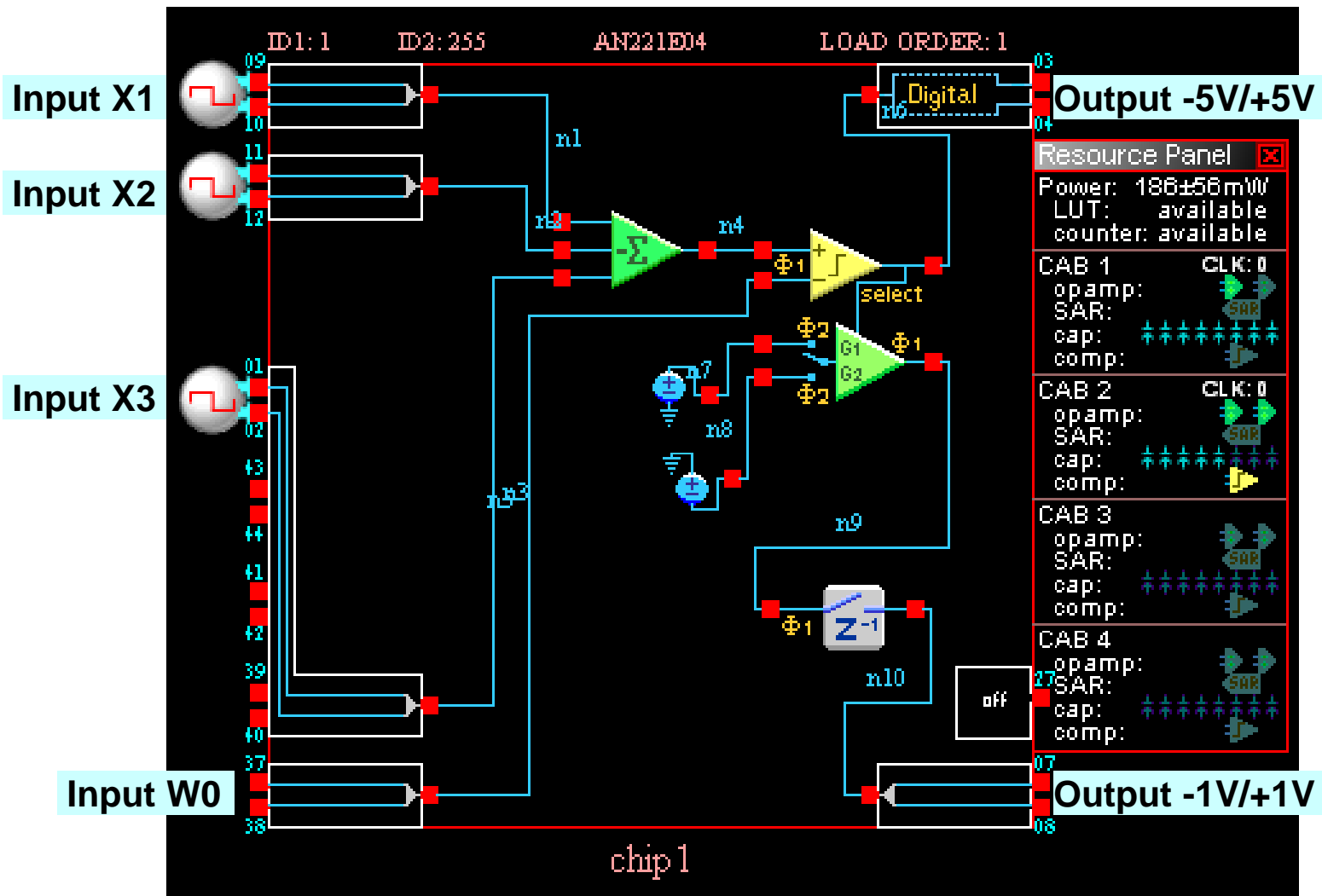
# FPAA Applications - Threshold Logic



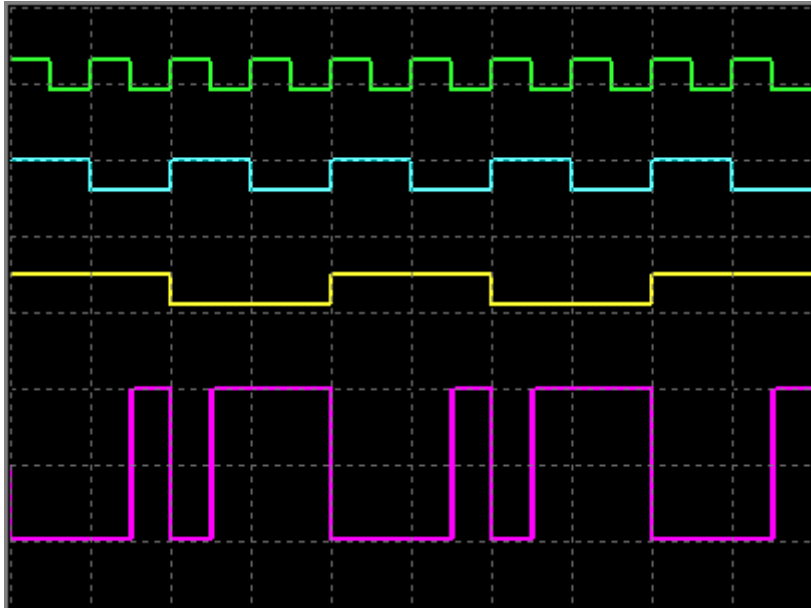
# FPAA Applications - Threshold Logic



# FPAA Applications - Threshold Logic

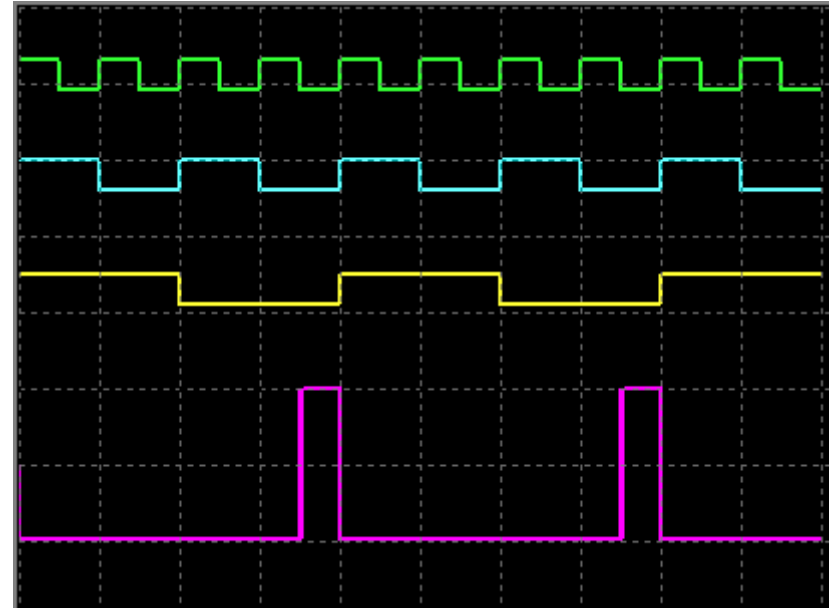


# FPAA Applications - Threshold Logic



$F(1,1,1)$

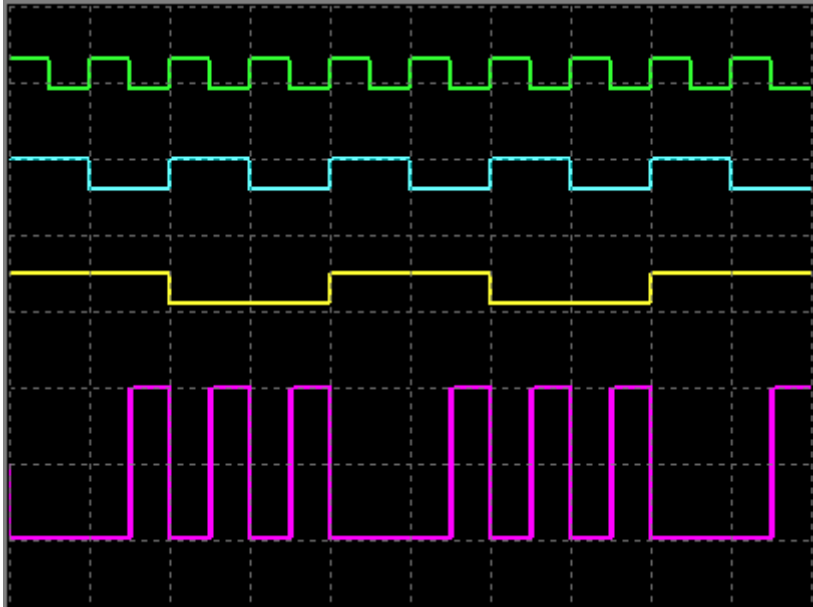
$$F = \bar{X}_1 \cdot \bar{X}_2 \vee \bar{X}_2 \cdot \bar{X}_3 \vee \bar{X}_1 \cdot \bar{X}_3$$



$F(-2,1,1)$

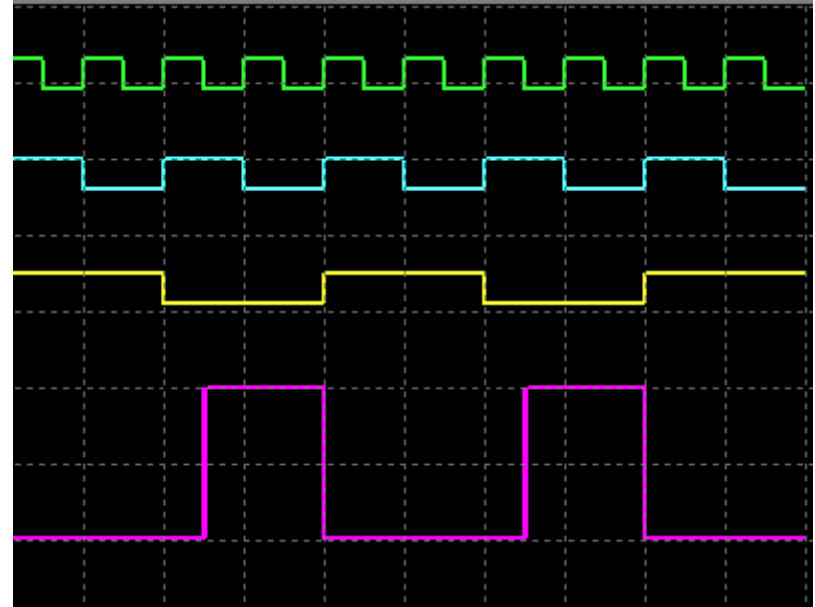
$$F = \bar{X}_1 \cdot \bar{X}_2 \cdot \bar{X}_3$$

# FPAA Applications - Threshold Logic



$$F(-2,2,1,1)$$

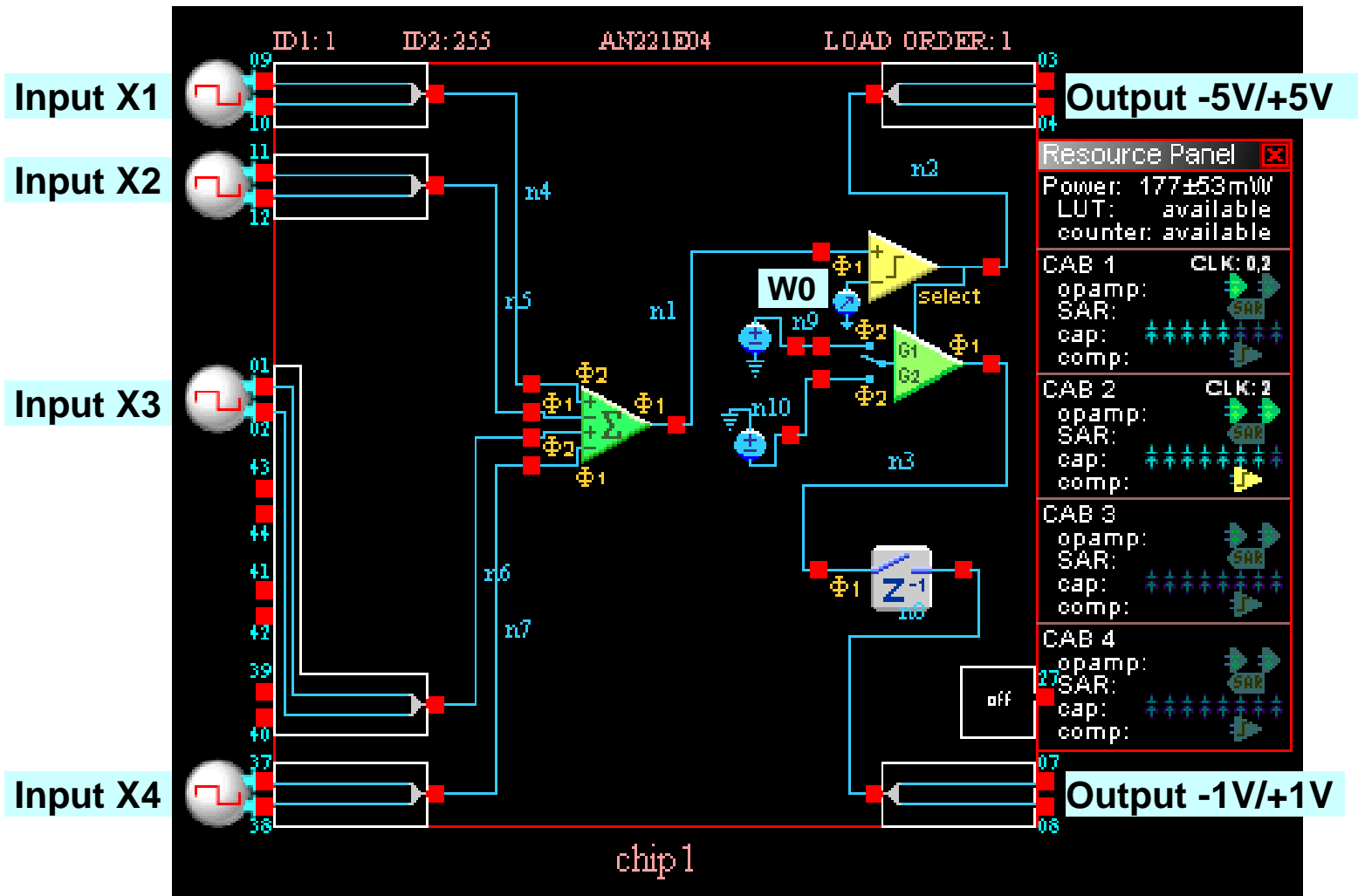
$$F = \bar{X}_1 \cdot \bar{X}_2 \vee \bar{X}_1 \cdot \bar{X}_3$$



$$F(-1,1,2,1)$$

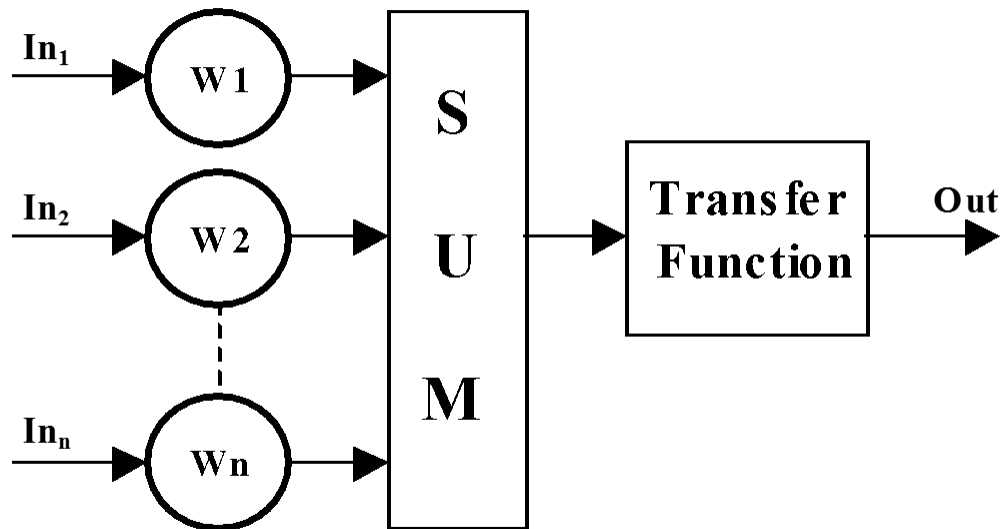
$$F = \bar{X}_2 \cdot \bar{X}_3 \vee \bar{X}_1 \cdot \bar{X}_3$$

# FPAA Applications - Threshold Logic

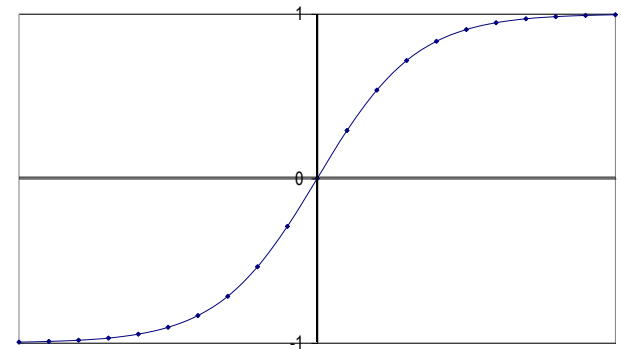


# FPAA Applications - Analog Neuron

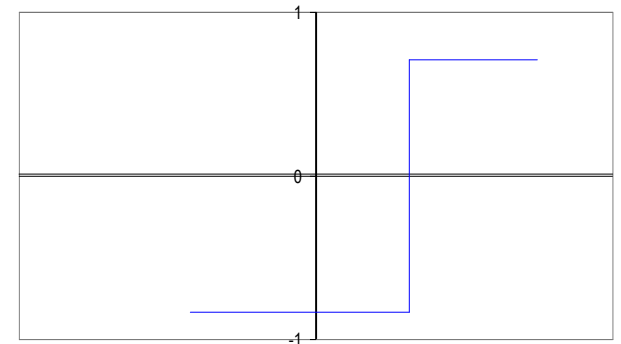
Functional model of analog neuron



Sigmoid

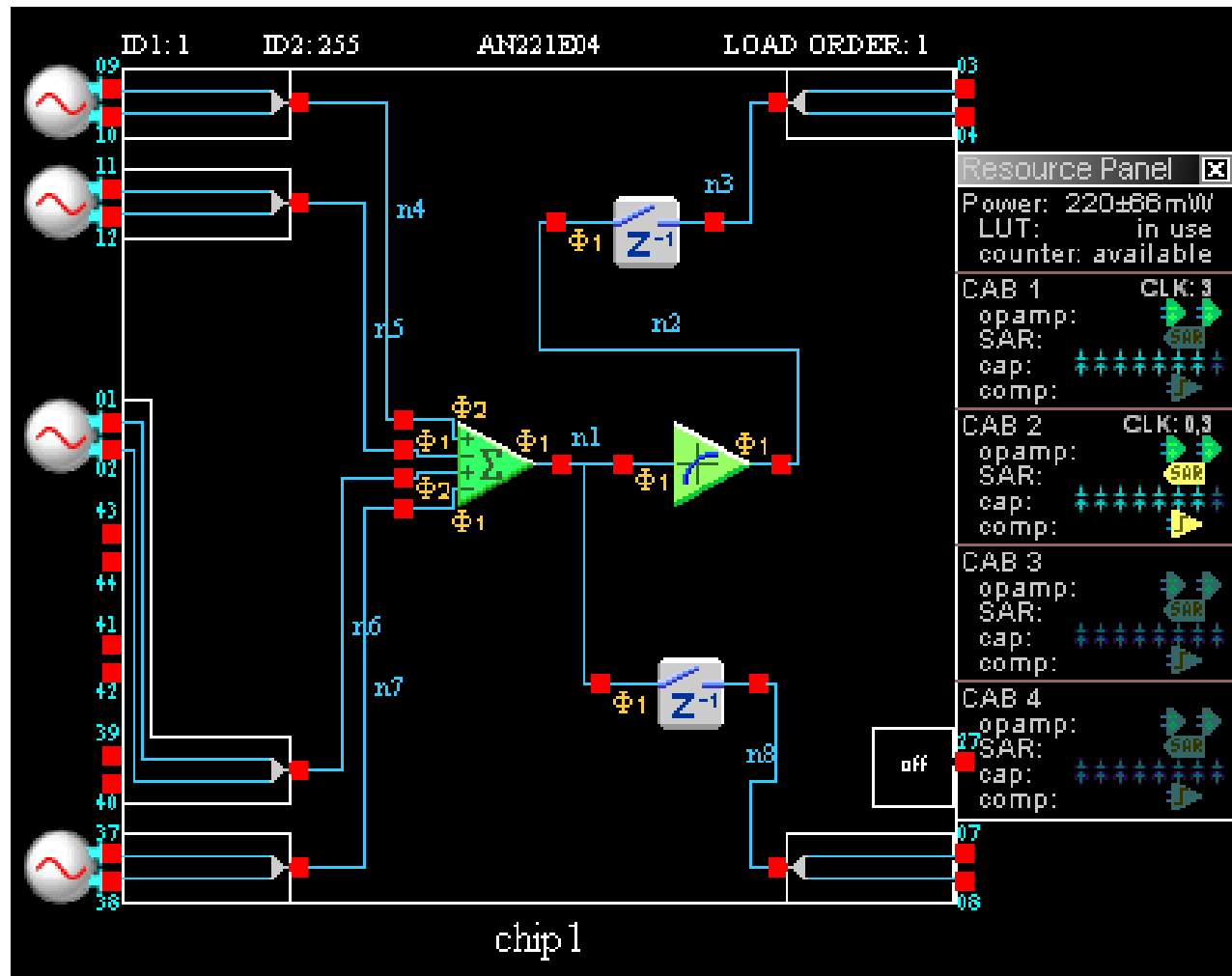


Threshold

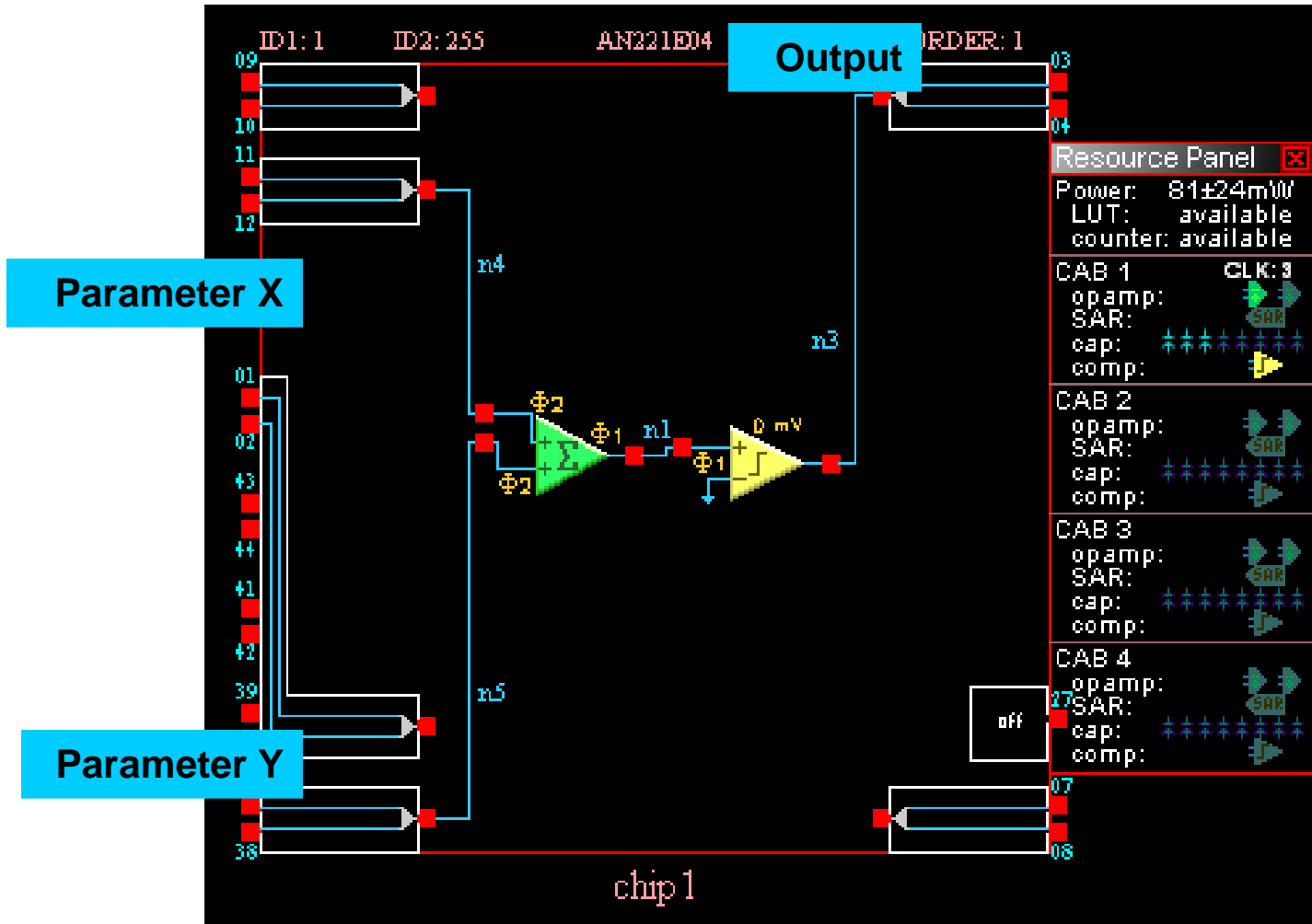




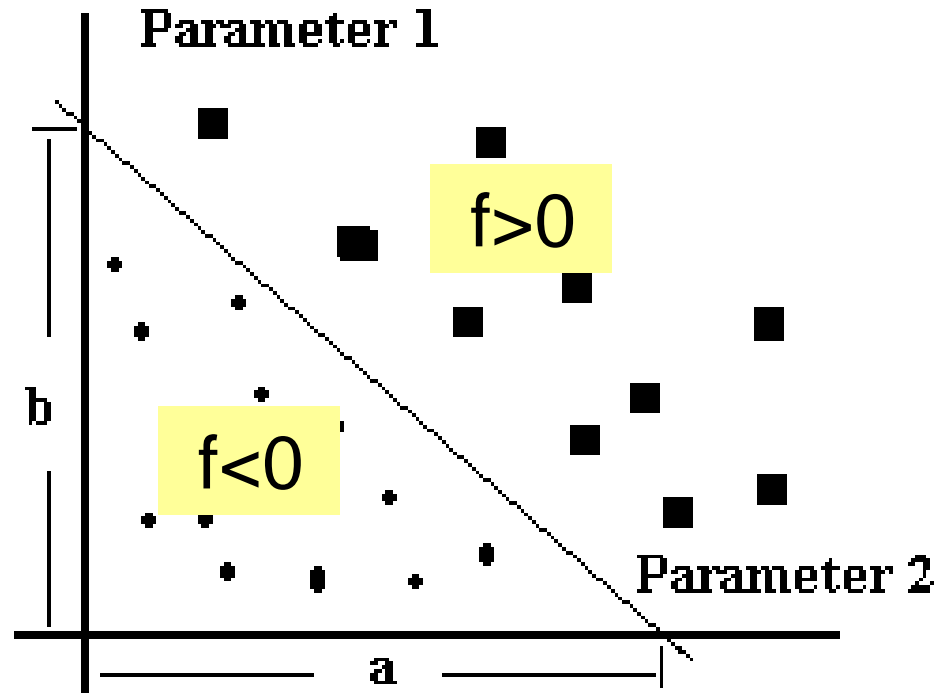
# FPAA Applications - Analog Neuron



# FPAA Applications - Analog Neuron

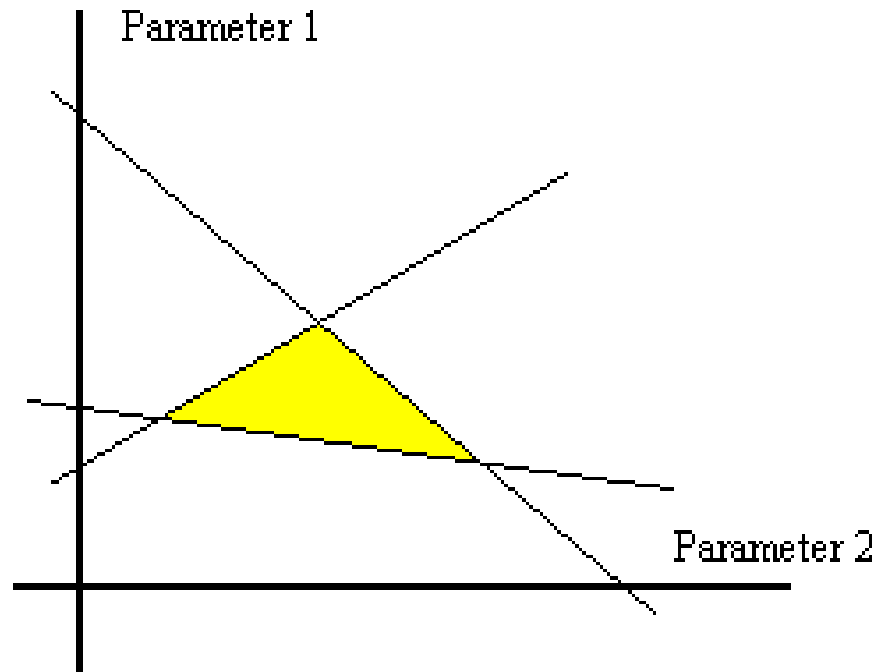


# FPAA Applications - Analog Neuron



$$f = X2 + \frac{b}{a} X1 - b$$

# FPAA Applications - Analog Neuron



The FPAA circuits, which solve more complex classification tasks, were developed by using appropriate combinations of simple artificial neurons and threshold logic circuits.

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# Conclusions

## **FPAAs design methodology:**

- **greatly simplify the design of complex analog systems by allowing to work at a higher level of abstraction in describing system functionality.** Simply by dragging and dropping CAMs, can design a complete analog system, simulate it immediately, and then download it to the FPAAs chip for testing, validation, and immediate move to production.

- **allows the using of single design to accommodate multiple design variations.** The re-configuration possibilities of the FPAAs reduce design risk and allow field updates of the project. Dynamic reconfiguration (without breaking the operation) allows for truly innovative analog system design.

**These very attractive and universal features of the FPAAs can be used and exploited in various applications in education, research and industry.**

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## Conclusions (cont.)

**Today there are many different FPAA solutions, which are developed in the areas of typical analog applications like sensor interfacing and signal conditioning, analog test and control circuits, complex filtering, etc. They can be very easily and inexpensively utilized in students' laboratories and research centers.**

**Despite of the areas of typical analog applications, the FPAAs hold out a good prospects for design, implementation and investigation of practical prototypes of digitally controlled re-configurable computational circuits and neural networks.**

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**THANK YOU !**