tion of the oscillators. In summary, the overall well-behaved performance of OTA-C oscillators for high frequencies has been demonstrated.

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Two Novel Fully Complementary Self-Biased CMOS Differential Amplifiers

Mel Bazes

Abstract—**Two novel CMOS differential amplifiers are presented. Both differ from conventional CMOS differential amplifiers in having fully complementary configurations and in being self-biased through negative feedback. The amplifiers have been applied as precision high-speed comparators in commercial VLSI CMOS integrated circuits.**

I. Introduction

THIS brief paper presents two novel CMOS differential amplifiers. The first differential amplifier is intended for applications in which the input common-mode range is relatively limited; this amplifier is denoted a complementary self-biased differential amplifier (CSDA) [1]. The second differential amplifier is intended for applications in which the input common-mode range is bounded only by the supply voltages; this amplifier is denoted a very-wide-common-mode-range differential amplifier (VCDA) [2].

The circuit configurations of both amplifiers differ from those of conventional CMOS differential-amplifier configurations in two important ways:

1) the amplifiers are completely complementary, i.e., each n-type device operates in push–pull fashion with a corresponding p-type device;
2) the amplifiers are self-biased through negative feedback.

These two differences in the amplifier configurations result in several performance enhancements:

- less sensitivity of active-region biasing to variations in processing, temperature, and supply;
- capability of supplying switching currents that are significantly greater than the quiescent bias current;
- nominal doubling of differential-mode gain (+6 dB).

These performance enhancements are particularly desirable in comparator applications in commercial digital CMOS VLSI integrated circuits, where precision, high speed, ease of interfacing to ordinary logic gates, and consistently high production yields are required. Both amplifiers have found application in commercial CMOS VLSI integrated circuits as precision comparators, as will be discussed below.

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II. CSDA

A. Theory of Operation

A self-biased, but noncomplementary, CMOS differential amplifier has been reported [3], as has a fully complementary, but externally biased, CMOS differential amplifier [4].

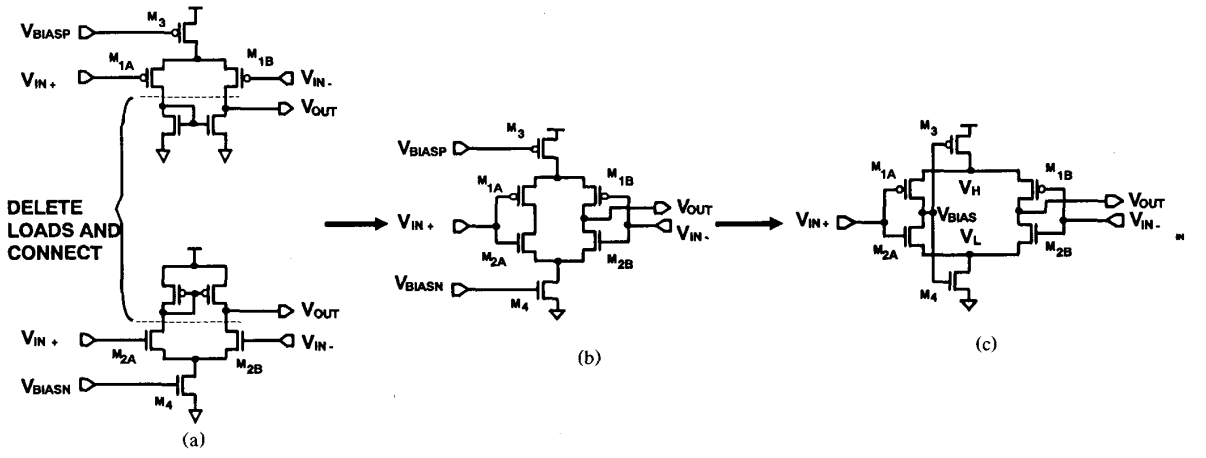


Fig. 1. Derivation of CSDA.

In contrast to these amplifiers, the CSDA incorporates both self-biasing and a fully complementary configuration.

The basic operation of the CSDA is perhaps most readily understood by following its derivation from well-known conventional CMOS amplifier configurations. Fig. 1(a) illustrates two conventional CMOS differential amplifiers, each the complement of the other. In the first step of the derivation, the loads from both amplifiers are deleted, and the input-pair drains of one amplifier are connected to the input-pair drains of the other. The resulting fully complementary, but externally biased, configuration is illustrated in Fig. 1(b).

However, the circuit of Fig. 1(b) cannot be biased in a stable fashion. In order for the circuit to be biased in a stable fashion, the currents through devices M_3 and M_4 must be identical. Any difference in currents through these two devices would result in extreme shifts in amplifier bias voltages. Achieving perfect equality of currents in these two devices using external biasing is practically impossible, so that the configuration of Fig. 1(b) is impractical.

A simple modification to the circuit of Fig. 1(b), however, results in a complete stabilization of the bias voltages. This modification is illustrated in Fig. 1(c), in which the two bias-voltage inputs are disconnected from the external sources and are instead connected to the internal amplifier node V_{BIAS}. This *self-biasing* of the amplifier creates a negative-feedback loop that stabilizes the bias voltages. Any variations in processing parameters or operating conditions that shift the bias voltages away from their nominal values result in a shift in V_{BIAS} that corrects the bias voltages through negative feedback. The circuit of Fig. 1(c) is the CSDA itself.

In the CSDA, devices M_3 and M_4 operate in the linear region. Consequently, the voltages V_H and V_L may be set very close to the supply voltages. Since these two voltages determine the output swing of the amplifier, the output swing can be very close to the difference between the two supply rails. This large output swing makes interfacing the CSDA to ordinary CMOS logic gates straightforward, since it provides a large margin for variations in the logic threshold of the gates.

Another consequence of the linear-region operation of devices M_3 and M_4 is that the CSDA can provide output switching currents that are significantly greater than its quiescent current. In contrast, conventional CMOS differential amplifiers cannot provide switching currents that exceed the quiescent current set by the current-source device, which operates in the saturation region. This capability of supplying momentarily large current pulses makes the CSDA especially suitable for high-speed comparator applications, where it is necessary to rapidly charge and discharge output capacitive loads without at the same time consuming inordinate amounts of power.

The complementary character of the CSDA affords it an approximate doubling (+6 dB) in dc differential-mode gain over that of either of the conventional amplifiers of Fig. 1(a). This conclusion may be reached qualitatively by noting that in either of the amplifiers of Fig. 1(a) there are only two amplifying devices (either devices M_{1A-B} or M_{2A-B}), while in the CSDA of Fig. 1(c) there are four amplifying devices (both M_{1A-B} and M_{2A-B}). The differential-mode gain A_d of the CSDA is given by

$$A_d \simeq \frac{g_{m1} + g_{m2}}{g_o} \tag{1}$$

where g_{m1} and g_{m2} are the transconductances of devices M_{1A-B} and M_{2A-B}, respectively, and g_o is the output conductance of the amplifier.

B. Application in an Input Buffer

The CSDA was applied for the first time in a commercial cache controller integrated circuit (Intel 82385), where it was used in the TTL-to-CMOS-level input buffers. The cache controller is manufactured on a 1.0-μm CMOS process. The input buffer configuration is illustrated in Fig. 2. The noninverting CSDA input is connected to a reference voltage source whose nominal voltage is 1.4 V, which is the midpoint of the standard TTL input-voltage range. The inverting CSDA input is connected to the external TTL input.

Circuit simulations showed that the addition of filter capacitors to the sources of device pairs M_{1A-B} and M_{2A-B}

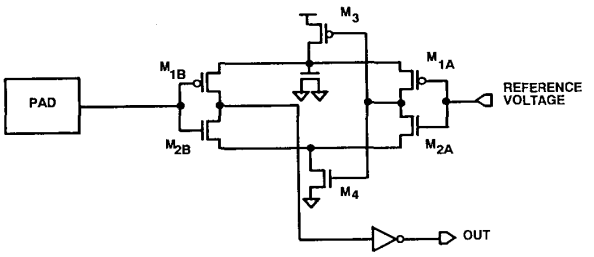
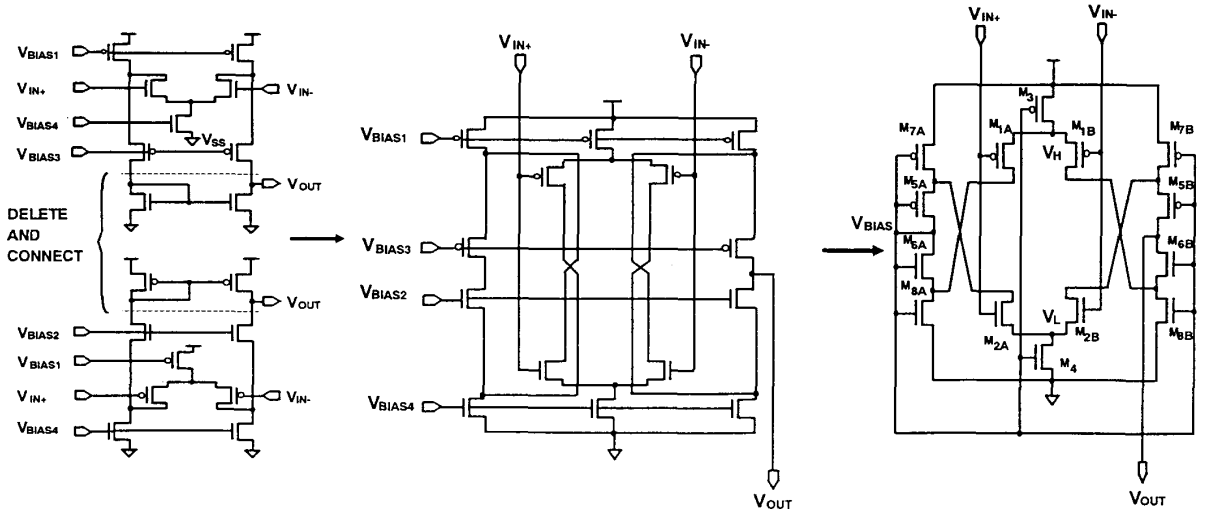


Fig. 2. CSDA application in a TTL-to-CMOS-level input buffer.



(a) (b) (c)

Fig. 3. Derivation of VCDA.

enhanced the switching speed of the CSDA in this particular application. This speed enhancement is the result of the additional charge supplied by the capacitors during switching transients. In practice, the fall time of the CSDA in this application was significantly better than the rise time, so that only a capacitor on the sources of device pair M_{1A-B} was ultimately used.

III. VCDA

A. Theory of Operation

CMOS differential amplifiers with wide input dynamic ranges have been reported [5]–[7]. All of these amplifiers are externally biased, while none of them is entirely complementary. In contrast, the VCDA is fully complementary and entirely self-biased.

As with the CSDA, the operation of the VCDA may be understood through its derivation. Fig. 3(a) illustrates two folded-cascode differential amplifiers, each the complement of the other. These amplifiers have greater dynamic ranges than ordinary differential amplifiers as a result of the larger drain–source voltage drop on the input pairs. This larger voltage drop maintains the input pairs in the active region even for very large swings of the input signal. While neither amplifier in Fig. 3(a) by itself is capable of covering the entire input range from negative supply to positive supply, a combination of the two amplifiers can cover this entire range.

In the first step of the derivation, the loads of the two amplifiers are deleted, and their outputs are connected together to produce the fully complementary, but externally biased, differential amplifier of Fig. 3(b). As in the case of the circuit in Fig. 1(b), the circuit of Fig. 3(b) cannot be biased in a stable fashion, so it is not practical.

However, just as in the case of the circuit of Fig. 1(c), by connecting all of the bias inputs to a single internal node, V_{BIAS}, the bias point of the amplifier is dramatically stabilized through negative feedback. The resulting self-biased amplifier is illustrated in Fig. 3(c), which is the VCDA itself.

The differential-mode gain of the VCDA is given by (1), just as for the CSDA.

B. Application in a Differential Input Buffer

The VCDA was applied for the first time in a commercial Ethernet serial interface integrated circuit (Intel 82C501AD). The Ethernet serial interface is manufactured on a 1.0-μm CMOS process. The VCDA was used in the implementation of a differential "squelch" input buffer having the following

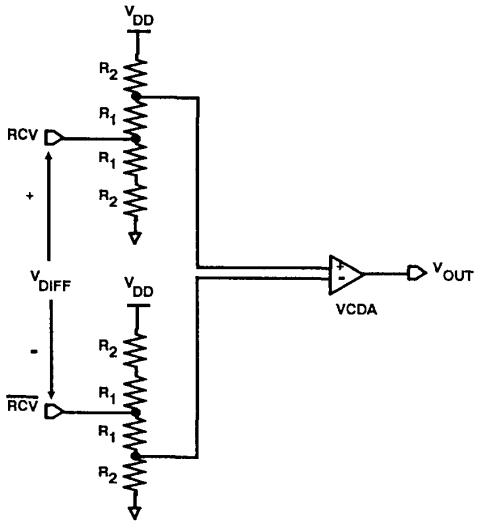


Fig. 4. Application of VCDA in a differential "squelch" input buffer.

specifications:

1) an accepted signal is any signal whose differential amplitude is more negative than -275 mV;
2) a rejected signal is any signal whose differential amplitude is more positive than -150 mV;
3) the common-mode component of the signal may vary all the way from the negative rail up to the positive rail.

The circuit diagram of the squelch input buffer implemented with the VCDA is illustrated in Fig. 4. In Fig. 4, V_{DD} is the positive supply and is nominally equal to 5.0 V. From Fig. 4, the output voltage V_{OUT} is found to be given by

$$V_{OUT} = A_d\left(\frac{1}{1+R_1/R_2}\right)\left[V_{DIFF}+(R_1/R_2)V_{DD}\right]. \quad (2)$$

V_{OUT} approaches V_{DD} if the expression in the brackets on the right-hand side of (2) is slightly positive, while V_{OUT} approaches 0 V if the expression in the brackets is slightly negative. Therefore, the buffer differential threshold voltage is just $-(R_1/R_2)V_{DD}$. The resistor ratio R_1/R_2 can be implemented with high precision and repeatability. Hence, the dominant source of variability by far in the differential threshold voltage is only V_{DD}. But even with the tolerance of V_{DD} specified at $\pm 10\%$, the buffer has a solid design margin, as demonstrated by nearly 100% production yields for the buffer threshold parameter.

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