Op-Amps and Startup Circuits for CMOS Bandgap References With Near 1-V Supply

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***Abstract*—The design of bandgap-based voltage references in digital CMOS raises several design difficulties, as the supply voltage is lower than the silicon bandgap in electron volts, i.e., 1.2 V. A current-mode architecture is used in order to address the main issues posed by the low supply, but the implementation of the operational amplifier and of dedicated startup circuits deserves some attention. Even if nonstandard devices such as depletion-mode MOS transistors may be helpful to manage the supply scaling, they are seldom available and poorly characterized. Therefore, they must be avoided in a robust design featuring a high portability. This paper proposes some circuit solutions suitable for very low-supply-voltage operation and addresses the main issues of achieving the correct bias point at the power on. A few bandgap references were implemented in digital 0.35- and 0.18-μm technologies featuring a nominal output voltage of about 500 mV and minimum supplies from 1.5 to 0.9 V.**

***Index Terms*—Bandgap-based voltage reference, CMOS integrated circuits, low-voltage design, voltage reference.**

I. Introduction

REFERENCE voltage generators with low sensitivity to the temperature and supply are commonly required both in analog and digital circuits such as DRAM or flash memories. Since the conventional implementation of the bandgap voltage reference provides an output voltage almost equal to the silicon energy gap, measured in electron volts, it cannot be used in the latest deep-submicron technologies whose supply voltage is already in the 1-V range [1]. A recently reported current-mode (CM) realization of the bandgap reference in CMOS technology has the potential of circumventing the supply-voltage limitation [2]. However, the reported implementation requires a minimum supply voltage of about 2 V, makes use of nonstandard devices (depletion-mode MOSTs), and requires an external power on-reset signal (POR) seldom available in analog and mixed-signal circuits. A CM voltage reference with sub-1-V supply in BiCMOS technology was recently reported, but the low-voltage operational amplifier (op amp) cannot be implemented in digital CMOS [3]. In this paper, the design of bandgap references with low supply voltage is discussed and some useful circuit techniques are proposed. Moreover, a few implementations with minimum supply voltages from 1.5 to 0.9 V in 0.35- and 0.18-μm CMOS technologies are presented.

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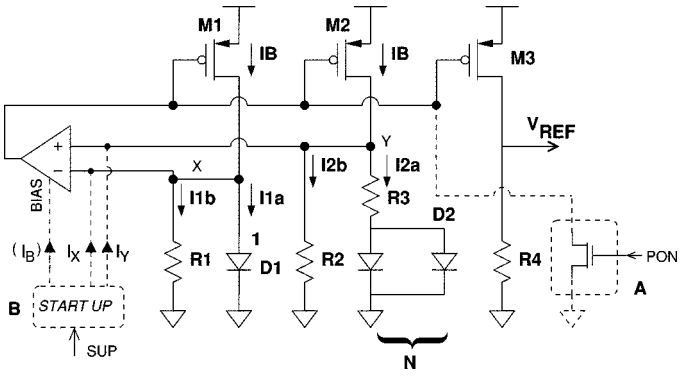

Fig. 1. Low-voltage current-mode CMOS bandgap reference. Either startup circuit A, right, or B, left, must be included for achieving the correct bias point at power on.

II. CMOS Bandgap References

In a bandgap reference, an output voltage with a low sensitivity to the temperature is obtained as the sum of a forward voltage drop on a p-n junction and a contribution proportional to absolute temperature (PTAT). By setting the output voltage V_{bg} approximately equal to the silicon bandgap measured in electron volts, it is possible to nullify its temperature sensitivity [4], [5]. In CMOS technology, substrate vertical p-n-p bipolar junction transistors (BJTs) implement the p-n junctions [6]. Since the output voltage is about 1.2 V, this architecture cannot be used with the latest CMOS technologies, where the supply voltage ranges from 1.8 (0.18 μm) to 1.2 V (0.13 μm), and is expected to drop to 0.9 V with the next technology scaling [1]. Use of nonstandard devices instead of p-n diodes might help to cope with the reduced supply voltage [7], [8], but at the cost of low reproducibility, poor portability of the design, and the need for accurate models of nonstandard devices. On the contrary, by means of resistive division, a reference voltage of about 0.7 V with sub-1-V supply has been demonstrated [9]. However, this technique is not suitable for high-precision reference working in a large temperature range, since the lowering of the output voltage obtained through resistive division greatly increases the curvature error. In the low-voltage CM bandgap reference of Fig. 1, the voltages at X and Y nodes are kept equal by the op amp, and since $R1 = R2$, $I1b = I2b$. Since the currents in $M1$ and $M2$ are also equal, $I1a = I2a$, and the voltage drop on $R3$ is $(kT/q)\ln(N)$. The current in $M2$ is, therefore, $I_{\rm B} = (1/R3)(kT/q)\ln(N) + V_{D1}/R2$, where $V_{D1} \equiv V_X$ is the voltage drop on $D1$. The first contribution is PTAT, while the second decreases with the temperature: by choosing N, $R2$, $R3$ so that $dI_{\rm B}/dT \approx 0$ and mirroring $I_{\rm B}$ by means of $M3$, an arbitrary $V_{\rm REF}$ with a very low temperature sensitivity can be obtained as the voltage drop on low-temperature coefficient resistor $R4$.

III. Bandgap References for Very Low Supply Voltage

The implementation of the CM bandgap reference reported in [2] exhibits some relevant limitations. The minimum supply voltage is about 2 V, well above the supply voltage supported by the latest CMOS generations. Moreover, the seldom-available depletion-mode MOST was used in the op amp, while a design aiming at easy portability should rely on standard CMOS devices only. Finally, a correct startup at power on was achieved by means of an external POR signal, which may be unavailable in analog and mixed-signal designs.

From inspection of the CM circuit in Fig. 1 the minimum theoretical supply voltage that can be supported is $V_{d1} + V_{\mathrm{dssat}-M1}$, $V_{\mathrm{dssat}-M1}$ being the saturation voltage of $M1$. Considering $V_{d1} \approx 0.65$ V and $V_{\mathrm{dssat}-M1} \approx 0.1$ V, a supply voltage as low as 0.75 V can be achieved in principle. However, achieving a sufficient gain of the op amp and an adequate stability margin is difficult at such a low supply voltage.

A. Design of the Op Amp

The common-mode input voltage of the op amp in Fig. 1 is $V_X \approx 0.65$ V, independent of the supply voltage, being imposed by the voltage drop across diode $D1$. Neglecting solutions involving switching devices for an easier and less noisy implementation, the input stage of the op amp may be either a pMOS or an nMOS differential pair. Three possible solutions are given in Fig. 2. All the op amps include an *R–C* compensation network for achieving a sufficient stability margin. In each configuration, the bias current may be derived either from the bandgap reference itself (dashed lines) or from the raw supply through the V_b pin. The former solution is usually preferred, providing a lower sensitivity to the supply voltage, but it leads to a very small voltage gain in the undesired bias point, i.e., when no current flows in the bandgap core. Furthermore, the input transistors should be designed with a large gate area and nonminimum gate length in order to keep offset low. Indeed, the spread of the reference voltages at wafer level is mainly contributed by the op-amp offset voltage, while a minor contribution arises from the pMOS current mirrors and the substrate p-n-ps.

In order to compare benefits and drawbacks of the reported arrangements, let us consider a digital 0.35-μm technology with typical thresholds (V_{T}) of 0.5-V nMOS and 0.6-V pMOS transistors. Note that these values do not change significantly in the latest digital CMOS technologies. In the pMOS solution, Fig. 2(a), a supply voltage lower than 1.5 V pushes the tail-current generator $M0$ in triode region and, consequently, causes a decrease of the bias current I_{T} and a degradation of the common-mode rejection ratio (CMRR). At 1.2-V supply, the input devices enter in weak inversion mode and the V_{ds} voltage of $M0$ is a few tens of millivolts. Below 1.2-V supply, I_{T} decreases abruptly and the op amp cannot provide enough loop gain and CMRR to keep the bandgap at the correct bias point.

The nMOS differential pair with pMOS followers, Fig. 2(b), allows the input common-mode voltage to be as low as 0 V, thus simplifying the design of the startup circuit. Moreover, the bias current I_{T} is almost independent of the supply voltage,

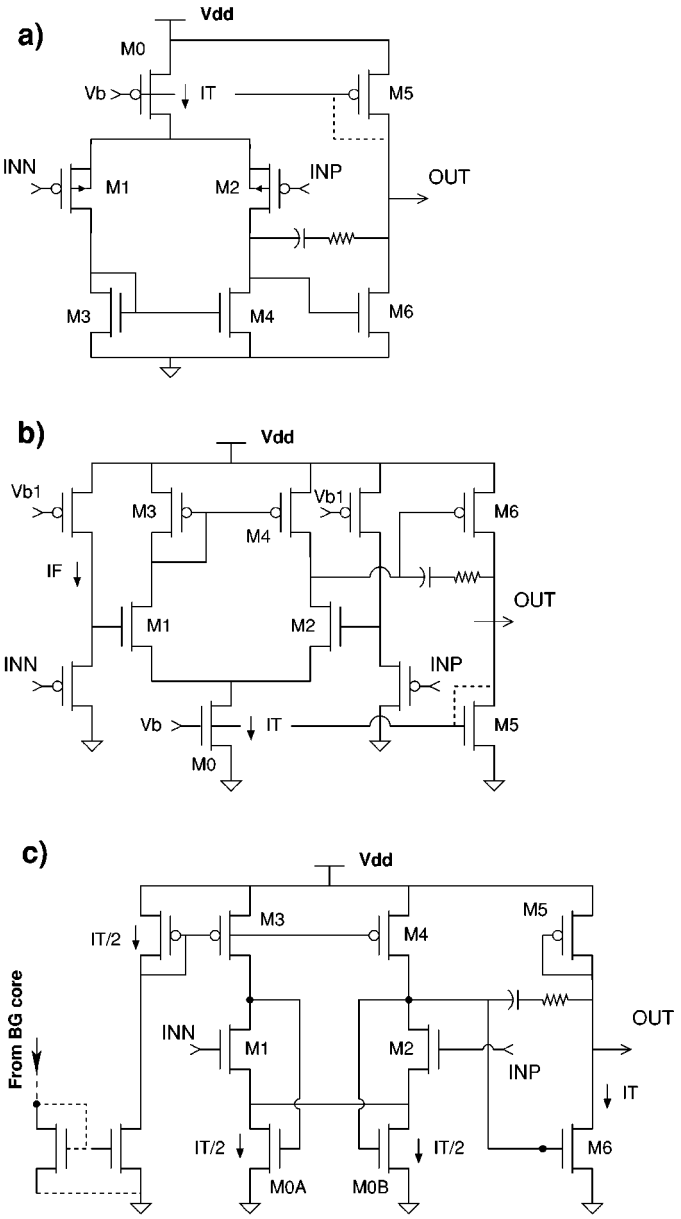

Fig. 2. Low-voltage op amps for the CM bandgap. The bias current may be derived either from the bandgap core (dashed lines) or from the raw supply through the V_b pin.

leading to a higher supply rejection. Nevertheless, due to the level shifting, the minimum tolerated supply is about 1.5 V and a higher offset voltage is expected.

The op amp in Fig. 2(c) is an evolution of the nMOS arrangement aiming at the reduction of the minimum supply voltage below 1 V. Indeed, the pMOS level shifters have been removed and the nMOS input devices are biased in weak inversion with a gate voltage equal to V_X, i.e., 0.65 V. The pMOS current mirror in the load of the input stage is replaced by a symmetric active load driven by a common-mode feedback control. Due to the very low supply voltage, common-mode feedback cannot be implemented with a differential stage, but it can be achieved by splitting the tail-current generator into two identical transistors, $M0A$ and $M0B$, whose gate voltages are controlled by the outputs of the differential stage. The higher the output

TABLE I
CIRCUIT PARAMETERS OF LOW-VOLTAGE OP AMPS IN FIG. 2

	a	b	c
M1-2	500/1	200/5	500/1
M3-4	100/1	100/10	500/0.5
M5	100/1	50/5	250/2
M6	100/4	30/5	100/1
I_T	5 μA	1.4 μA	10 μA
I_F		3 μA	

common-mode voltage, the higher the tail current. This feedback control fixes the voltage at the drain of $M1$ and $M2$ at about $V_{\rm Tn}$, $M0A$ and $M0B$ being biased in weak inversion. However, it should be remarked that any difference between the desired common-mode voltage at the outputs of the differential stage and the measured common-mode voltage, represented by the V_{gs} voltage of $M6$, leads to a systematic offset voltage. This is easily avoided if the drain current of $M6$ is set to $I_{\rm T}$, i.e., equal to the tail current of the differential stage. The minimum supply voltage is determined by the load transistors $M3$ and $M4$ and by the pMOS current mirrors in the bandgap core which enter in triode region. Simulations show an open-loop gain higher than 60 dB at 27 °C down to 0.75-V supply. Aspect ratios and bias currents for the op amps in Fig. 2 are reported in Table I.

B. Startup Issues and Countermeasures

The startup of the CM bandgap of Fig. 1 involves several issues since it exhibits an operating point with no current flowing in the bandgap core and $V_X = V_Y = 0$. This point may be stable if the op amp does not provide enough gain, as a consequence of a bias current derived from the bandgap core or a limited input common-mode range. Moreover, startup may fail because of the op-amp offset voltage, pushing the bias point in the wrong direction. The perturbation caused by the startup circuit in the bandgap core must either be removed as the circuit settles at the correct bias point or have a minimal impact on the behavior of the reference circuit. Known solutions for conventional bandgap circuits cannot be used here, since the output reference voltage is even lower than a diode voltage drop.

Two alternative startup strategies are reported at either sides of the CM bandgap of Fig. 1. The solution at the right is based on a switch driven by a POR signal and temporarily closed at power on, thus forcing the op-amp output at the low potential and causing some current to flow in the arms of the bandgap core [2].

The alternative strategy, shown on the left side of Fig. 1, is expanded in Fig. 3. Three controlled-current generators inject some current at nodes X and Y of the bandgap core and also provide some bias current $I_{\rm B}$ to the op amp. Note that $I_{\rm B}$ is not required if the op-amp bias is derived from the supply. I_X must be larger than I_Y in order to drive the circuit toward the correct bias point and to override any offset voltage of the op amp. Three possible ways of driving the pMOS devices are illustrated in the right side of Fig. 3. The first resorts to a POR signal. The second is the least complex, since it makes use of a constant

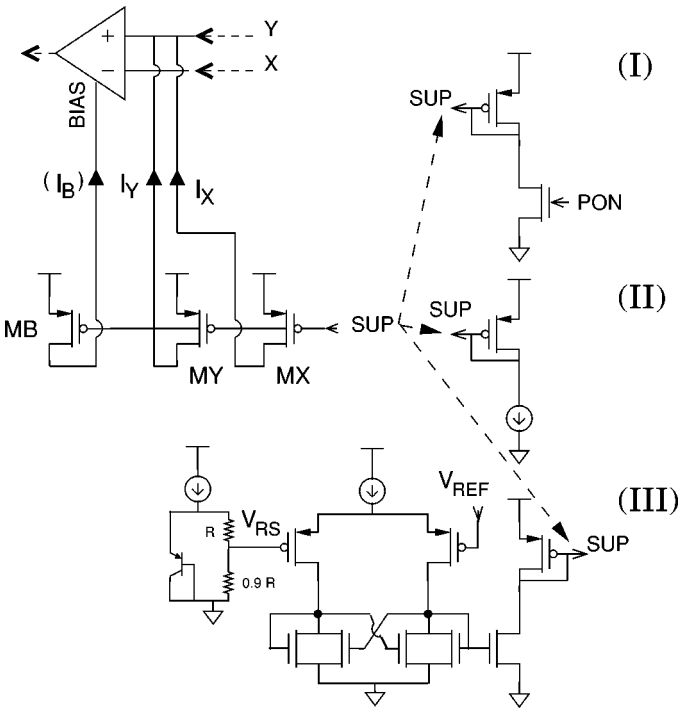

Fig. 3. Proposed strategy for achieving the correct bias point at the power on. Transistors MX, MY, and MB must be driven by one of the three circuits at the right. Circuit (I) requires a POR. Circuit (II) does not require any external signal and forces a constant current into the bandgap core. Circuit (III) does not require any external signal, but is able to remove the injected current as soon as the correct bias point is established.

current derived from the raw supply, without requiring any POR signal. Here, the perturbing currents, I_X and I_Y, should be as low as possible in order to minimize the perturbation on the bandgap circuit at regime, but be effective in moving the bias point of the circuit away from the wrong bias point. To this aim, the op amp must provide enough gain at the wrong bias point and only the one in Fig. 2(b) proves to be adequate. The last solution, proposed in Fig. 3 at the bottom, avoids both the POR signal and the perturbation on the bandgap reference. Here, a comparator compares the output reference voltage $V_{\rm REF}$ with a rough reference developed from a diode by means of a resistive divider ($V_{\rm RS} \approx V_{\rm REF}/2$), and the startup current is supplied as long as the output voltage is smaller than $V_{\rm RS}$. It is important that the op amp provides enough gain for overriding the second feedback loop provided by the startup comparator. Otherwise, oscillatory behavior or settling at a wrong stable bias point may occur.

IV. EXPERIMENTAL RESULTS

Combining the op amps reported in Fig. 2 and the startup circuits in Fig. 3 with the basic CM bandgap core, three reference circuits were designed with $N = 19$ (diode ratio) and 10 μA of bias current. The first one (BG-A) uses the pMOS op amp [Fig. 2(a)] and the startup circuit with an external PON signal [circuit (I) in Fig. 3], the second (BG-B) uses the nMOS op amp with input followers [Fig. 2(b)] in conjunction with the simplest startup [circuit (II) in Fig. 3]. Both bandgap references were implemented in a digital 0.35-μm technology and BG-B also in

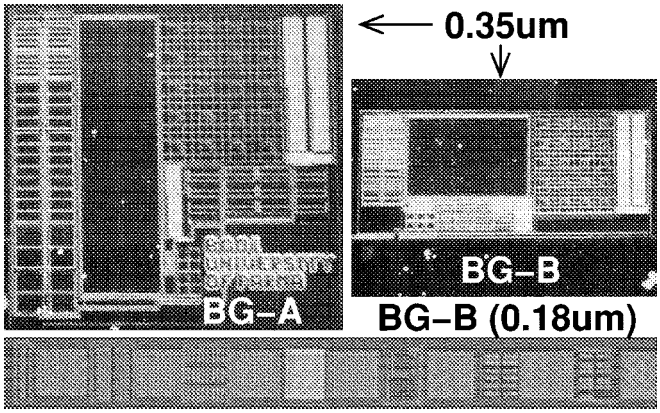

Fig. 4. Chip photographs of the BG-A, BG-B (0.35 μm technology), and BG-B (0.18 μm technology).

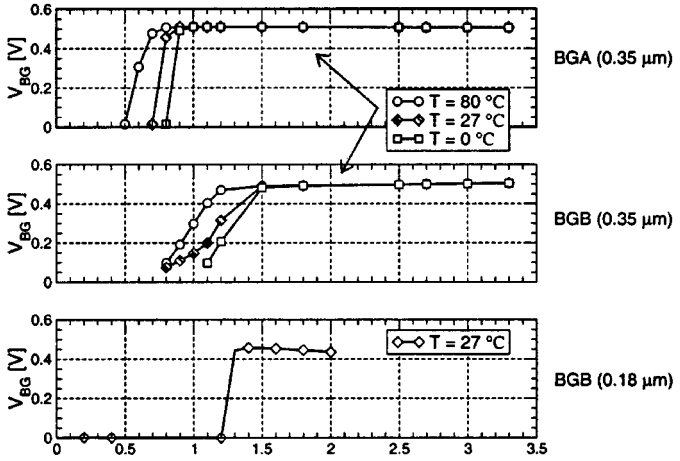

Fig. 5. Measured $V_{\rm REF}$ at different supply voltages and temperatures for BG-A, BG-B (0.35 μm implementation) and BG-B (0.18 μm implementation).

0.18 μm (see Fig. 4). $V_{\rm REF}$ was set by design at about 500 mV; the measured $V_{\rm REF}$ at different supply voltages and over a large temperature range ($-40\,^{\circ}\mathrm{C} \div 140\,^{\circ}\mathrm{C}$) is reported in Figs. 5 and 6. The measurements demonstrate a minimum supply voltage of about 1 and 1.5 V for the BG-A and BG-B implementations, respectively. The measured supply sensitivity is 2 mV/V with a supply ranging from 2.5 to 1 V, and 6.5 mV/V with a supply ranging from 2.7 to 1.5 V, for BG-A and BG-B, respectively. Fig. 7 shows the distribution of the $V_{\rm REF}$ of BG-B (0.35-μm implementation) voltage over 16 samples and at different supplies and temperatures, highlighting a 4 σ value lower than 4%. Regarding the 0.18-μm implementation, measurements over more than 1000 samples show a standard deviation of about 3.5 mV at 27 °C. Furthermore, a reference for sub-1-V supply (BG-C) was designed in the 0.35-μm technology, using the nMOS op amp with fully differential active load [Fig. 2(c)] and the startup circuit (III) in Fig. 3. The simulated reference voltages at 27 °C are reported in Fig. 8, top graph, together with their correspondent supply sensitivities. Taking into account the tolerances affecting the devices and a temperature range extending down to 0 °C, BG-C exhibits a minimum supply as low as 0.85 V.

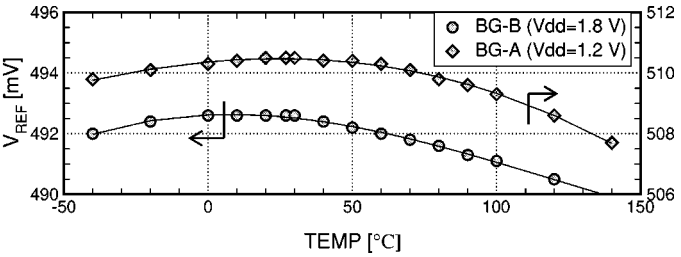

Fig. 6. From top to bottom, measured $V_{\rm REF}$ over the $-40 \div 140$ °C temperature range for the BG-A and BG-B (0.35 μm implementation) respectively.

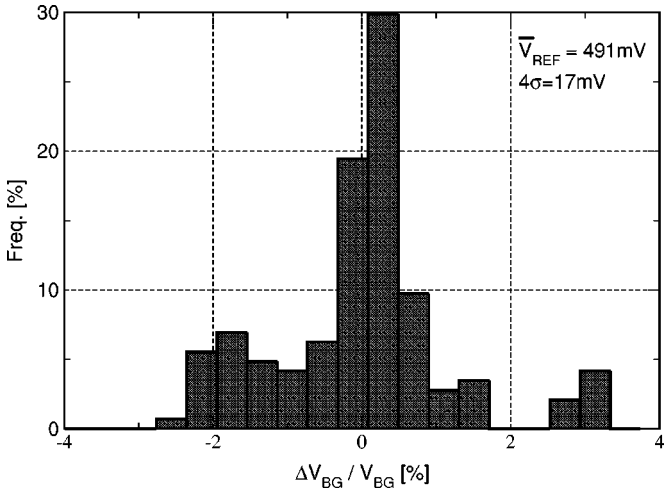

Fig. 7. Measured distribution of $V_{\rm REF}$ of 0.35-μm BG-B over 16 samples at different supplies (1.8 and 2 V) and temperatures (0 °C, 27 °C, 85 °C, 125 °C).

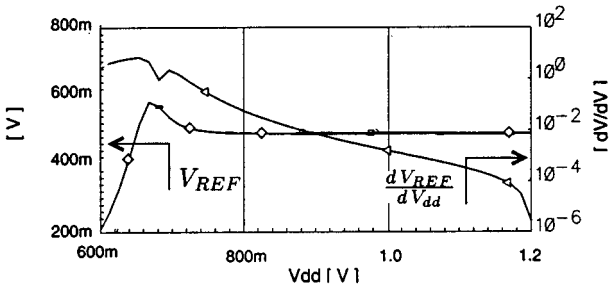

Fig. 8. Simulated reference voltage $V_{\rm REF}$ provided by the CM bandgap using the op amp of Fig. 2(c) (diamonds), together with its supply sensitivity (triangles) as functions of the supply voltage.

The simulated output noise at 100 kHz, 27 °C, is 230 nV/$\sqrt{\rm Hz}$ for BG-A (1.2 V), 205 nV/$\sqrt{\rm Hz}$ for BG-B (1.5 V, 0.35 μm), and 170 nV/$\sqrt{\rm Hz}$ for BC-C (0.9 V).

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