High Speed and High Resolution Self Biased Differential Amplifier based Latch Comparator

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ABSTRACT

In high speed ADC, comparator influences the overall performance of ADC directly. This paper describes a very high speed and high resolution preamplifier comparator. The comparator use a self biased differential amp to increase the output current sinking and sourcing capability. The threshold and width of the new comparator can be reduced to the millivolt (mV) range, the resolution and the dynamic characteristics are good. Based on UMC 0.18um CMOS process model, simulated results show the comparator can work under a 25dB gain, 55MHz speed and 210.10µW power .

Keywords

High speed ADC, high speed comparator, high resolution and preamplifier latch comparator.

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1. INTRODUCTION

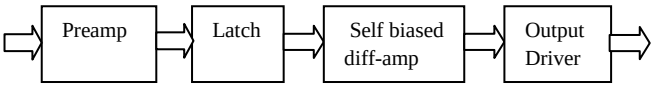
High speed ADC is essential part of modern data communication receivers and hard disk drive read channels [6], [7]. Recently several high-speed, high-resolution CMOS pipelined A/D converters with the operational frequency up to MHz have been reported [4], [5]. ADCs are widely used in many applications including data storage systems, fast serial links and high-speed measurement instruments. The preamplifier latch comparator [1], [2], combines the application of both comparators, to enhance the performance of A/D converter.

In this paper, architecture for a high-speed comparator is presented. In high speed analog-to-digital converters, the performance of comparator especially speed and resolution has a crucial influence on the overall performance that can be achieved by using preamplifier, latch stage and a self-biased differential amplifier. The comparator senses the charge imbalance produced by the input at the preamplifier and reacts to that imbalance to create desired digital voltage levels at the output.

2. STRUCTURE AND OPERATION OF CIRCUIT

A. Preamplifier

The pre-amplifier used in this design is a simple common source differential amplifier with PMOS transistors as active loads. Pre-amplifier is followed by a small circuit which is basically used for two main functions. First is the amplified weak signal to desired level and second it passes to the input of the latch comparator because latch comparator have minimum propagation delay at high input. There are several types of comparator which can provide the high speed, such as CMOS comparator, the conventional three stage comparator, regenerative latch comparator and preamplifier latch comparator. Open loop comparator can obtain high speed by cascading several stages. Speed is limited by the bandwidth of amplifier. Dynamic latch comparator has high speed but poor resolution because of higher offset.



Block Diagram of pre-amp Latch Comparator

Vin (+) and Vin (-) are the two input signals for the pre-amplifier. The change in these two signals is amplified by the per-amplifier. From the pre-amplifier, the amplified voltage difference is transferred to the input of the latch part.

Fig1 shows the small signal model for the calculation of the gain of the preamplifier.

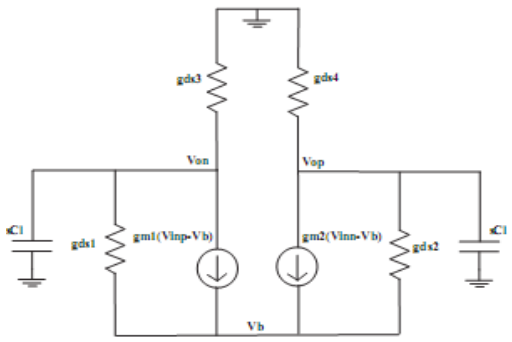


Figure 1. Small signal model for pre-amplifier

Applying KVL and calculated gain of preamplifer

At Von:

$$(Von)g_{ds3} + (Von - Vb)g_{ds1} + (Vinp - Vb)g_{m1} + (Von)(scl) = 0$$

At Vop:

$$(Vop)g_{ds4} + (Vop - Vb)g_{ds2} + (Vinp - Vb)g_{m2} + (Vop)(scl) = 0$$

At Vb:

$$(\text{Von - Vb})g_{ds1} + (Vop - Vb)g_{ds2} + (Vinp - Vb)g_{m1} + (Vinn - Vb)g_{m2} = 0$$

(Assuming $g_{ds1} = g_{ds2}$ and $g_{m1} = g_{m2}$)

$$A_v = \frac{g_{m1}}{g_{ds1} + g_{ds3} + sCl}$$

The DC gain can be written as:

$$A_v = \frac{g_{m1}}{g_{ds1} + g_{ds3}}$$

B. Regenerative Latch

Dynamic latch is composed of two inverters connected in a closed loop. Fig2 presents the dynamic latch circuit schematic.

It works as follows: when *Vout+* increases (*Vout* decreases), transistor *M2* will increase the current drawn from the *Vout-* node, decreasing its voltage. Consequently, the transistor *M1* will reduce the gate to source voltage, *Vgs*. Thus decreasing the current through *M1*, causes the voltage at node *Vout+* to increase. The PMOS transistors have the same function as the NMOS transistors.

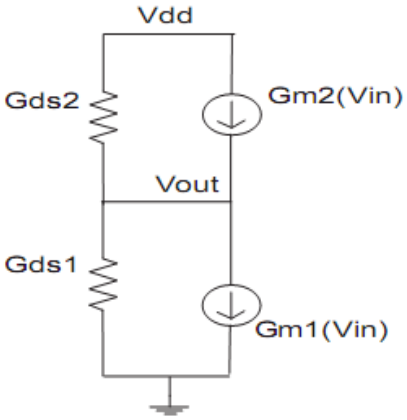


Figure 2. NMOS latch and small signal analysis

From above Fig2 calculated gain of latch comparator
At Vout:

$$-\text{Vout}(g_{ds1}) = \text{vout}(g_{ds2} + sCl) + \text{Vin}(g_{m1} + g_{m2}) = 0$$

$$A_v = \frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2} + sCl}$$

DC gain can be written as:

$$A_v = \frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2}}$$

First pole of the latch can be derived as:

$$A_v = \frac{A_0}{1 + s/p_1}$$

By substituting the values we get:

$$p_1 = \frac{g_{ds1} + g_{ds2}}{Cl}$$

C. Self-biased differential amplifier

Self-biased differential amplifier circuit is used for comparators to increase the output current sinking and sourcing capability of the comparators.
This amplifier consists of two differential amplifier connected back to back and each serving as the load for the other. The tail current of the differential amplifier become adaptive by connecting the gates of M5 and M6 to the drains of M1 and M3 from Fig3.

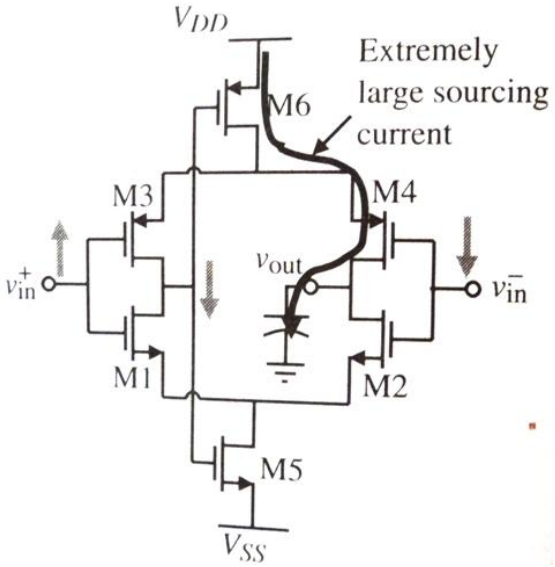


Figure 3. Self-biased differential amplifier

When the positive input voltage , V_{in}^+, is increased, drains of M1 and M3 fall and turn on M6 to a larger current, which sourced to the output capacitance connected to the drains of M2 and M4 through M4. During this condition, the current in M5 is zero. When V_{in}^+ is decreased, M5 turn on and a larger current is sunk through the output capacitance via M5. Thus, this circuit has ability to source and sink large currents without a large quiescent current.

D. Output Driver

The comparator has large capacitive load. The chances are that its slew rate is limited. By connecting output driver at output the minimum loading effect will occur. If the (W/L) increases by factor of 2.72, the minimum propagation time is achieved.

3. DESIGN AND OPTMIZATION OF CIRCUIT

A. Improve GB of Differential Comparator

The gain bandwidth (GB) product should be high [11]. In the high speed comparator, the differential amplifier should have a wide bandwidth [3]. Meanwhile, it should have a high gain to amplify the input signals. GB can be increase by increasing drain current of transistor M5 and decreasing compensation capacitor Cc.

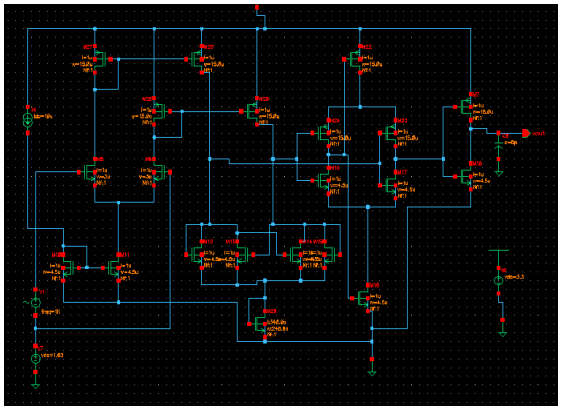


Figure 4. Circuit diagram of the preamplifier latch comparator

But when we increase the current in transistor M5 the DC gain start decreasing and power consumption will also increase. So we have to choose the appropriate vale of drain current of transistor M5.

Gain of first stage

$$Av1=\frac{gm1}{gds2+gds4} \quad (1)$$

Gain of second stage

$$Av2=\frac{gm6}{gds6+gds7} \quad (2)$$

Total Gain $(A_V) = A_{V1} * A_{V2}$ (3)

Gain Bandwidth (GB) = $\frac{g_{m1}}{C_c}$ (4)

Gain and Bandwidth of the system is important for high resolution and high speed operation. From the above equations Gain Bandwidth (GB) can be increase by increasing aspect ratio of the transistor M1, M2 and it also depends on compensation capacitor (Cc).

B. High Resolution of Comparator

Latch comparator has faster response, but input should be large. So latch added after pre-amp have large input amplified by pre-amp. Pre-amp added before latch will reduce the offset because offset will not transfer continuously during complete cycle. The offset voltage can be expressed by the equation:

$$\sigma^2 V_{OS} = \sigma^2 V_{OS1} + \frac{1}{A_{pre}} \sigma^2 V_{OS2} \quad (5)$$

In this paper the pre-amp has a high gain, so the main offset voltage is caused by the pre-amp. According to the analysis in the literature [17], this offset can be approximately expressed by the equation

$$\sigma^2 V_{OS} \approx \sigma^2 V_{OS1} \approx \sigma_{3,4}^2 + \sigma_{5,6}^2 + \sigma_{8,9}^2 + \sigma_{7,10}^2 + \frac{\Delta Q^2}{C^2} \quad (6)$$

$$\sigma_{3,4}^2 \approx \frac{A_{VTN}^2}{W_{3,4}L_{3,4}} + \frac{V_{DAST3,4}^2}{4} * \frac{A_{\beta N}^2}{W_{3,4}L_{3,4}} \quad (7)$$

$$\sigma_{5,6}^2 \approx \frac{A_{VTN}^2}{W_{6,5}L_{5,6}} + \frac{V_{DAST5,6}^2}{4} * \frac{A_{\beta N}^2}{W_{5,6}L_{5,6}} \quad (8)$$

$$\sigma_{8,9}^2 \approx \frac{1}{A_{pre}}\left[\frac{A_{VTP}^2}{W_{8,9}L_{8,9}} + \frac{V_{DAST8,9}^2}{4} * \frac{A_{\beta P}^2}{W_{8,9}L_{8,9}}\right] \quad (9)$$

$$\sigma_{7,10}^2 \approx \frac{1}{A_{pre}}\left[\frac{A_{VTP}^2}{W_{7,10}L_{7,10}} + \frac{V_{DAST7,10}^2}{4} * \frac{A_{\beta P}^2}{W_{7,10}L_{7,10}}\right] \quad (10)$$

In the equations above, A_{VTP}^2, A_{VTN}^2 and $A_{\beta P}^2$, $A_{\beta N}^2$ denote the standard difference of threshold voltage and technical mismatch respectively. W, L denotes the width and length of corresponding transistors. V_{DAST}^2 are initial overdriving voltage of the corresponding transistors. A_{pre} denotes the gain of preamplifier. ΔQ is the charge injection mismatch caused by turning off M7.

These equations show that, in order to obtain a small offset, transistors M3-M10 need to be made large, at the same time design the transistors have small initial overdriving voltage. It reduces the charge injection caused by M7.

C. High Speed of the Comparator

If we use multistage or latch comparator individually propagation delay will be more, so combining these two propagation delays will reduce. High speed can be achieved. The time constant of latch is:

$$\tau_L \approx \frac{\tau}{g_m R} = \frac{C}{g_m} \quad (11)$$

If C is mostly the gate-source capacitance, then the latch time constant can be expressed as

$$\tau_L = \frac{0.67WLC_{OX}}{\sqrt{2K'(W/L)I}} = 0.67C_{OX}\sqrt{\frac{WL^3}{2K'I}} \quad (12)$$

In where W, L, I denote the width, length, and initial current of the transistor respectively.

The propagation delay of latch can be found be found by:

$$t_p = \tau_L \ln\left(\frac{V_{OH} - V_{OL}}{2\Delta V_i}\right) \quad (13)$$

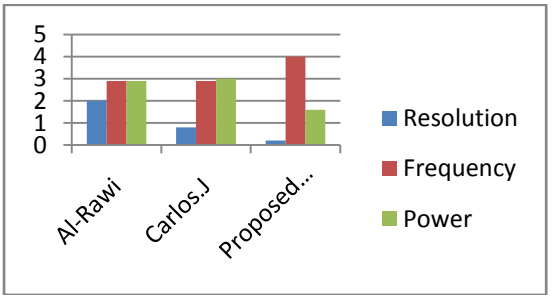
From the above equation ΔV_i is always less than 0.5($V_{OH} - V_{OL}$), the argument of the logarithm is always greater than unity.

4. SIMULATED RESULTS

In the circumstance of cadence composer, based on UMC 0.18µm CMOS process model the graphs (a), (b), (c) and (d) given below are of gain, offset voltage, propagation delay and power consumption. The observed values are 25dB, 17.11µV, 18.18ns and 210.10µW respectively. The graph (e) shows the layout of the comparator. The gain calculation is done by the equation (2). The stability of the system can be done by selecting appropriate value of load capacitor for good phase margin. However the mean value of the absolute value of the offset is approximately 17.11µV. Hence input signals can amplify enough to overcome the offset voltage at a wide bandwidth.

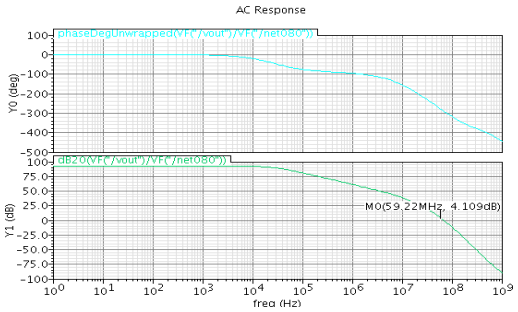
TABLE I. COMPARISON OF SEVERAL COMPARATORS

Author	Resolution	Frequency	Power
Al-Rawi [4]	400µV	40MHz	1mW
Kotani [10]	4mV	Not reported	4.3µW/(MS/s) (172µW @40 MHz)
Carlos J Solis [2]	1.8mV	40MHz	750µW
Proposed Design	17.11µV	55MHz	210.10µW

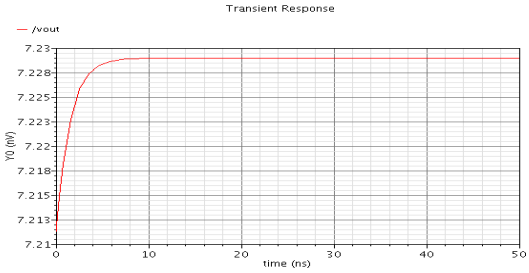


5. CONCLUSION

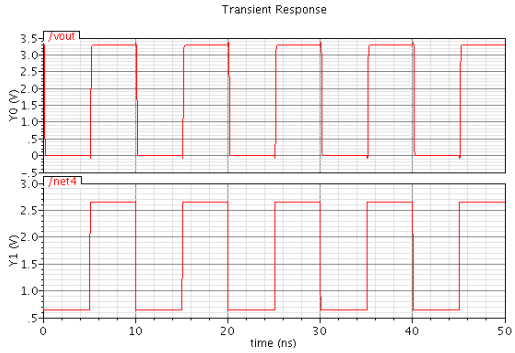
The paper introduces a novel high speed comparator. The resolution and the dynamic characteristics are also good. It is designed and simulated in a UMC 0.18µm technology. The simulation results show its gain is 25dB which is important for high resolution. The propagation delay is 18.18ns it is suitable for high speed ADC.



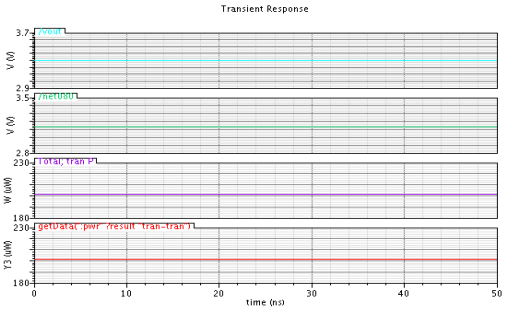
(a) AC analysis of comparator



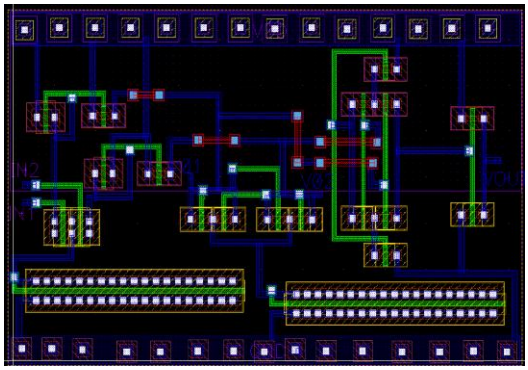
(b) Transient analysis for offset calculation



(c) Transient analysis of comparator



(d) Power analysis of comparator



(e) Chip Layout simulation of comparator

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