High Speed Digital Input Buffer Circuits

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***Abstract*—This paper illustrates design, fabrication and testing of novel differential high-speed digital input buffers. The delay of the proposed input buffers are nearly independent of power supply voltage and input signal amplitudes. The pulse shape of the output signal is highly symmetric which mitigates skew related errors.**

Keywords- CMOS, Differential Amplifier, Digital design, High-frequency Input Buffer.

I. INTRODUCTION

Input buffer circuits are present at a chip's input and convert input signals with imperfections such as slow rise and fall times into clean, full logic level digital signals for use inside the chip. If the buffer doesn't slice the data at the correct time instants, timing errors can occur. If the input signal is sliced too high or too low, the output signal's width is incorrect. In the high speed systems this reduces the timing budget in the systems and can result in errors [1]. This paper presents design, fabrication and test results of novel, differential high-speed input buffers which mitigate these problems.

II. DIFFERENTIAL INPUT BUFFER CIRCUITS

In order to precisely 'slice' the input data, the data is transmitted differentially as an input and its complement. A differential amplifier input buffer amplifies the different between the two inputs. The buffer topologies used in this design employ self biased differential amplifiers as no external reference is used to set the bias current in the diff-amp [1],[2]. Fig.1 shows an NMOS version of input buffer. When the input falls below V_{THN}, then the circuit will not work very quickly as the NMOS are moved into subthreshold region. This will result in an increase in the delay [1].

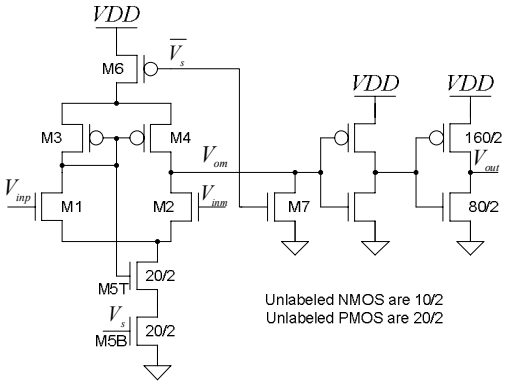

Figure 1. NMOS input buffer

Ideally, the delay of the buffer should be independent of power supply voltage, temperature, input signal amplitudes or pulse shape. In order to obtain better performance for lower input level signals, a PMOS version of input buffer (fig.2) can be used. However this scheme leads to the appearance of a large offset. To avoid the offset, the NMOS buffer can be used in parallel with a PMOS buffer as shown in fig.3, to form an input buffer that operates well with input signals approaching ground or *VDD*. The topology with the buffers in parallel provides a robust input buffer that works for a wide range of input voltages [1].

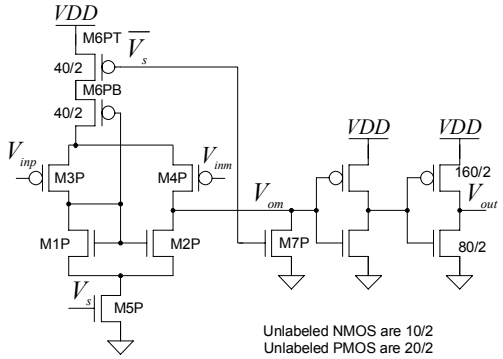

Figure 2. PMOS input buffer

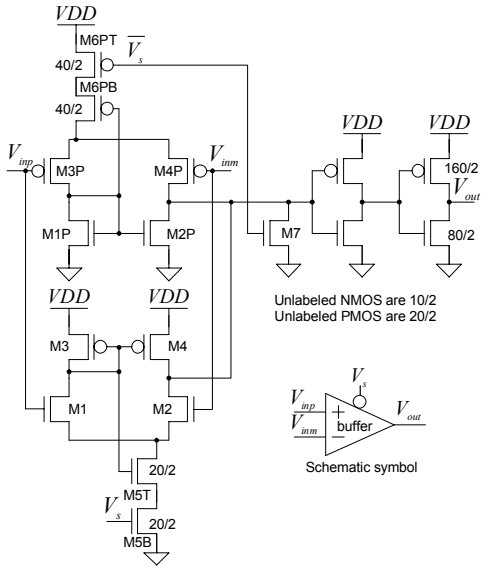

Figure 3. Rail-to-rail input buffer combining NMOS and PMOS buffers

The input buffers are designed with 'enable' logic using the NMOS and PMOS switches, like M5B and M6 in fig.1,

controlled by signals V_s and $\overline{V_s}$. When the enable signals are off, the output of the diff-amp will be in high impedance state. This can cause a large amount of current to flow in the inverters and damage the chip. To avoid this scenario, a switch M7 is connected to the output of the diff-amp which clips the node to ground when the buffer is disabled.

The buffers are fabricated in AMI's CN5 (0.5µm) process with a *VDD* of 5V as shown in fig. 4. The buffers are designed to drive a load of 30pF which accounts for the load offered by the probe setup. A large inverter (160/80) is used to drive the large load with optimal delay.

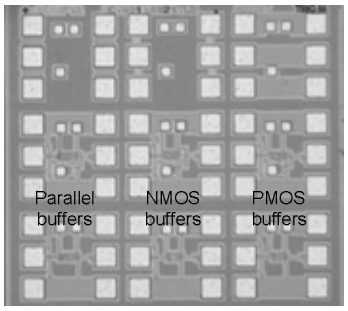

Figure 4. Micrograph showing the input buffer circuits fabricated on a chip.

III. TEST RESULTS

The input buffers were tested using the setup shown in fig.5. The common mode reference voltage V_{ref} was nominally kept at 2.5V and the input differential signal v_p (clock pulses with 1MHz frequency) was applied at the positive terminal of the buffer. The net delay was measured as the sum of charging and discharging delays (i.e. $t_{pLH} + t_{pHL}$). Figs.6-9 show the net delay offered by the input buffers for varying supply voltage, common mode reference voltage, input signal swing and temperature respectively.

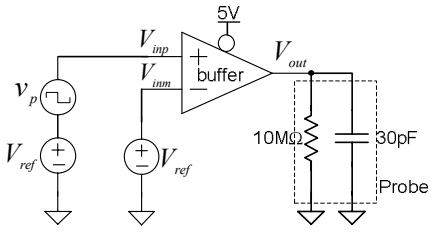

Figure 5. Test setup for the input buffers

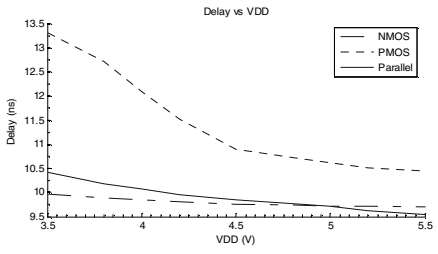

Figure 6. Delay vs supply voltage (*VDD*) plot for the input buffers.

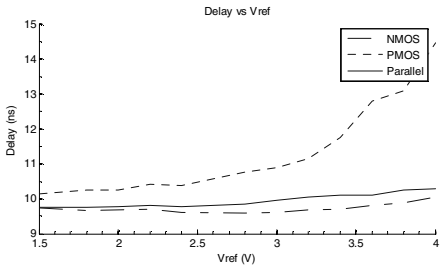

Figure 7. Delay vs common mode reference (*Vref*) plot for the input buffers.

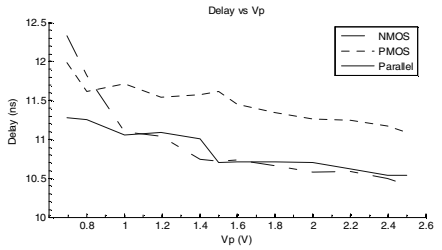

Figure 8. Delay vs input signal swing (*Vp*) plot for the input buffers.

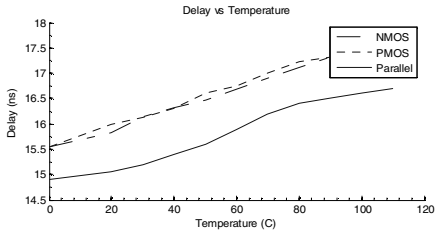

Figure 9. Simulated delay vs temperature plot for the input buffers.

The test results demonstrate that the designed input buffers operate well for high-speed input signals. The delay is virtually independent of power supply voltage, input common mode reference and voltage swing. The output pulse is highly symmetric and skew is absent. The parallel buffer topology provides the optimal performance for wide range of input voltages.

IV. CONCLUSION

A set of differential high-speed input buffers have been designed, fabricated and tested. The designed input buffers provide high frequency operation with lower delays. The delays are nearly independent of variations in power supply, input signal common mode and differential voltages, and temperature.

REFERENCES

[1] R. J. Baker, *CMOS: Circuit Design, Layout and Simulation, 2nd ed*. Boise, ID: Wiley-IEEE, 2005, pp. 531-538

[2] M. Bazes, "Two Novel Fully Complementary Self-Biased CMOS Differential Amplifiers," *IEEE Journal of Solid State Circuits*, vol. 26, no. 2, Feb. 1991.