A High-Speed CMOS Comparator with 8-b Resolution

G. M. Yin, F. Op't Eynde, and W. Sansen

Abstract—**This paper introduces a high-speed CMOS comparator. The comparator consists of a differential input stage, two regenerative flip-flops, and an *S-R* latch. No offset cancellation is exploited, which reduces the power consumption as well as the die area and increases the comparison speed. An experimental version of the comparator has been integrated in a standard double-poly double-metal 1.5-μm n-well process with a die area of only 140 × 100 μm^2. This circuit, operating under a +2.5/−2.5-V power supply, performs comparison to a precision of 8 b with a symmetrical input dynamic range of 2.5 V (therefore ±0.5 LSB resolution is equal to ±4.9 mV).**

I. Introduction

THE FUNCTION of comparison is a crucial, and often a limiting component in the design of high-speed data conversion systems due to its finite accuracy, comparison speed, and power consumption. More advances in MOS technologies allow MOS comparators to be realized for higher speed applications. However, it is difficult to achieve a high speed and a high accuracy (for example, 8 b) at the same time, due to MOS device mismatches. The highest operating speeds of MOS comparators with 8-b precision previously introduced have been limited to sampling rates of 30 and 40 MHz in 1.5- and 2-μm CMOS technologies, respectively [1]–[5].

This paper presents the design of a very low-power, very small-area, and high-speed CMOS comparator appropriate for use in conventional and sigma–delta analog-to-digital converters. The experimental prototype achieving 8-b accuracy with the sampling rates up to 65 MHz is obtained through a very fast circuit configuration, intensive transistor dimension optimizations, and careful layout, while no offset cancelling techniques are employed. The power consumption of the comparator is only 0.85 mW at 65-MHz clock rate with 32.5-MHz input signal.

Section II of this paper describes the comparator circuit. Its operation in detail and design optimization are examined in Section III. Experimental results are presented in Section IV.

II. Comparator Circuit

The proposed comparator circuit is depicted in Fig. 1. It consists of a differential input pair ($M1$, $M2$), a CMOS latch circuit, and an *S-R* latch. The CMOS latch is composed of a n-channel flip-flop ($M4$, $M5$) with a pair of n-channel transfer gates ($M8$, $M9$) for strobing and an n-channel switch ($M12$) for resetting, and a p-channel flip-flop ($M6$, $M7$) with a pair of p-channel precharge transistors ($M10$, $M11$). ϕ_1 and ϕ_2 are the two nonoverlapping clocks.

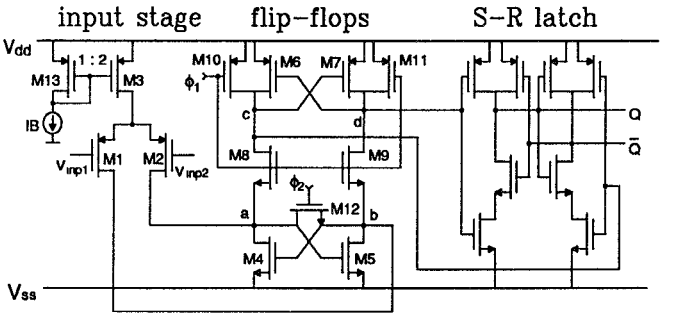

Fig. 1. Schematic of the CMOS comparator.

The dynamic operation of this circuit is divided into a reset time interval and a regeneration time interval. The two intervals are approximately between t_1 and t_2 and between t_2 and t_4, respectively, as shown in Fig. 2. During ϕ_2, the comparator is in the reset mode. Current flows through the closed resetting switch $M12$, which forces the previous two logic state voltages to be equalized. After the input stage settles on its decision, a voltage proportional to the input voltage difference is established between nodes a and b in the end. This voltage will act as the initial imbalance for the following regeneration time interval. In the meantime, as the n-channel flip-flop is reset, the p-channel one is also reset by the two closed precharge transistors which charge nodes c and d to the positive power supply voltage. As a result, the CMOS latch is set to the astable high-gain mode.

The regeneration is initialized by the opening of switch $M12$. Since the strobing transistors $M8$ and $M9$ isolate the n-channel flip-flop from the p-channel flip-flop when ϕ_1 is low, the use of two nonoverlapping clocks performs the regenerative process in two steps. The first step of regeneration is within the short time slot between ϕ_2 getting low and ϕ_1 getting high. The second regeneration step starts when ϕ_1 gets high and $M8$ and $M9$ are closed. The n-channel flip-flop, together with the p-channel flip-flop, regenerates the voltage differences between nodes a and b and between nodes c and d. The voltage difference between node c and node d is soon amplified to a voltage swing nearly equal to the power supply voltages. The following *S-R* latch is driven to full complementary digital

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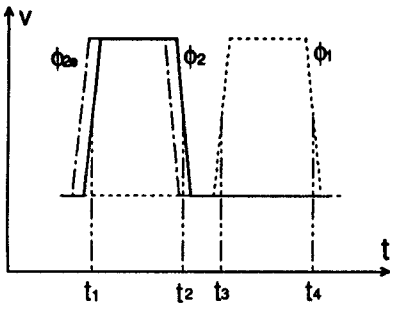


Fig. 2. Time relation between ϕ_2, ϕ_{2e}, and ϕ_1.

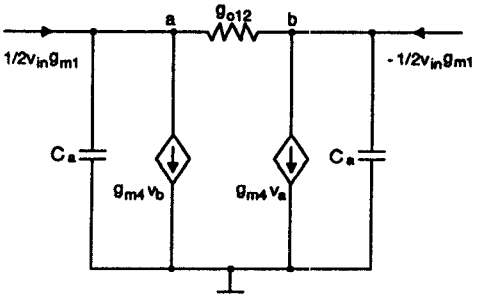


Fig. 3. Linearized small-signal model.

output levels at the end of the regenerative mode and remains in the previous state in the reset mode. There is no slew-rate problem in the regenerative period because the p-channel flip-flop is used instead of two class-A current sources.

The first regeneration step is very important, not only in raising the regeneration speed but in reducing the total input offset voltage. The differential errors caused by the charge injection from $M8$ and $M9$, the mismatches in the p-channel flip-flop, the two precharge transistors, and the S-R latch are divided by the amplification gain in the first regeneration step, when referred to the input as an equivalent offset voltage. Therefore, their contribution to the total equivalent input offset voltage can be neglected if the gain is large enough.

III. Operating Analysis and Design Optimizations

Our goal is to design a comparator that has optimum comparison speed, high accuracy, and low power consumption. In order to achieve high comparison speed, the minimum channel length is used for all transistors.

A. Regeneration Speed and Equivalent Input Offset Voltage

The comparison mechanism has to be closely explored in order to optimize speed and accuracy. At the time when ϕ_2 falls, voltages at nodes a and b decrease because of the clock injection, and in the meantime the currents from $M1$ and $M2$ charge the two nodes to resume their voltages. Later, as the conductance of switch $M12$ becomes smaller than half of the transconductance of $M4$ and $M5$, the n-channel flip-flop starts the first step of regeneration. This regeneration process can be approximately analyzed using a small-signal model as shown in Fig. 3, where the mismatches in the two transistor pairs and their output conductances are ignored. In this equivalent circuit, g_{m1}, g_{m4}, and g_{o12} are the transconductances of $M1$ or $M2$, $M4$ or $M5$ and the conductance of $M12$, respectively. C_a represents the capcitance at node a or b. Then we can derive two differential equations as follows:

$$1/2\ v_{in}g_{m1} = C_a\, dv_a/dt + g_{m4}v_b + g_{o12}(v_a - v_b) \tag{1}$$

$$-1/2\ v_{in}g_{m1} = C_a\, dv_b/dt + g_{m4}v_a - g_{o12}(v_a - v_b). \tag{2}$$

In the equations, v_{in} is equal to $v_{inp1} - v_{inp2}$. Voltages v_a and v_b stand for the increments relative to the voltage at nodes a and b with zero input difference. Solving (1) together with (2) gives

$$v_{ab} = [v_{a0} - v_{b0} - g_{m1}/(2\ g_{o12} - g_{m4})\ v_{in}]\ \exp\ (t/\tau) + g_{m1}/(2\ g_{o12} - g_{m4})\ v_{in} \tag{3}$$

with the time constant

$$\tau = C_a/(g_{m4} - 2\ g_{o12}). \tag{4}$$

Expressions (3) and (4) show that when g_{o12} is smaller than half of g_{m4}, τ becomes positive and the first step of regeneration starts. In (3), v_{a0} and v_{b0} are the increments at the initial moment, and v_{ab} stands for $v_a - v_b$. The differential charge injection error, say V_e, from the fast turn-off of $M12$ causes $v_{a0} - v_{b0}$ to be different from the value established in the end of the last reset mode, which adds some offset to the comparator. Therefore the total equivalent input offset voltage can be approximately expressed as

$$V_{off} = V_{off1} + g_{m4}/g_{m1}(V_{off2} + V_e). \tag{5}$$

In the equation, V_{off1} and V_{off2} represent the offset voltages in the input transistor pair and the n-channel flip-flop transistor pair, respectively. A negligible error can be realized if $M12$ is sized in relation to the total capacitance C_a or C_b and the comparator is laid out symmetrically. The term $g_{m4}/g_{m1}V_{off2}$ is normally smaller than V_{off1} since the two transistors in the n-channel flip-flop are at 0-V substrate bias.

To optimize the speed of the first regeneration step, the most efficient way is to minimize the time constant. When $M12$ is switched off, the time constant only depends on the capacitance at node a or b and the transconductance of $M4$ or $M5$. The capacitance is related to the sizes of $M1$, $M2$, $M4$, $M5$, $M8$, $M9$, and $M12$. Because the width of $M12$ also directly affects the resetting speed, let us first have a look at the resetting process.

B. Resetting Process and Resetting Speed

It is shown in (3) that the initial voltage difference, $v_{a0} - v_{b0}$, is very important in the decision of the regenerative direction. Imperfect resetting will cause hysteresis.

As an example, assume that node a is at a high-voltage level before reset. The voltage difference between nodes a and b reduces very quickly at the beginning of the reset. Later the reduction rate slows down. It will have a local minimum at some instant if the current through $M12$ is equal to the current through $M5$ while $M4$ just reaches the edge of conducting, which should be avoided in high-speed applications. Therefore, the width of $M4$ or $M5$ and $M12$ should satisfy the inequality of $I_{12} > I_5$ at that moment to ensure that there is still some extra current to charge node b. By using a simplified current model, the inequality is

$$W_{12}/L\, K_{pn}[(V_{dd} - V_b - V_{Tn12})(V_a - V_b) - 0.5(V_a - V_b)^2)] > W_5/L\, K_{pn}[(V_a - V_{ss} - V_{Tn5}) \cdot (V_b - V_{SS}) - 0.5(V_b - V_{SS})^2)]. \quad (6)$$

The voltage at node a is about 1.2 V before the reset mode starts because n-channel strobing transistors are used. A value of V_a in (6) of several hundred millivolts could be taken. V_{Tn} is about 0.75 V and V_b is about -1.75 V. Solving (6) according to the technological parameters gives as an approximate expression $W_{12} > 1/4\ W_4$.

In the second period of the reset mode, the circuit behavior can be derived using the same small-signal model shown in Fig. 3. Under the resetting circumstances, we obtain

$$v_{ab} = g_{m1}v_{in}/(2\ g_{o12} - g_{m4}) + A \exp(t/\tau) \quad (7)$$

$$v_a + v_b = B \exp(-g_{m4}/C_a t) \quad (8)$$

where τ is expressed the same as in (4). Parameters A and B can be decided by some initial conditions. Expressions (7) and (4) indicate that if $2\ g_{o12}$ is smaller than g_{m4} it is impossible to have the comparator reset. For $W_{12} > 1/4\ W_4$, $2\ g_{o12}$ is more than five times g_{m4} when $V_{GS4} - V_T$ is about 0.3 V. The stable values are $g_{m1}v_{in}/(2\ g_{o12} - g_{m4})$ for v_{ab} and 0 for $v_a + v_b$. This v_{ab} is much smaller than v_{in}, since g_{m1} and g_{m4} are about equal in order to obtain a minimum regeneration time constant as discussed later. From (8) we can see that resetting $v_a + v_b$ will be no problem if a small time constant for the first step of regeneration is realized.

Knowing the approximate size of $M12$, now we can optimize the regeneration time constant.

C. Optimization Results

When $M12$ is off, the time constant in the first regeneration step can be written as

$$\tau_{reg} = (\alpha W_4 + C_p)/\sqrt{2I_4 W_4/L_4 K_{pn}} \quad (9)$$

where α is a parameter. αW_4 represents the capacitance related to the width of $M4$ or $M5$, and it will also include the capacitances from $M12$ and $M8$ or $M9$ if W_{12}, W_8, and W_9 are all chosen to be proportional to W_4. C_p is the other parasitic capacitances at node a or b.

For certain current I_4, a minimum τ_{reg} can be obtained when the equation $\alpha W_4 = C_p$ is satisfied. Then the following relations between the transistor widths are derived: $W_{12} = 1/3\ W_4$, $W_1 = 2\ W_4$, $W_8 = W_{12}$, $W_{10} = 2.5\ W_{12}$, and $W_6 = 2.5\ W_4$, with the help of SPICE simulations.

A comparator was designed according to those optimum conditions. Taking into account the load effect from the S-R latch and the mismatch from transistor width, W_4 is chosen equal to 12 μm. The values of $V_{GS1} - V_{Tp1}$ and $V_{GS4} - V_{Tn}$ are 0.21 and 0.2 V with $IB = 20$ μA, and the symmetrical dynamic range is about 2.5 V. The reference current can be increased to raise the comparison speed. However, $V_{GS1} - V_{Tp1}$ will be larger, and a larger offset voltage will result. The simulated transient analysis shows the comparator can still perform comparison with 1-mV sensitivity for sampling rates of 150 MHz with $IB = 40$ μA.

With these dimensions the total capacitance at node a or b is about 0.05 pF. The time constant of the first step regeneration can be calculated to be 0.25 ns for $IB = 20$ μA. Therefore, the amplification gain will be 54 within 1 ns, while for the structure in [1], a time period of about 13.5 ns will be needed to obtain the same gain since the amplification is linear. Yet another several nanoseconds are needed to let the preamplifier set up the charging current, $g_{m1}\ v_{in}$. Therefore, a resetting time internal, i.e., when ϕ_1 is low, of more than 15 ns will be necessary, which obviously limits the comparison speed. The resetting interval plus the period for the first step of regeneration of the comparator presented here can be as small as 3 ns according to the simulation results. Another advantage is that when ϕ_1 is high, the comparator has been ready to regenerate while the comparator in [1] first needs some time to charge the drain nodes of the n-channel flip-flop to a voltage higher than the threshold.

The comparator has been used in an oversampling sigma–delta modulator [7]. When it is employed in a flash converter, the effects of kickback noise have to be considered. The effects can be greatly reduced by introducing a sampling switch controlled by ϕ_2 or ϕ_{2e} (ϕ_{2e} is a clock phase a bit earlier than ϕ_2) and a small capacitor with a value, say, of 0.1 pF before each of the comparator inputs. In order to reduce the charge injection error, these two switches must be sized as small as possible in relation to the total capacitance at the comparator input sides, and the whole structure must be laid out symmetrically.

IV. Experimental Results

A chip photograph of the die is shown in Fig. 4. Fifty chips are measured. About 40% of the chips exhibit an offset voltage less than 3.3 mV and sensitivity within 1.5 mV up to a sampling rate of 65 MHz. The highest offset plus sensitivity measured is 10.6 mV, which is about 7-b accuracy. It is believed that the offset voltage can be reduced by increasing the transistor dimensions [6] at the expense of comparison speed.

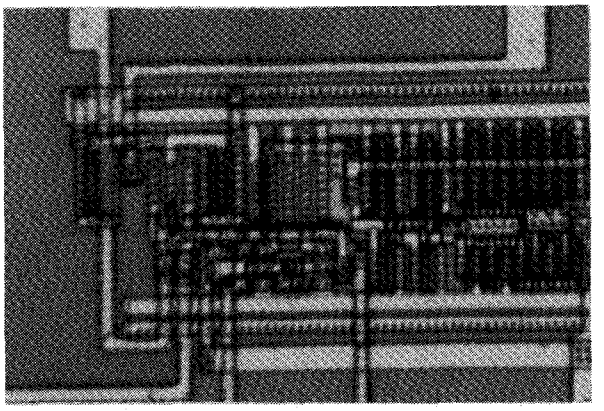
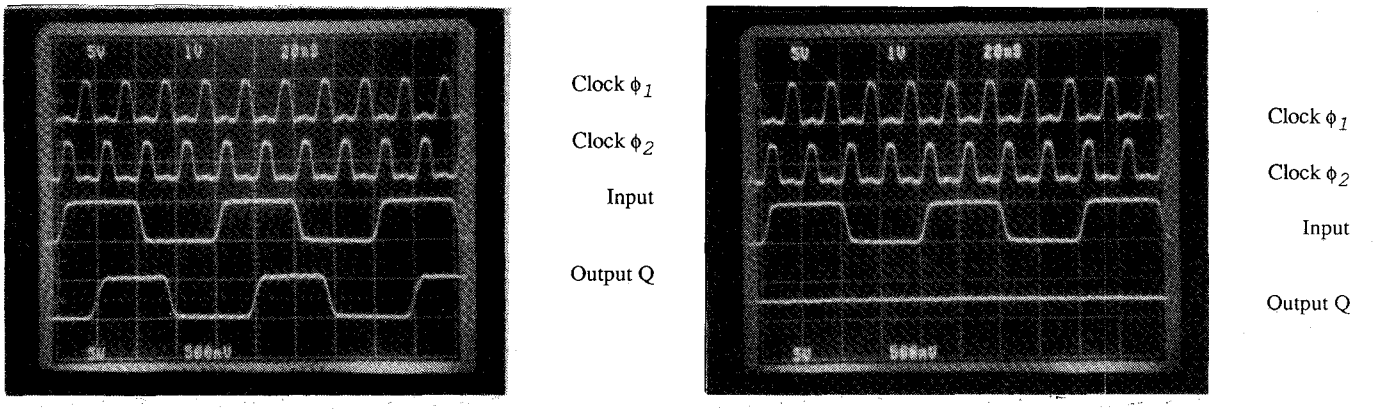


Fig. 4. Photograph of the comparator test die.



(a) (b)

Fig. 5. Oscilloscope photographs of typical waveforms for the input overdrive recovery test: (a) the input difference changes from -1 V to $+5$ mV; and (b) the input difference changes from -1 V to -5 mV.

Fig. 5(a) and (b) shows oscilloscope photographs of the waveforms for a typical chip, with overdrive input from -1 V to within ± 5 mV on the consecutive clock cycles. The waveforms demonstrate that the output correctly indicates the polarity of the input voltage wave.

The input capacitance of the comparator is 30 fF.

V. Conclusion

Since the comparator performs comparison directly by means of regeneration without extra offset cancellation circuit, substantial reduction in delay, power consumption, and die area has been achieved. The low offset voltage of the comparator is obtained through carrying out the comparison in two steps of regeneration with the use of two nonoverlapping clocks, and through design optimizations.

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