A Power Efficient and Fast Transient Response Low Drop-Out Regulator in Standard CMOS Process

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ABSTRACT

A low drop out regulator (LDO), which can adaptively change driving current to the PMOS gate and have a fast transient response time, is proposed in this paper. As we know, LDO circuits have to provide a regulated output voltage regardless of input voltage variation, load current variation, and process variation. A load transient test will test the transient behavior of changing output loading. In order to get a good performance in a load transient testing, a buffer with current driving capability is usually added in front of PMOS gate to make the transient response faster. This buffer needs to drive the PMOS gate, and it will consume a few quiescent current in LDO circuits. This static quiescent current will occupy a few percentage of power consumption of LDO circuits at a light load condition, and the efficiency of the LDO at a light load condition will be very poor. In this paper, we proposed a new architecture of LDO, which can adaptively change the driving current of the buffer to the PMOS gate. Then we can improve the efficiency of the LDO up to 10% at light load condition. Meanwhile, we can have a fast transient response time. The load transient response time from 1mA to 138mA is about 2us, which is faster than other reference designs. This chip is manufactured in 0.35um standard CMOS process, and it consumes 24uA in a light load condition.

I. INTRODUCTION

In modern hand-held and portable devices, low drop out regulators (LDO) are used extensively because they can provide a regulated output voltage, which is not affected by input voltage changes, output loading variation and other environmental disturbances. LDO circuits not only can provide a stable output voltage with good noise performance but also consume less power consumption than switching regulators. They are used in many applications such like cellular phones, PDA, and other portable devices, and they are usually important components in power management circuits and systems.

Although LDO circuits have such many advantages, they encounter several problems in their design and implementation. The first one is the stability problem. Because of the low drop out voltage, a standard architecture, as illustrated in Fig.1, will use a PMOS transistor to be the power device. Then it will induce a significant pole and cause complexity to compensate the frequency response. In [1], a solution, which uses a VCCS circuit to generate an additional zero to compensate the frequency response, was proposed. By utilizing this topology, we can add an extra zero in frequency response and promote the phase margin of the loop response. However, a buffer is still needed to drive the gate capacitance of PMOS so as to get a fast transient response. The gate capacitance of PMOS will also induce a significant pole and degrade the stability. Therefore, we need a buffer to keep this significant pole far away from the dominant pole. Then this buffer will consume significant power consumption at a light load condition.

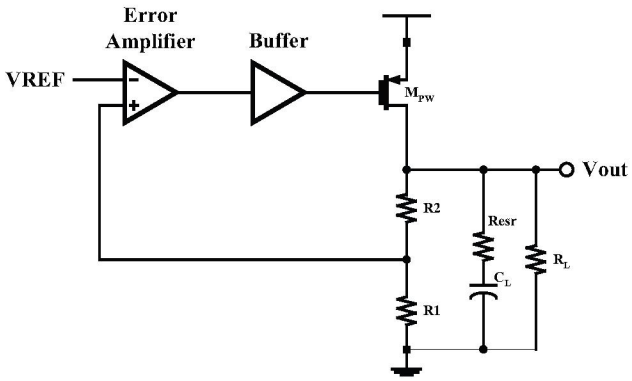

Fig. 1 General LDO architecture

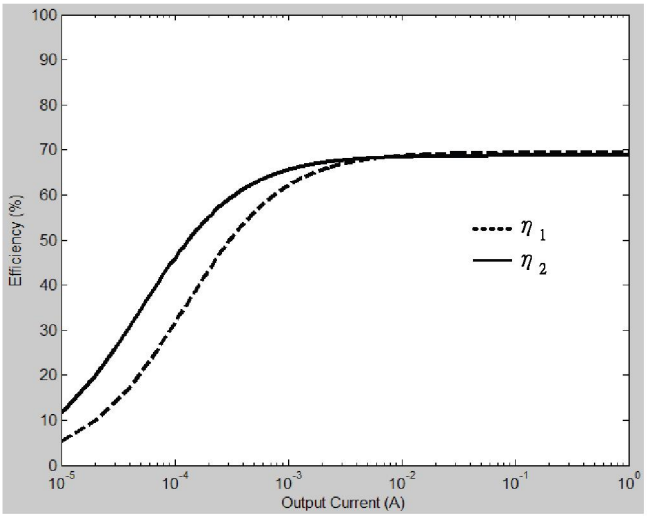

Fig. 2 Comparison of efficiency between general LDO and proposed LDO
η_1: general LDO; η_2: proposed LDO

In [2], an emitter follower buffer with an npn bipolar transistor is used to drive the PMOS gate. However, it needs to be implemented in BiCMOS process to get an npn bipolar transistor. If we replace the npn transistor with a NMOS transistor, we will encounter the worse driving ability and the voltage headroom problem. In this paper, we propose a LDO architecture that can adaptively change the bias current with the loading condition. Then we can improve the efficiency of the LDO at a light load condition without degrading the transient response time.

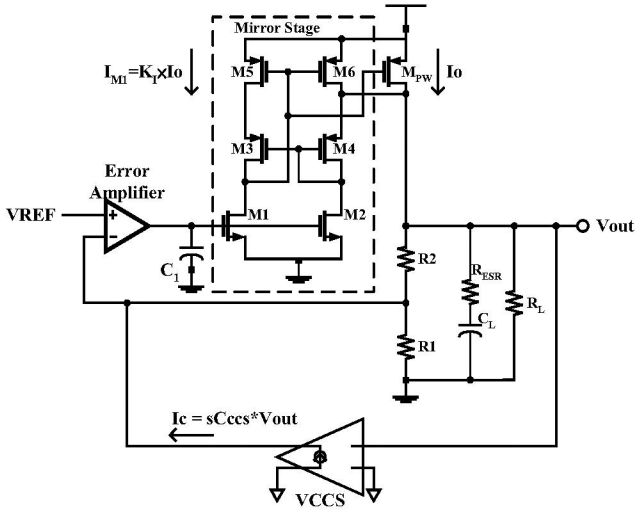

Fig. 3 Proposed LDO architecture

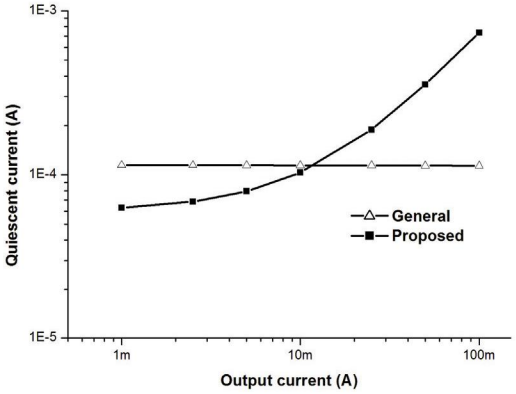

Fig. 4 Quiescent current vs. output current

The general efficiency equation is

$$\eta_1 = \frac{I_O \bullet V_O}{I_O \bullet V_O + I_O \bullet (Vdd - Vo) + I_q * Vdd} \times 100\%$$

Where Io is the output current, Vo is the output voltage, Vdd is the input supply voltage, Iq is the internal quiescent current.

In this design, we let $I_q = K_I \bullet I_O + I_{q,base}$ to accomplish the behavior of changing bias current with load current, where K_I and $I_{q,base}$ are constant factors. Then we can modify the original equation into the following equation.

$$\eta_2 = \frac{I_O \bullet V_O}{I_O \bullet V_O + I_O \bullet (Vdd - Vo) + (K_I I_O + I_{q,base}) * Vdd} \times 100\%$$

If we assume a typical condition that is Vdd=3.6V, Vo=2.5V, Iq=120uA, K_I=0.01, $I_{q,base}$=50uA, we can then get the simulation results, which are illustrated in Fig. 2. As Fig. 2 described, we can know that the efficiency at a light load condition will be improved to about 10% by using the proposed topology.

The detailed descriptions about the proposed topology will be explained in the following section.

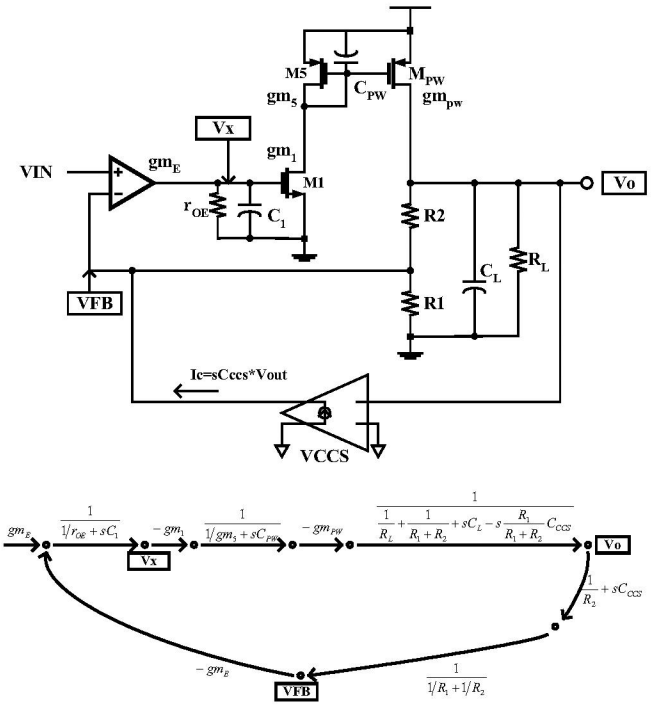

Fig. 5 Small signal analysis by signal flow graph topology

II. Circuit Topology

The proposed LDO regulator is shown in Fig. 3. As illustrated in Fig. 3, the LDO is comprised of an error amplifier, a mirror stage (M1-M6), a power transistor (M_{PW}), feedback resistors, and an output capacitor. The mirror stage can keep the bias current of the mirror stage proportional to the output current. As Fig. 3 described, The current I_{M1} is equal to K_I×Io, and the quiescent current of the LDO can be written as $I_q^{'} = K_I \times I_O + I_{q,base}$, *where the* $I_{q,base}$ *is a constant factor.*

Therefore the power loss resulted from I_q×V_{DD} can be decreased when Io goes low. However, the equation also shows that I_q will become large when Io goes high. Then the large quiescent current can possibly degrade the efficiency of the LDO in a heavy load condition. Fortunately, from the equation of η_2, Io×Vo becomes dominant when Io goes high. Then the power loss resulted from $I_q^{'} \times V_{DD}$ will not degrade the efficiency a lot, just as the right side of Fig. 2 illustrated.

The loop response of the proposed LDO is analyses by signal flow graph method [3], which is depicted in Fig. 5. The transfer function can be written as

$$\frac{V_O}{V_{IN}} = \frac{A(s)}{1 + A(s)\beta(s)}$$

, Where

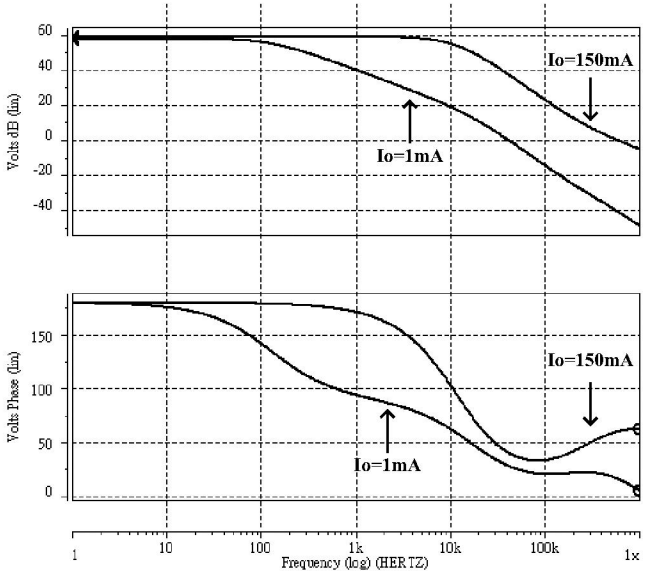

Fig. 6 Simulated AC responses of the proposed LDO

$$A(s)=\frac{gm_E}{\frac{1}{r_{OE}}+sC_1}\cdot\frac{gm_1}{gm_5+sC_{PW}}\cdot\frac{gm_{PW}}{\frac{1}{R_L}+\frac{1}{R_1+R_2}+sC_L-s\frac{R_1}{R_1+R_2}C_{CCS}}$$

$$\beta(s)=\frac{1+sR_2C_{CCS}}{1+\frac{R_2}{R_1}}$$

With the assumption of Aβ>>1, we can know the DC characteristic is $\frac{V_O}{V_{IN}}=1+\frac{R_2}{R_1}$

Then we can design the desired output voltage by selecting proper resistor values of R_1 and R_2.

From the equation of the loop response A(s)β(s), we can know that this loop contains three poles and 1 zero. They are described as follows.

$$pole_1\sim\frac{1}{2\pi}\frac{1}{R_L\,||\,(R_1+R_2)\,||\,C_L}\ (\text{Assume } C_L>>\frac{R_1}{R_1+R_2}C_{CCS})$$

$$pole_2\sim\frac{1}{2\pi}\frac{1}{r_{OE}C_1},\ pole_3\sim\frac{1}{2\pi}\frac{gm_5}{C_{PW}},\ zero_1\sim\frac{1}{2\pi}\frac{1}{R_2C_{CCS}}$$

Here we neglect the zero generated by ESR of C_L.

Then we can design the frequency response of the LDO. We let the $pole_1$ be the donminant pole and let $pole_2$ be the non-donminant pole. $Zero_1$ is designed to be higher than $pole_2$ to compensate the phase margin. The designed values are R_1=113.25kΩ, R_2=120kΩ, C_L=1uF, Cccs=7.6pF, C_1=4.8pF, r_{OE}=1.62MΩ, and R_L is from 16.67 Ω to 2.5kΩ. Finally we can get a stable loop response. The phase margin are 60° at I_L=150mA and 28° at I_L=1mA. The simulation results of AC response are shown in Fig. 6.

The detailed transistor sizes of the error amplifier are shown in Fig. 7, and the bias current of the error amplifier is about 5uA. The

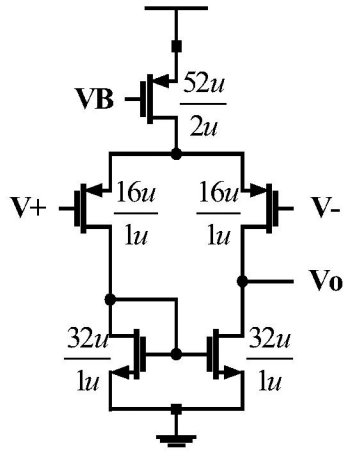

Fig. 7 Error amplifier schematics

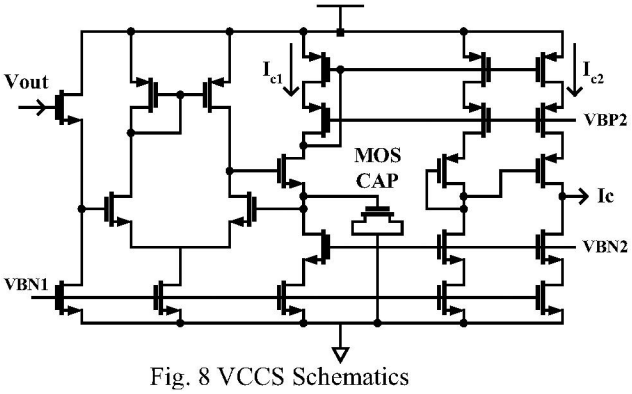

Fig. 8 VCCS Schematics

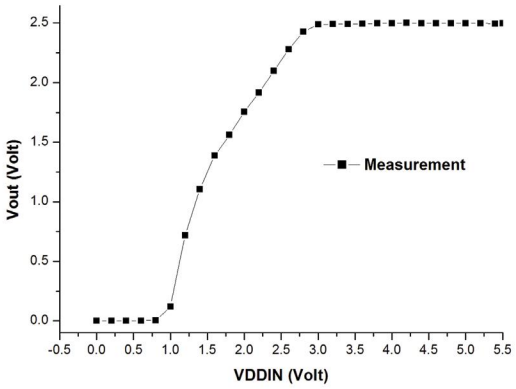

Fig. 9 Measured line regulation characteristic

schematics of VCCS circuits [1] are described in Fig. 8. Here we let I_{C2}=2*I_{C1}=1.4uA, and the effective compensation capacitance=7.6pF.

III. Measurement Results

This chip is implemented in 0.35um 2P4M CMOS process. The output voltage of the proposed LDO is 2.5V. The measured line regulation characteristic is depicted in Fig. 9. As Fig. 9 described, the output voltage is locked at 2.5V over the range of VDD from 2.7V to 5.5V, and the line regulation error is about ±0.088%/V. The load transient response is shown in Fig. 10, Fig. 11 and Fig. 12. The load regulation error is about 20mV from 1mA to 138mA, and the transient response time is about 2us, which is faster than other reference designs. The die photo is illustrated in Fig. 13. The summary table is illustrated in Tabel I. This chip consumes 24uA quiescent current excluding bandgap reference circuits.

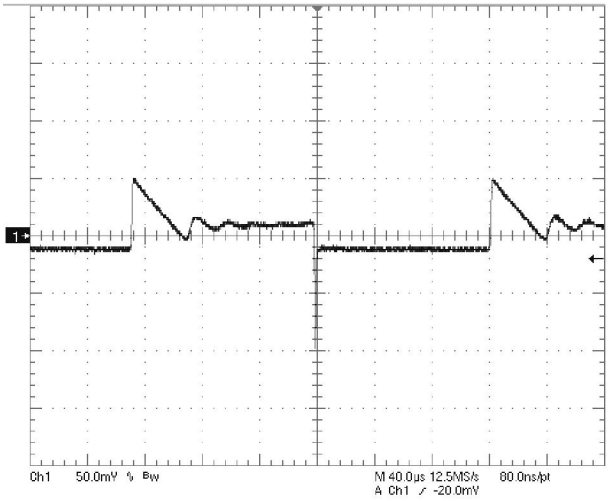

Fig. 10 Load transient testing
@ IL=1mA-138mA, VDD=3V

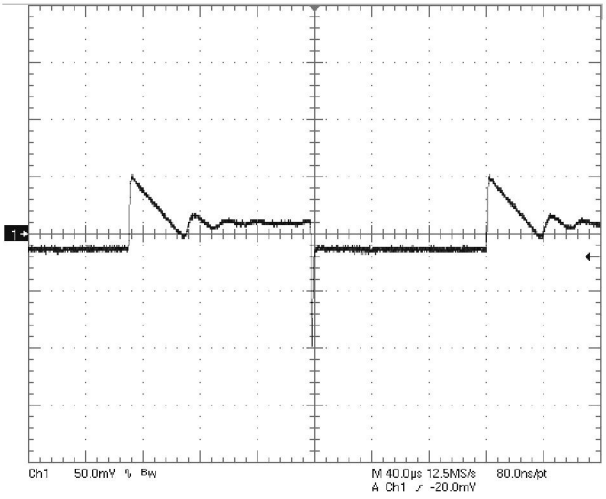

Fig. 11 Load transient testing
@ IL=1mA-138mA, VDD=5.5V

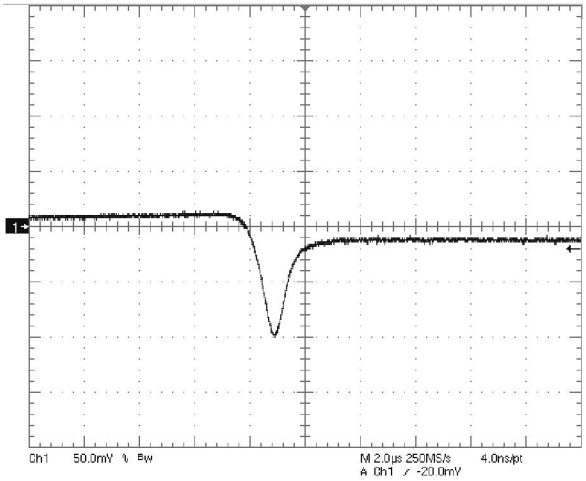

Fig. 12. Measured transient response time
@ IL=1mA-138mA, VDD=3V

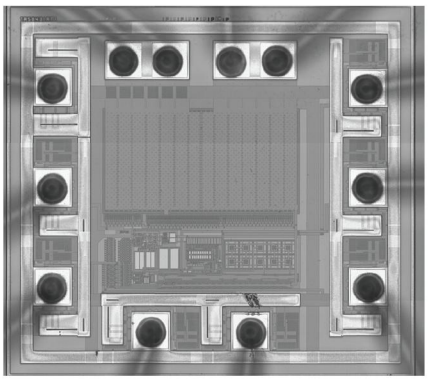

Fig. 13 Die photo

IV. Conclusion

In this paper, we proposed a new architecture to improve the power efficiency and transient response time of the LDO. By the proposed topology, the efficiency at a light load condition can be improved to about 10%, and the achieved transient response time is 2us, which is faster than other reference designs. This chip is manufactured in a low cost 0.35um CMOS process and consumes 24uA excluding bandgap reference circuit.

Tabel I. Summary Table

Parameter	**Ref [1]**	**Ref [2]**	**This work**
Process	CMOS	BiCMOS	CMOS
Vddin	3.3V	1.2V-5V	2.7V-5.5V
Vout	2.8V	1.2V	2.5V
Io	1mA-100mA	0-50mA	1mA-138mA
Iquiescent @Io=1mA	25uA	23uA	24uA
Response time	25us Io=1-40mA	50us Io=0-50mA	2us Io=1-138mA

References

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[2] Gabriel A. Rincon-Mora and Phillip E. Allen, "A Low-Voltage, Low Quiescent Current, Low Drop-Out Regulator", *IEEE Journal of Solid-State Circuits*, VOL. 33, No. 1, pp. 36-44, Jan. 1998.

[3] Khoman Phang, "CMOS Optical Preamplifier Design Using Graphical Circuit Analysis", *P.H.D. Thesis, University of Toronto in Canada*, pp. 74-107, 2001