

## A New High Performance CMOS Differential Amplifier

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### Abstract

Differential amplifiers play a very important role in the analog circuit design because of their excellent performance as input amplifiers and the straightforward application with the possibility of feedback to the input. The classical differential amplifier faces the disadvantage of the nonlinearity of the transfer characteristic, especially for large values of the differential input voltage amplitude. The differential amplifier circuit characterized in terms of self-bias capability, common-mode rejection, voltage gain, and the gain-bandwidth product. In this paper we report a new model for high performance CMOS differential amplifier. The proper selection of device parameters has been playing an important role in the design of differential amplifier. This model is simulated in SPICE simulator and optimized device parameters.

**Keywords:** Differential pair, CMRR, Transconductance, current Sink.

### Introduction

The differential amplifier is one of the most versatile circuits used in analog circuit design. These are widely used in the electronics industry and are generally preferred over their single-ended counterparts because of their better common-mode noise rejection, reduced harmonic distortion, and increased output voltage swing [1, 2, 3]. Differential amplifiers are used to amplify analog as well as digital signals, and can be used in various implementations to provide an output from the amplifier in response to differential inputs. It is also very compatible with integrated circuit technology and serves as the input stage to most of operational amplifier [3, 4, 5, 6, 7]. They can be readily adapted to function as an operational amplifier, a comparator, a sense amplifier and as a front-end buffer stage for another circuit.

The differential amplifier is often a building block or sub-circuit used within high-quality integrated circuit amplifiers, linear and nonlinear signal processing circuits, and even certain logic gates and digital interfacing circuits. In recent years, there has been an increasing demand for a system-on-chip configuration (SOC) and reduction of power consumption, in response to which the CMOS has been widely used [4, 8, 9, 10, 11].

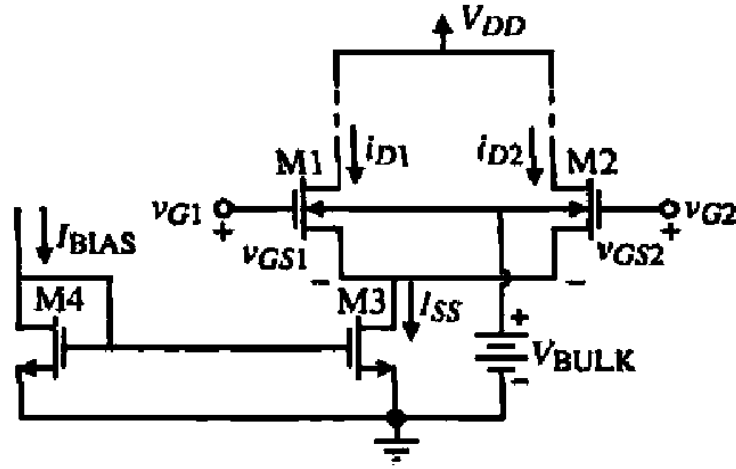
CMOS differential amplifiers are used for various applications because a number of advantages can be derived from these types of amplifiers, as compared to single-ended amplifiers. Differential amplifiers are used where linear amplification having a minimum of distortion is desired. A fully differential amplifier circuit is a special type of amplifier that has two inputs and two outputs. This device amplifies input signals on the two input lines that are out of phase and rejects input signals that have a common phase such as induced noise. The common mode feedback is accomplished by the use of a common mode feedback circuit that monitors the two differential amplifier output lines and provides a feedback signal that adjusts the amplifier's bias current, thereby rejecting the unwanted common mode signals on the amplifier's output.

The sensitivity is an important specification target for differential amplifier design. Component mismatching and their drift induces the extra output differential voltage, which is indistinguishable from the signal being processed. The extra output differential voltage limits the minimum detectable differential voltage level. Also, such mismatching could convert the common mode input signal to the differential output, which is treated as the desired signal by the subsequent stages.

### **Basic Differential Amplifier**

The objective of the differential amplifier is to amplify only the difference between two different potentials regardless of common mode value. It is characterized by its CMRR and its offset voltage. In ideal differential amplifier, the common mode gain should be zero and thus CMRR should be infinite, also the input offset voltage should be zero [12, 13, 14, 15, 17].

In real differential amplifier, the output offset voltage is the difference between the actual output voltage and the ideal output voltage when the input terminals are connected together. If this offset voltage is divided by the differential voltage gain of the differential amplifier then it is called the input offset voltage. Figure 1, shows the basic differential amplifier that uses n-channel MOSFETs M1 and M2 to form a differential amplifier. M1 and M2 are biased with a current sink  $I_{SS}$  connected to the sources of M1 and M2. This configuration of M1 and M2 is often called a source-coupled pair. The current sink  $I_{SS}$  is implemented using M3 and M4.



**Figure 1:** Basic CMOS Differential Amplifier.

The transistors M1 & M2 are perfectly matched and always worked in saturation region. The behavior of large signal analysis is given as

$$V_{ID} = V_{GS1} - V_{GS2} = \left( \frac{2i_{D1}}{\beta} \right)^{1/2} - \left( \frac{2i_{D2}}{\beta} \right)^{1/2}$$

$$\text{and } I_{DS1} = i_{DS1} - i_{DS2}$$

So,

$$i_{DS1} = \frac{I_{SS}}{2} + \frac{I_{SS}}{2} \left( \frac{\beta v_{ID}^2}{I_{SS}} - \frac{\beta^2 v_{ID}^4}{4I_{SS}^2} \right)^{1/2}$$

and

$$i_{DS2} = \frac{I_{SS}}{2} - \frac{I_{SS}}{2} \left( \frac{\beta v_{ID}^2}{I_{SS}} - \frac{\beta^2 v_{ID}^4}{4I_{SS}^2} \right)^{1/2}$$

These relationships are only useful for

$$V_{ID} < 2(I_{SS} / \beta)^{1/2}$$

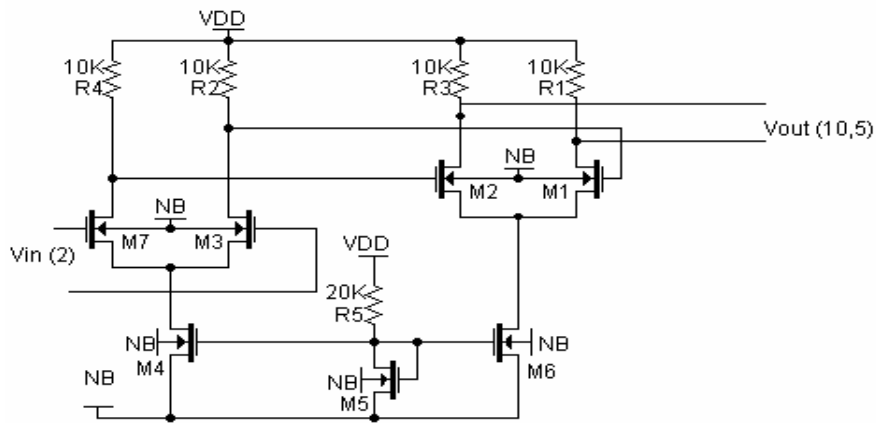
The transconductance of the amplifier is

$$g_m = \left( \frac{K_1 I_{SS} W_1}{4L_1} \right)^{1/2}$$

It is interested to note that as  $I_{SS}$  is increased the transconductance also increases.

### Proposed CMOS Differential Amplifier

The proposed differential amplifier is shown in Fig. 2. This circuit provides better differential gain and very small common mode gain. Thus, the CMRR of the proposed differential amplifier is extremely high. The transistor M3 and M7 forms the input stage of differential amplifier and M2 and M1 are for the output stage. Transistor M4 and M6 are used for current sink. The differential input is applied between the gate terminals of M3 & M7, the output can be taken across the drain of M1 and M2. The proposed structure is simulated for  $W/L=1$  in order to obtain the proper matching. Simulation in differential mode is carried out by taking step signal as input to gate terminal of M7 and the gate of M3 is ground. In order to analysis the common mode gate of M7 and M3 is shorted and then step input is applied for simulation.



**Figure 2:** Proposed CMOS Differential Amplifier.

### Simulation Results

The transient response for differential mode and common mode is shown in figure 2.1 and 3.1. This result shows the voltage at input terminal ( $V_2$ ) is amplified at output terminal ( $V(10,5)$ ) in differential mode and in common mode it is almost zero which shows that the amplifier has very high CMRR. Figure 2.2 and 3.2 shows the ac analysis of differential mode and common mode respectively.

The ac analysis plots the input and output noise of the circuit. This result shows that the circuit works properly up to 5 MHz frequency. After this frequency the performance of circuit is poor. Figure 2.3 and 3.3 shows the voltage transfer characteristic in differential mode and common mode configurations. The differential mode curve is linear for input voltage between -3.14 volts to +3.14 volts. So the present circuit is suitable for low voltage applications, whereas in common mode configuration the graph is non linear and noisy but in the range of nano volts. This shows that in common mode configuration, the output voltage is very-very small which also confers that the CMRR is very high. So this circuit can be used in design of low voltage high CMRR operational amplifier.

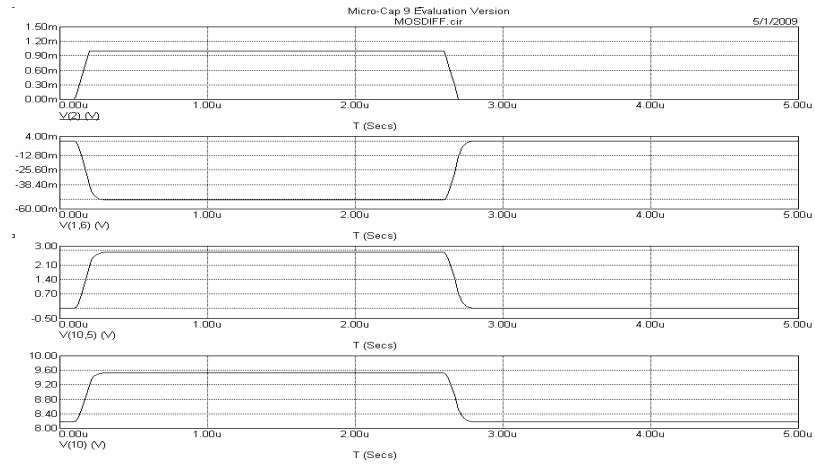


Figure 2.1: Transient analysis of proposed differential amplifier for differential mode.

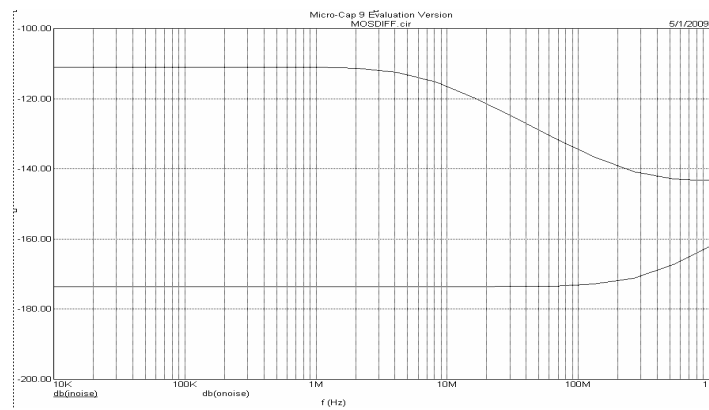


Figure 2.2: AC analysis of proposed differential amplifier for differential mode.

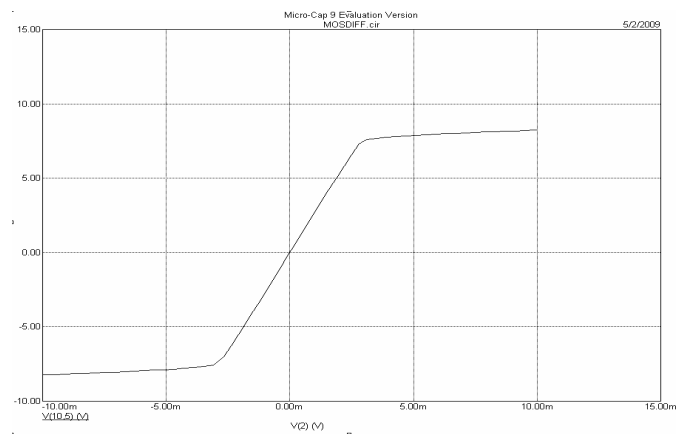


Figure 2.3: Voltage transfer characteristics of proposed differential amplifier for differential mode.

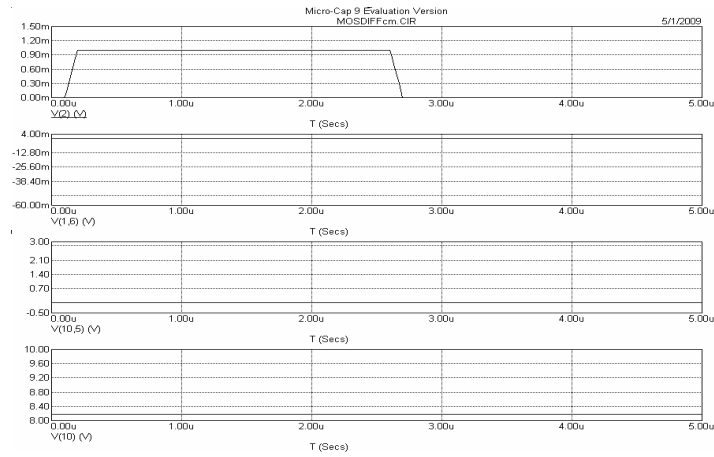


Figure 3.1: Transient analysis of proposed differential amplifier for common mode.

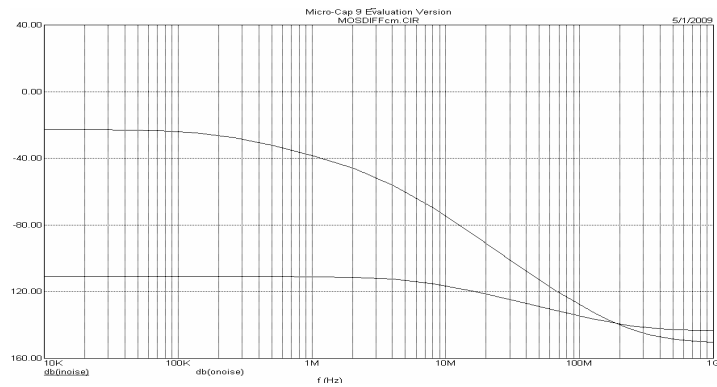


Figure 3.2: Voltage transfer characteristics of proposed differential amplifier for common mode.

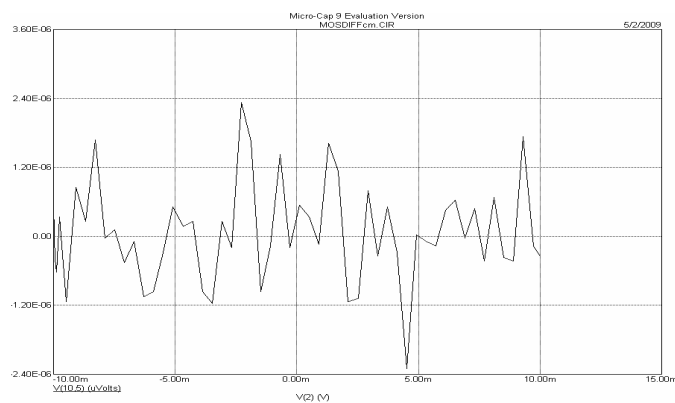


Figure 3.3: Voltage transfer characteristics of proposed differential amplifier for differential mode.

## **Conclusion**

In this paper a high performance CMOS differential amplifier circuit has been proposed. This circuit best suited for low voltage and high common mode rejection ratio (CMRR) applications. The input voltage can be applied between -3.14 volts to +3.14 volts and its performance is better up to 5 MHz. The circuit can be used in design of low voltage and CMRR operational amplifiers, Operational transconductance amplifiers, Voltage controlled oscillators (VCO).

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