A High Input Impedance Single-Ended Input to Balanced Differential Output Amplifier

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A high input impedance single-ended input to balanced differential output amplifier

Enrique M. Spinelli, Marcelo A. Haberman, Federico N. Guerrero and Pablo A. García

Abstract— A high input impedance circuit to convert a single-ended (SE) voltage to its differential counterpart is proposed. It allows setting the common-mode (CM) output voltage to a reference voltage v_R, while providing gain and a balanced output. The circuit, intended to work as sensor front-end for instrumentation applications, can be implemented by using available commercial devices, thus proving a solution for board-level design of instrumentation systems. It is based on operational amplifiers and can be tailored to specific requirements such as low noise levels, low bias currents or limited power supply voltages. The CM output voltage is controlled by a closed loop scheme, that results in a very good balance between circuit outputs.

In order to test the proposed topology, two single-ended to differential output amplifiers were built and tested: a low-noise amplifier that presents a noise of 70 nV_{RMS} in a 0.1 Hz-1 kHz bandwidth with a noise spectral density lower than 2 $nV/\sqrt{Hz}$ for higher frequencies, and a low input bias current amplifier for coaxial piezoelectric sensors.

***Index Terms*—differential circuits, conditioning circuits, instrumentation front-end.**

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I. INTRODUCTION

The present analog signal processing trend is towards fully-differential (FD) circuits, because they present a higher dynamic range than their single-ended counterparts, and because current high-resolution analog-to-digital converters (ADCs) have differential inputs. At the same time, FD circuits are well suited for low-voltage, single-supply operation and are insensitive to potential drops on the ground tracks, thus relaxing printed circuit board design.

The conversion of a SE voltage to a differential-mode (DM) one is depicted in Fig. 1. A ground-referenced input voltage v_i is converted to a differential output voltage as:

$$v_\mathrm{oD} = v_\mathrm{oP} - v_\mathrm{oN} = G v_\mathrm{i}\,, \tag{1}$$

$$v_\mathrm{oC} = 0.5(v_\mathrm{oP} + v_\mathrm{oN}) = v_\mathrm{R} \tag{2}$$

where v_{oD}, v_{oC} are the DM and common mode (CM) output voltages; v_{oP}, v_{oN} are the potentials at the output nodes P and N; v_R is the desired CM output voltage; and G the circuit gain. If (1) and (2) are fulfilled simultaneously, the voltages at output nodes v_{oP}, v_{oN} are given by:

$$v_\mathrm{oP} = v_\mathrm{R} + 0.5 G v_\mathrm{i}, \tag{3}$$

$$v_{oN} = v_R - 0.5\mathrm{G}v_i. \tag{4}$$

In this case the output is balanced, allowing to exploit the full span of ADCs and analog-processing blocks. Equations (1-4) consider that source and common-mode reference impedances Z_S and Z_R do not affect the output voltages. This implies high input impedances for both v_i and v_R.

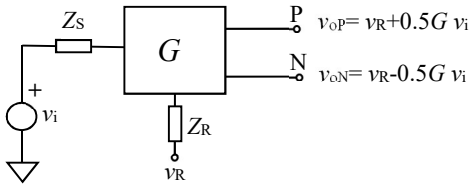

Fig. 1. Conversion of a single-ended voltage to a balanced differential output voltage. Potentials at output nodes P and N (v_{oP}, v_{oN}) verify (3) and (4).

When differential output sensors are used (e.g. Wheatstone bridges), all analog signal processing stages, including the front-end, can be implemented using FD circuits [1], but if the sensor provides a SE output, it should be converted to a differential output. In this case, typical instrumentation schemes include several SE analog signal conditioning stages, and signals are converted to DM voltages before being connected to a differential-input ADC [2], [3]. However, to take advantage of FD circuits, this conversion should be done as early as possible, i.e. at the front-end. Moreover, if possible, the conversion may be done on the sensor itself, as proposed in [4] for capacitive sensors. Special care should be taken when designing a front-end circuit, since it determines the main virtues and limitations of an instrumentation system. Frequent requirements for voltage-output sensors are: high input impedance, low input bias currents, low noise, and a significant gain to reduce noise contributions of subsequent stages. It is not easy to fulfill all these requirements simultaneously, but at board-level design, the selection of devices can be optimized for specific needs.

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The conversion of v_i to v_{oD}, v_{oC} given by (1, 2), can be implemented with a fully-differential operational amplifier (FDOA) by using the circuit of Fig.2 (a), where $G = R_2/R_1$. This is a simple and efficient solution, appropriate for conditioning SE signals for differential-input ADCs, but not to work as front-end, because it presents low input impedances. In order to remedy this, unity-gain buffers must be included at v_i and v_R inputs, thus adding noise and dc errors. Moreover, FDOAs are intended for high-speed applications and they are not well suited for high-precision low-power instrumentation circuits [2].

There are topologies based on operational amplifiers that allow performing the SE-to-differential conversion. Some of them, which combine inverting and noninverting amplifiers, are appropriate to generate balanced outputs for synchronous detectors, or lock-in-based systems [5], [6], but they present low input impedances. There are topologies and Integrated Circuits (IC) solutions for RF applications such as active baluns [7], but they are intended for 50 Ω systems and their gain depends on devices parameters as their transconductance.

High input impedance circuits based on noninverting amplifiers are commercially available, such as the LT6350 from Linear Technologies and the ADA4922 from Analog Devices. These devices, that implement the circuit of Fig.2 (b), are usually employed with unity gain ($G = 1$) but can be adapted to amplify v_i. They provide high input impedance for both v_i and v_R, and their common-mode output voltage v_{oC} fulfils equation (2), but their outputs are not balanced: the potential at node P ($v_{oP} = 0.5\mathrm{v_i}$) is a scaled version of v_i, while the potential at node N ($v_{oN} = 2v_R - 0.5Gv_i$) sets the common-mode voltage. The same situation arises with the solution proposed in [8] and shown in Fig.2 (c), which includes an OA at the input and a FDOA working in a closed-loop scheme. In all these cases, the output common-mode voltage v_{oC} equals v_R, but the differential output voltage, given by $v_{oD} = Gv_i - 2v_R$, does not fulfill (1) and the differential output is not "centred". Moreover, a dc voltage at v_R (i.e. for single supply circuits), produces undesired dc shifts in v_{oD}, thus wasting the input span of the subsequent stage.

A circuit that presents high input impedance and ensures the desired common-mode output voltage v_R by using a closed-loop scheme is described in [9]. The circuit shown in Fig.3 (a) provides a balanced output but it does not provide gain: the differential-mode output voltage v_{oD} is the attenuated version of the input signal v_i and is not appropriate for a front-end. The circuit herein proposed, replaces the DM attenuator by an amplifier, thus providing gain but also producing stability problems that will be described and solved in the following sections.

II. Proposed Circuit

The proposed circuit, depicted in Fig.3 (b), consists in a fully-differential amplifier [10] with an additional CM feedback. The CM output voltage v_{oC} is sensed by the averaging network $R_A - R_A$, compared against v_R, amplified, and then fed back to the input stage. If the open-loop gain A_3 of OA_3 is high enough, the output CM voltage equals v_R. Note that the traditional gain resistor R_1 was split in order to provide a CM injection node and, as it will be stated later, a resistor R_3 was added to provide a DM gain without affecting the CM behavior.

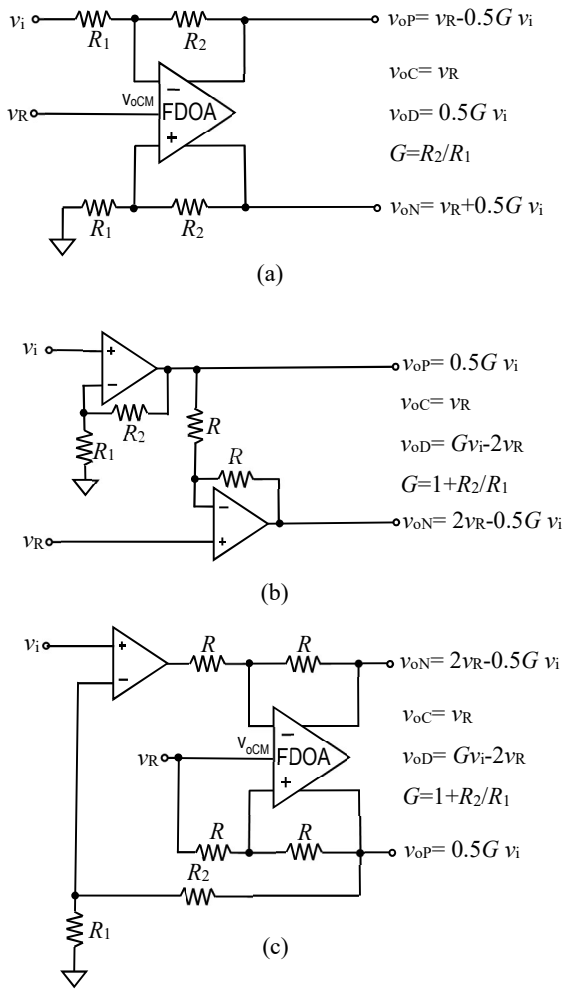

Fig. 2. Three circuits for converting single-ended to differential signals. Circuit (a) is based on Fully Differential Amplifiers (FDOA), circuit (b) on specific commercially available devices as LT6350, or ADA4922, and circuit (c) a combination of them proposed in [8].

Given that the circuit works with both common and differential-mode voltages, its analysis can be conducted using its CM and DM equivalent circuits [11, 12] shown in Fig.4(a) and Fig.4(b) respectively (see Appendix). Solving these circuits considering that the open-loop gains A_1, A_3 of OA_1, OA_3 are high enough, the output voltages for CM and DM voltages result

$$v_{\mathrm{oC}} = v_{\mathrm{R}} \tag{5}$$

$$v_{oD} = v_{iD}(1 + R_2/R_{13}) \tag{6}$$

where R_{13} denotes the parallel of $R_1, R_3/2$ and the DM and CM input voltages as function of v_i are $v_{\mathrm{iD}} = v_{\mathrm{i}}$; $v_{\mathrm{iC}} = v_i/2$. Then, replacing $v_{\mathrm{iD}} = v_i$ in (5) and (6), (7) results showing that the circuit amplifies and converts the SE voltage v_i into a DM one v_{oD} and sets the common-mode output voltage to v_R:

$$v_{oD} = G\, v_i \;;\; v_{oC} = v_R \tag{7}$$

$$G = (1 + R_2/R_{13}) \;\; ; \;\; R_{13} = R_1 \parallel R_3/2. \qquad (8)$$

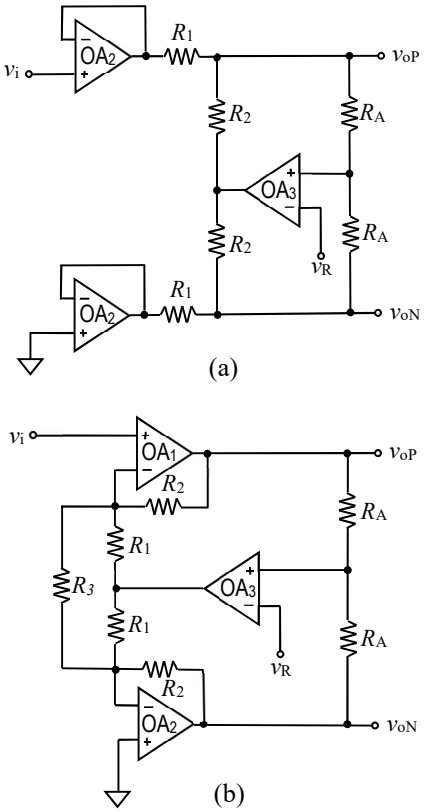

Fig. 3. (a) Circuit described in [9] that provides a balanced output, ensures a desired common mode output voltage v_R, but attenuates the input signal v_i. (b) Proposed circuit to correct this problem by including amplification in the first stage.

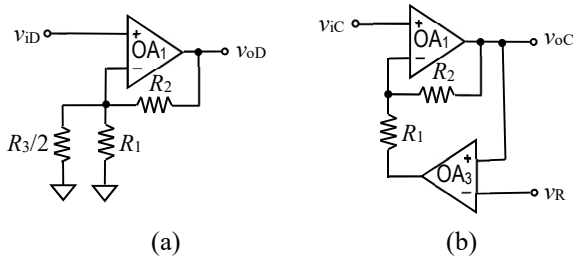

Fig. 4. Differential Mode (a) and Common Mode (b) equivalent circuits of the proposed topology.

A. Stability considerations

The proposed circuit is in fact fully-differential with one of its inputs grounded. The stability of FD circuits can be analysed by a space-state approach [13] or, as proposed in [14], by its CM and DM half-circuits. To ensure stability both the CM and DM half circuits must be stable.

Using internally compensated "unity-gain stable" OAs, the DM half circuit of Fig.4(a) is stable, (it is a simple non-inverting amplifier), but its CM counterpart of Fig.4(b) could present stability problems. The CM open-loop gain of this circuit is given by that of OA_3, plus additional gain and phase provided by the inverting amplifier composed by OA_1, R_1 and R_2, that leads to stability problems.

The strategy proposed to ensure stability is setting the ratio R_2/R_1 to a value around or below 0 dB and use for OA_3 an amplifier with a gain-bandwidth product (GBP_3) lower than that of OA_1 (GBP_1). Adopting $R_2/R_1 = 1$ and GBP_3 ten times lower than GBP_1, achieves an overall open-loop gain close to that of OA_3 for frequencies around the 0 dB crossing and below. Hence, the circuit inherits the stability features of OA_3 and works properly.

Figure 5 shows, in dashed line, a typical open-loop gain of OA_3 and, in solid grey line, the gain of the inverting amplifier composed by OA_1, R_1, R_2 for $R_2/R_1 = 1$ and $GBP_1 = 10\ GBP_3$. As can be seen in this figure, the gain of the inverting amplifier maintains its nominal value ($R_2/R_1 = 1$) beyond the 0 dB crossing of OA_3. Then, the overall common-mode open-loop gain, indicated in solid black line, agrees with that of OA_3.

A low R_2/R_1 ratio ($R_2/R_1 \leq 1$) allows achieving CM stability but limits the DM gain. This is solved by including a resistor R_3 in parallel to the R_1-R_1 network as Fig.3 (b) shows. This resistor provides DM mode gain without affecting CM stability, because it does not appear in the CM half-circuit of Fig.4 (b).

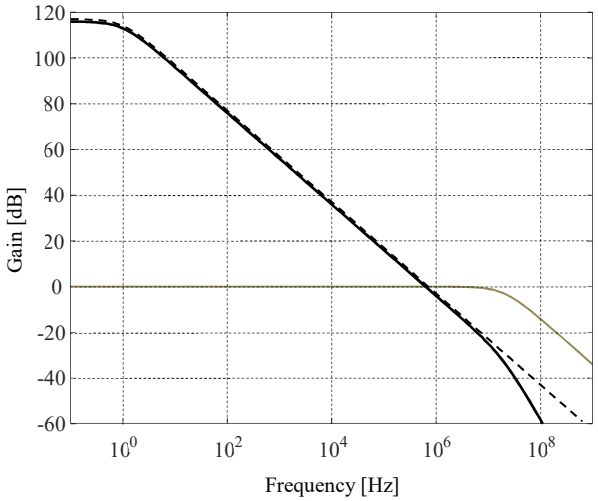

Fig. 5. CM open-loop gain. The gain of the closed-loop inverter amplifier for $R_2/R_1 = 1$ and $GBP_1 \gg GBP_3$ is indicated in grey, the open-loop gain of OA_3 in dashed line, and the resulting overall open-loop gain in black solid line.

B. Frequency response

Equations (5, 6, 7) assume OAs with ideally infinite open-loop gains A_1, A_3 and are valid for low frequencies. As frequency increases (5,6) becomes (Appendix):

$$V_{oD} = G_{DD}(s)V_i \qquad (9)$$

$$V_{oC} = 0.5\ G_{CC}(s)V_i + G_{RC}(s)V_R \quad , \qquad (10)$$

where capital letters denote Laplace transforms. Considering the conditions adopted for stability, ($R_2/R_1 = 1$ and $GBP_1 \gg GBP_3$), the transfer functions in (9) and (10) can be approximated by (Appendix):

$$G_{DD}(s) \approx \frac{A_1(s)}{1+A_1(s)/G} \; ; \; G_{CC}(s) \approx \frac{2}{1+A_3(s)};$$

$$G_{RC}(s) \approx \frac{A_3(s)}{1+A_3(s)} \quad (11)$$

If the open loop gains A_1 and A_3 are high enough, $G_{DD}(s) \approx G$, $G_{CC}(s) \approx 0$, $G_{RC}(s) \approx 1$. Therefore, equations (9-10) reduce to (12) and the circuit converts the SE voltage V_i into a differential output:

$$V_{oD} = GV_i \; ; \; V_{oC} = V_R \quad (12)$$

This expression is valid if the conditions $A_1/G \gg 1$ and $A_3 \gg 1$ are fulfilled, thus limiting the useful bandwidth of the proposed circuit. The amplifier gain, which depends on GBP_1, can be approximated by:

$$G_{DD}(s) \approx \frac{G}{1+s\tau_1} \; ; \; \tau_1 = \frac{G}{2\pi\, GBP_1}, \quad (13)$$

and its -3dB bandwidth is approximately

$$BW_{-3dB} \approx GBP_1/G \; . \quad (14)$$

C. Mismatch between v_{oP} and $-v_{oN}$

A figure of merit for single-ended to differential converters is the difference between its outputs v_{oP} and $-v_{oN}$. An advantage of the proposed circuit comes from the closed-loop control it performs over v_{oC} : the differential output is naturally balanced since any mismatches are reduced by the open-loop gain. However, as in any feedback loop, the control can only be as good as the estimation of the controlled variable. The high CM open-loop gain A_3 that OA_3 provides, ensures a null voltage at its input (virtual ground), and the middle point of the averaging network R_A-R_A equals v_R. Considering a mismatch in these resistors, and thus renaming them as R_{AP}, R_{AN}, the OA_3 virtual ground condition leads to:

$$v_{oP}\frac{R_{AN}}{R_{AN}+R_{AP}} + v_{oN}\frac{R_{AP}}{R_{AN}+R_{AP}} = v_R \; , \quad (15)$$

where v_R can be considered equal to 0 without loss of generality in order to analyse the unbalance between v_{oP} and $-v_{oN}$ thus yielding:

$$\frac{v_{oP}}{-v_{oN}} = \frac{R_{AP}}{R_{AN}} \; . \quad (16)$$

The amplitude error $\varepsilon_M = (-v_{oP}/v_{oN} - 1)$ [3], hence depends on R_{AP}, R_{AN} values:

$$\varepsilon_M = (R_{AP}/R_{AN} - 1) \, , \quad (17)$$

and using resistors with tolerance $t = \Delta R/R$, the worst case corresponds to $\varepsilon_M = 2t$.

However, as frequency increases and even with a perfect matching between R_{AP} and R_{AN}, amplitude and phase errors $\varepsilon_M, \varepsilon_P$ appear because of OA frequency responses. As it is described in the Appendix, their Laplace transforms V_{oP}, V_{oN} are given by:

$$V_{oP} = \frac{1}{2}\big(G_{CC}(s) + G_{DD}(s)\big)V_i \, , \quad (18)$$

$$V_{oN} = \frac{1}{2}\big(G_{CC}(s) - G_{DD}(s)\big)V_i \; . \quad (19)$$

Note that for low frequencies, $G_{DD} \gg G_{CC}$, and (18), (19) reduce to:

$$V_{oP} = -V_{oN} \, , \quad (20)$$

but as frequency increases V_{oP} and $-V_{oN}$ differs because of G_{CC}. The amplitude and phase errors $\varepsilon_M, \varepsilon_P$ considering dc effects described by (17) and the frequency responses given by (18) and (19) result:

$$\varepsilon_M(s) = 1 - \frac{R_{AP}}{R_{AN}}\frac{|G_{CC}(s)+G_{DD}(s)|}{|G_{CC}(s)-G_{DD}(s)|} \quad (21)$$

$$\varepsilon_P(s) = \phi\left(\frac{G_{CC}(s)+G_{DD}(s)}{G_{CC}(s)-G_{DD}(s)}\right) \quad (22)$$

III. Experimental Results

The proposed circuit can be built with standard operational amplifiers, thus allowing selecting commercially available devices to fulfil specific requirements, such as low noise, low bias current or low voltage power supplies, among others. Two prototypes were designed, built and tested: a low-noise amplifier and a low input bias current amplifier, both for converting single-ended sensor signals to differential-output voltages.

A. Low Noise Amplifier.

In order to implement a low-noise version of the proposed circuit, the ultra-low noise OA OPA2211 from Texas Instruments was selected for OA_1, OA_2. OP07 was used for AO_3, because it presents a $GBP_3 = 0.6$ MHz, lower enough than that of OA_1 ($GBP_1 = 80$ MHz), thus ensuring stability for a ratio $R_2/R_1 = 1$. A resistor $R_3 = 41\ \Omega$ was set to achieve, according to (7), a gain of 40 dB (100 times). In summary, component selection for the circuit of Fig. 3 (b) results:

$$OA_{1,2}\text{:OPA2211} \; ; \; OA_3\text{:OP07}$$

$$R_1\text{=2.1 k}\Omega,\ R_2\text{=2.1 k}\Omega,\ \ R_3\text{=41 }\Omega,\ \ R_A\text{=22 k}\Omega \quad (23)$$

In order to verify design equations (7) and (8), the circuit was tested with low frequency sinusoidal signals for v_i and dc voltages from 0 to 2.5 V for v_R . Figure 6 depicts the experimental setup. The sensor voltage v_i was simulated by a function generator and a resistive attenuator x101. This signal was applied to the proposed circuit, and its outputs v_{oP}, v_{oN} acquired using a digital oscilloscope Agilent MSO-X-2024A, resulting in the signals shown in Fig. 7. This case corresponds to $v_i = 10\,mV$, $v_R = 2.5\,V$ and the output voltages agree with those predicted by (7). The amplifier was powered by a ±5 V power supply.

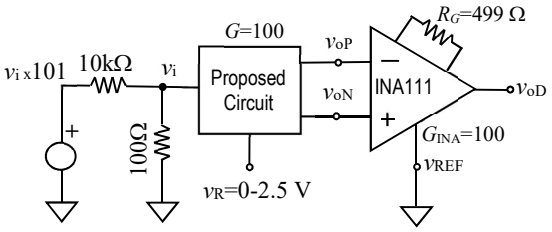

Fig. 6. Experimental setup. A function generator and an attenuator were used to simulate a SE sensor. The Instrumentation Amplifier was included to amplify v_{oD} for noise test purposes.

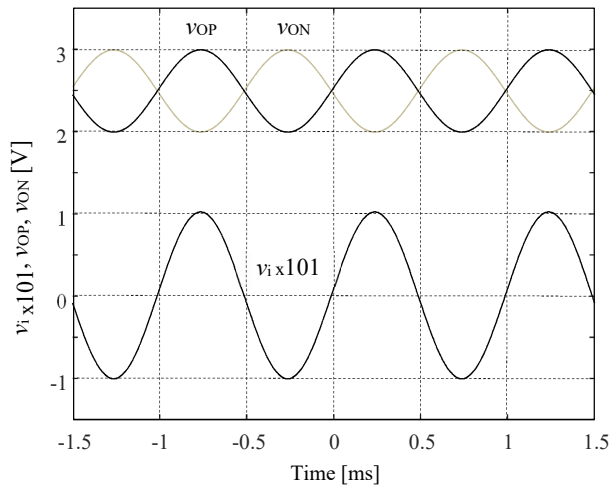

Fig. 7. Input and output signals obtained with $v_i = 10$ mV and $v_R = 2.5$ V.

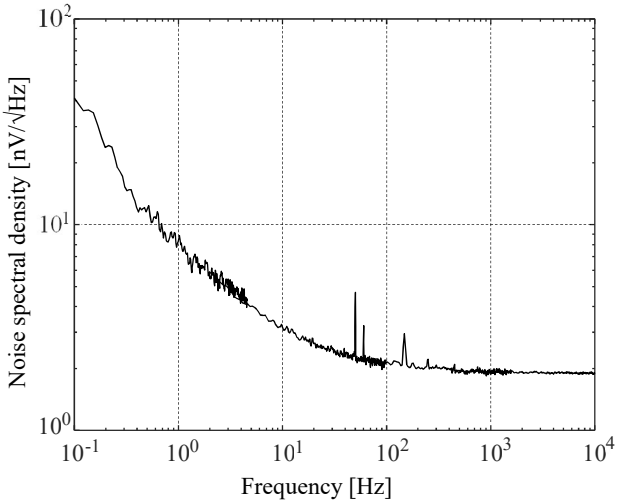

Fig. 8. Noise spectral density (input referenced) of the built prototype.

In order to evaluate noise features, an instrumentation amplifier INA111 was introduced. It converts v_{oD} to single-ended and amplifies it 100 times before feeding it to a Stanford Research 760 Spectrum Analyser. The INA111 presents a voltage noise of around $10\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ but, considering the gain $G = 100$ of the amplifier under test, it introduces an input-referred noise of $0.1\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ and does not contribute significantly to the overall noise.

The noise spectral density of the prototype with its input short-circuited is shown in Fig.8. The total noise in the 0.1 Hz -1 kHz bandwidth is 70 $\mathrm{nV_{RMS}}$ and the noise spectral density is lower than $2\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ for higher frequencies.

Frequency Response

The frequency response of the prototype was obtained experimentally up to 4 MHz using the function generator of the Agilent MSO-X-2024A oscilloscope as V_i and measuring the peak-to-peak amplitudes of V_{oP} , V_{oN} and V_{oD} with this same instrument. The results are shown in Fig. 9: V_{oP}/V_i in triangles, V_{oN}/V_i in squares and V_{oD}/V_i in circles. They present a good agreement with the frequency responses predicted by (13) and (20) considering $\mathrm{GBP_1} = 80$ MHz.

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Error between v_{oP} and v_{oN}

The circuit prototype was built with 1% tolerance metal-film resistors. Resistors R_{AP} and R_{AN} were measured by an Agilent 34401A multimeter resulting $R_{AP} = 22.092\ \mathrm{k\Omega}$, $R_{AN} = 22.062\ \mathrm{k\Omega}$ and an estimated amplitude error ε_M given by (17) of 0.13 %. Sinusoidal signals V_i were applied for frequencies from 10 to 300 kHz and the RMS value of the output voltages v_{OP}, v_{ON} measured by the same multimeter. The experimentally obtained magnitude error ε_M, shown in Fig. 10 with circles, presents a very good agreement with the theoretical error (solid line) predicted by (21) for the R_{AP}, R_{AN} circuit values and $GBP_1 = 80$ MHz and $GBP_3 = 0.6$ MHz.

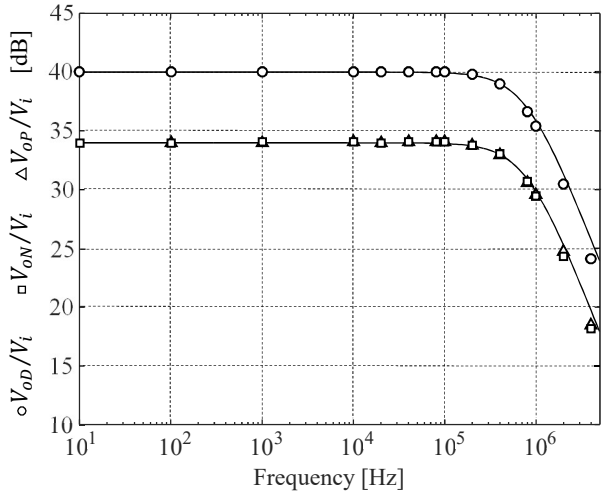

Fig.9. Experimental data showing the dependence with frequency of $G_{DD} = V_{oD}/V_i$ (in circles), $G_{oP} = V_{oP}/V_i$ (in triangles) and $G_{oN} = V_{oN}/V_i$ (in squares). Solid lines correspond to theoretical transfer functions G_{DD}, G_{oP} and G_{oN} predicted by (13) and (20).

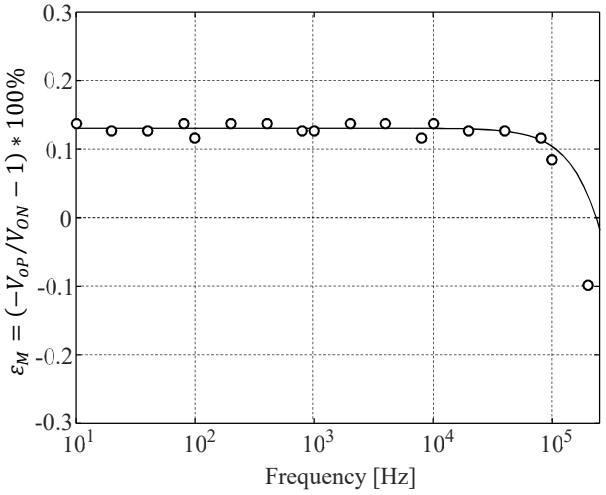

Fig. 10. Amplitude error ε_M between V_{oP} and V_{oN} as function of the frequency. Experimental data in circles and, in solid line, the ε_M predicted by (21) for the R_{AP}, R_{AN} prototype resistors values, $GBP_1 = 80$ MHz and $GBP_3 = 0.6$ MHz.

Phase error

The phase angle $\phi(V_{oP}, V_i)$ between V_i and V_{oP}, and $\phi(V_{oN}, V_i)$ between V_i and V_{oN}, were measured using the digital oscilloscope Agilent MSO-X-2024A. Using this data, the phase error ε_P was computed as stated in [3] as $\varepsilon_P = \phi(V_{oP}, V_i) - \phi(V_{oN}, V_i)$. The results, shown in Fig. 11, show a phase error below ±1 degree for frequencies up to 200 kHz, increasing to 5 degrees at 1 MHz and 15 degrees for 4 MHz. Taking into account that the circuit is intended to work as instrumentation front-end for low frequencies, this phase error does not impose a serious limitation. The experimental data present a good agreement with the theoretical curves given by (18) and (19) depicted by continuous lines in Fig. 11.

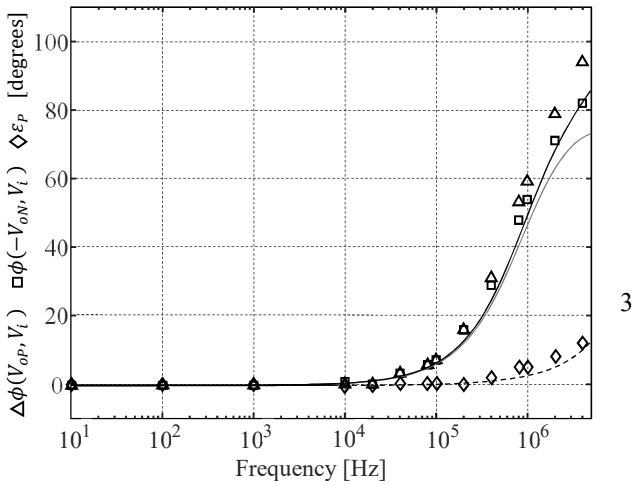

Fig. 11. Experimental phase angles: $\phi(V_{oP}, V_i)$ in triangles and $\phi(-V_{oN}, V_i)$ in squares. The continuous lines indicated the same phase angles as predicted by theoretical equations (18) in black and (19) in gray. The phase error ε_P, defined as the difference between these measured angles, is indicated in diamonds, and in dashed line its predicted value according to Eq. (22).

B. A Low Input Bias Current Amplifier.

As another example of the proposed circuit, a low input bias current amplifier, was built to work as front-end for a coaxial piezoelectric Vibromax™ sensor. In this case, the OA TLC2202, that presents an input bias current of 1 pA and a $GBP_1 = 2$ MHz, was selected for OA_1 and OA_2. To ensure stability, a ratio $R_2/R_1 = 1$ was set and the OA LM308, with a compensation capacitance of C_F=1 nF ($GBP_3 = 100$ kHz), was used for OA_3. The resistor R_3 was set to 41 Ω to achieve a gain of 40 dB. The component selection for the circuit of Fig. 3 (b) results:

$OA_{1,2}$: TLC2202 ; OA_3: LM308, C_F=1 nF

$$R_1 = 2.1\ k\Omega,\ R_2 = 2.1\ k\Omega,\ R_3 = 41\ \Omega,\ R_A = 22\ k\Omega \qquad (24)$$

1. Figure 12 shows the experimental setup and Fig.13 the output voltages v_{oP}, v_{oN} when soft taps were applied on the sensor. Note the balanced output and the common mode output voltage $v_{oC} = v_R = 2.5$ V.

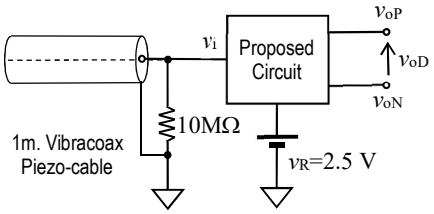

Fig. 12. Experimental setup used to test the proposed circuit working as front-end for a piezo-electric cable sensor.

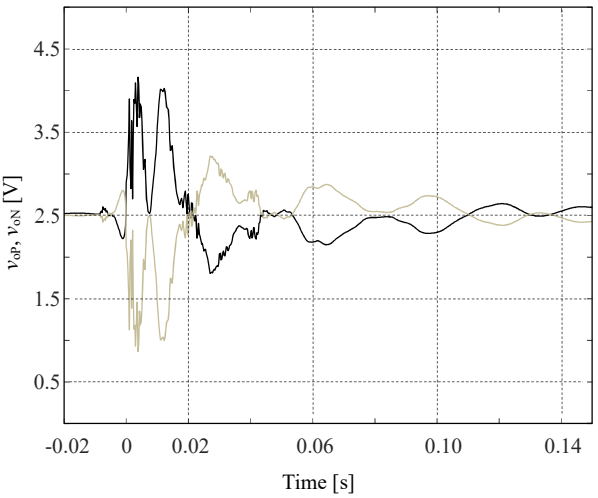

Fig. 13. Differential output voltage produced by a coaxial Vibromax™ piezo-cable.

IV. Conclusion

A circuit for a single-ended input to differential-output amplifier was proposed. It allows setting the differential gain G and the common-mode output voltage v_{oC} independently. The circuit, shown in Fig.3 (b), presents a high input impedance as the previous circuits of Fig.2 (b) and (c), but its differential output is centred with respect to the desired common-mode output, thus exploiting the complete voltage range of the circuit. It also implies an improvement over the circuit of Fig.3 (a), which provides a balanced output but not gain. Furthermore, if the gain of the proposed amplifier is high enough its input-referred noise corresponds to that of OA_1 and OA_2, whereas for the circuit of Fig.3 (a) this noise is amplified by the attenuation ratio $1 + R_1/R_2$.

The proposed scheme allows obtaining an output voltage with a very good balance that only depends on the ratio of the two resistances that estimate v_{oC} from the circuit output. This feature is achieved thanks to the closed-loop control performed over the common-mode voltage, that also introduces a limitation: the circuit works properly as long as its open-loop gain is high enough, this means for frequencies bellow the OAs gain-bandwidth products.

The proposed circuit, intended to work as front-end in board-level designs, can be implemented using standard OAs. This allows tailoring circuit features to particular requirements as low-noise or low bias current applications. The presented design equations were experimentally validated on an ultra-low

noise single-ended input to differential-output amplifier and were also applied to the design of a front-end for a coaxial piezoelectric sensor.

V. Appendix I- DM and CM half circuits

The proposed topology is comprised of a fully-differential circuit excited by a single-ended source as shown in Fig. 14. One of its inputs is $v_{iP} = v_i$ whereas the other is $v_{iN} = 0$. Assuming a perfectly symmetric circuit, CM input voltages only produce CM voltages, while DM input voltages just produce DM voltages. In this condition, the effects of CM and DM signals can be analysed separately by using CM and DM half-circuits [11, 12].

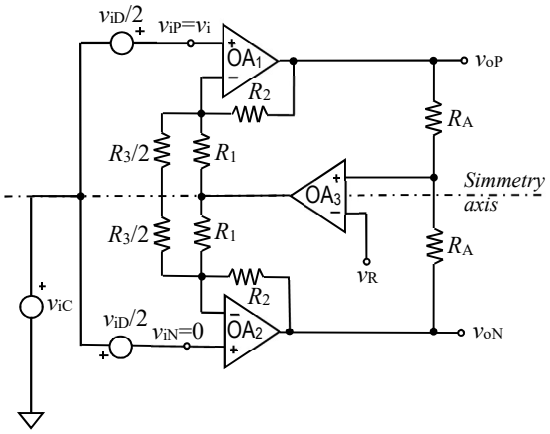

Fig. 14. Proposed circuit with its symmetry axis indicated in "dashed-point" line.

A. Differential Mode half circuit

The proposed circuit has a symmetry axis, indicated in "dash-dot" line in Fig. 14, that splits it into two identical semi-circuits. Note that resistor R_3 was split to achieve symmetry while preserving circuit behaviour. Each node in the upper side has its homologue in the lower side. When a pure DM input voltage is applied, potentials of the upper semi-circuit nodes vary opposite to those from their lower semi-circuit counterparts. Then, the potential on the symmetry axis remains unaltered: it can be considered an isopotential line for DM signals. Their effects can thus be analysed using the DM half circuit which is obtained grounding all the nodes of the semi-circuit on the symmetry axis. This circuit can be used to compute the DM output voltage v_{oD} that a DM input voltage v_{iD} produces.
The DM half circuit is shown in Fig. 4 (a). Solving this circuit, the transfer function $G_{DD}(s)$ between the Laplace Transforms of DM output voltages V_{oD} and DM input voltages V_{iD} results:

$$G_{DD}(s) = \frac{V_{oD}}{V_{iD}} = \frac{A_1(s)}{1+\frac{A_1(s)}{1+R_2/R_{13}}} = \frac{A_1(s)}{1+\frac{A_1(s)}{G}} \quad , \tag{25}$$

where A_1 denotes the open-loop gain of OA_1. Assuming that an internally compensated OA with a gain-bandwidth product GBP_1 is used, and a significant nominal gain $G = (1 + R_2/R_{13}) \gg 1$ is adopted, $G_{DD}(s)$ can be approximated by:

$$G_{DD}(s) \approx \frac{G}{1+s\tau_1} \;;\; \tau_1 = \frac{G}{2\pi\, GBP_1} \tag{26}$$

Common Mode half-circuit

If a pure CM voltage v_{iC} is applied to a symmetrical circuit, the potentials of the upper semi-circuit nodes show the same variation as those of their lower semi-circuit counterparts. Then, no current flows through any impedances connecting the semi-circuits and these elements do not have any effect for CM voltages, as occurs with R_3 in the circuit of Fig. 3 (b). The CM half circuit, which allows analysing the CM output voltage v_{oC} that a CM input voltage v_{iC} produces, is obtained omitting these impedances. Special care must be taken when bisecting the circuit of Fig. 14, because the key of the proposed scheme is the feedback provided by OA_3, that only works for CM voltages. In this case, the middle point of the averaging network $R_A - R_A$ adopts a potential equal to the CM output voltage v_{oC} and can be replaced by a short circuit for the CM half circuit. The sensed CM voltage v_{oC} is compared against v_R, amplified by OA_3, and fed back to the middle point of the $R_1 - R_1$ network. Hence, the output of OA_3 affects both outputs v_{oP} and v_{oN} equally, thus producing CM voltages. Finally, taking into account these conditions, the CM half circuit of Fig. 4 (b) results. It allows obtaining the CM output voltage V_{oC} that the inputs V_{iC} and V_R produce:

$$V_{oC} = \frac{1+R_2/R_1}{1+\frac{1+R_2/R_1}{A_1(s)}+A_3(s)R_2/R_1} V_{iC} + \\ + \frac{A_3(s)R_2/R_1}{1+\frac{1+R_2/R_1}{A_1(s)}+A_3(s)R_2/R_1} V_R \quad , \tag{27}$$

where A_3 denotes the open-loop gain of OA_3. This expression states two transfer functions: $G_{CC}(s) = V_{oC}/V_{iC}$ and $G_{RC}(s) = V_{oC}/V_R$. In the conditions stated for circuit stability ($GBP_1 \gg GBP_3$ and $R_2/R_1 = 1$), they can be approximated by:

$$G_{CC}(s) \approx \frac{2}{1+A_3(s)} \;;\; G_{RC}(s) \approx \frac{A_3(s)}{1+A_3(s)} \tag{28}$$

If both open-loop gains A_1, A_3, are high enough: $G_{CC}(s) \approx 0$, $G_{RC}(s) \approx 1$ and the CM output voltage v_{oC} exclusively depends on v_R. The gain G_{CC} is very small for low frequencies but increases as A_3 decreases, tending to a maximum value of 2. Since OA_3 is working with unity feedback, the G_{CC} frequency response corresponds to that of OA_3 working as a unity-gain buffer. Finally, considering that the input voltages V_{iC}, V_{iD} are related to the input voltage V_i of the proposed amplifier by:

$$V_{iC} = V_i/2 \;;\; V_{iD} = V_i \;. \tag{29}$$

Their CM and DM outputs are:

$$V_{oD} = G_{DD}(s)V_i \;, \tag{30}$$

$$V_{oC} = 0.5\, G_{CC}(s)V_i + G_{RC}(s)V_R \;, \tag{31}$$

where G_{DD}, G_{CC} and G_{RC} are the transfer functions given by (26) and (28)

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