A Fast-Settling CMOS Op Amp for SC Circuits with 90-dB DC Gain

KLAAS BULT AND GOVERT J. G. M. GEELEN

Abstract—**A technique is presented that combines the high-frequency behavior of a single-stage op amp with the high dc gain of a multistage design. Bode-plot measurements show a dc gain of 90 dB and a unity-gain frequency of 116 MHz (16-pF load). Settling measurements with a feedback factor of 1/3 show a fast single-pole settling behavior corresponding to a closed-loop bandwidth of 18 MHz (35-pF load) and a settling accuracy better than 0.03%.**

I. Introduction

SPEED and accuracy are two of the most important properties of analog circuits; however, optimizing circuits for both aspects leads to contradictory demands. In a wide variety of CMOS analog circuits such as switched-capacitor filters [1]–[3], algorithmic A/D convertors [4], sigma–delta convertors [5], sample-and-hold amplifiers, and pipeline A/D convertors [6], speed and accuracy are determined by the settling behavior of operational amplifiers. Fast settling requires a high unity-gain frequency and a single-pole settling behavior of the op amp, whereas accurate settling requires a high dc gain.

The realization of a CMOS operational amplifier that combines high dc gain with high unity-gain frequency has been a difficult problem. The high-gain requirement leads to multistage designs with long-channel devices biased at low current levels, whereas the high unity-gain frequency requirement calls for a single-stage design with short-channel devices biased at high bias current levels.

There have been several circuit approaches to circumvent this problem. Cascoding is a well-known means to enhance the dc gain of an amplifier without degrading the high-frequency performance. The result is a dc gain which is proportional to the square of the intrinsic MOS transistor gain $g_m \cdot r_o$. In modern processes with short-channel devices and an effective gate-driving voltage of several hundreds of millivolts, the intrinsic MOS transistor gain $g_m \cdot r_o$ is about 20–25 dB, resulting in a dc gain of the cascoded version of about 40–50 dB. In most cases, however, this is not enough [1], [7], [8].

Dynamic biasing of transconductance amplifiers [9]–[11] was one of the first approaches reported to combine high dc gain with high settling speed. In this approach the bias current is decreased, either as a function of time during one clock period [9], [10] or as a function of the amplitude of the input signal [11], resulting in a higher dc gain at the end of the settling period. This decreases the unity-gain frequency, which makes the last part of the settling very slow.

In [12] a triple-cascode amplifier has been implemented where the gain is proportional to $(g_m \cdot r_o)^3$. This approach has two significant disadvantages. First, every transistor added in the signal path introduces an extra pole in the transfer function. In order to obtain enough phase margin, the minimum load capacitance has to be increased, resulting in a lower unity-gain frequency. Second, each transistor reduces the output swing by at least the effective gate-driving voltage.

In [7] positive feedback is used to enhance the gain of an amplifier. This approach, however, is limited by matching. A gain enhancement of about 16 dB is reported. For high-Q, high-frequency switched capacitor filters, this is not enough. Even a moderate Q of 25 and a maximum deviation of 1% requires a minimum op-amp gain of 74 dB [1], [7]. Therefore, we aim at a dc gain of at least 80 dB combined with a unity-gain frequency of 200 MHz.

Future processes with submicrometer channel length will enable us to realize even higher unity-gain frequencies. However, the intrinsic MOS transistor gain $g_m \cdot r_o$ will then be lower [13], and the problem of achieving enough dc gain becomes even more severe. This paper presents an op amp based on the gain-boost principle [14]–[16]. Although first presented in 1979, no op-amp design using this technique has been reported yet. We show here a new implementation of the gain-boost technique, allowing for a larger output voltage swing and an extension of the technique boosting the dc gain to even higher values. Furthermore, we show that when using this technique in the design of an op amp, care should be taken to avoid instability or slow settling components, and present a design guideline for optimal settling behavior. Finally, we show dc, ac, as well as settling measurement results.

In Section II the principle of this technique is explained. Section III deals with the high-frequency behavior. Section IV discusses the optimization towards fast

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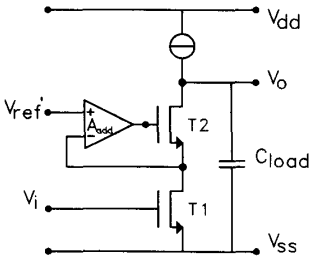

Fig. 1. Cascoded gain stage with gain enhancement.

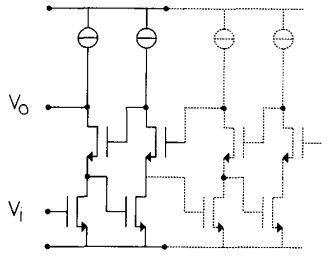

Fig. 2. Repetitive implementation of gain enhancement.

settling behavior. In Section V the circuit implementation is presented, and in Section VI the measurement results will be given.

II. Gain Boosting

The gain-boost technique is based on increasing the cascoding effect of $T2$ by adding an additional gain stage as shown in Fig. 1. This stage reduces the feedback from the output to the drain of the input transistor. Thus, the output impedance of the circuit is increased by the gain of the additional gain stage, A_{add}:

$$R_{\text{out}} = (g_{m2}r_{o2}(A_{\text{add}}+1)+1)r_{o1} + r_{o2}. \quad (1)$$

In this way, the dc gain can be increased several orders of magnitude:

$$A_{o,\text{tot}} = g_{m1}r_{o1}(g_{m2}r_{o2}(A_{\text{add}}+1)+1). \quad (2)$$

Section III deals with the high-frequency behavior of this circuit and discusses what happens if the gain of the additional stage decreases as a function of frequency.

If the additional stage is implemented as a cascode stage, the gain-enhancement technique as described above can also be applied to this additional stage. In this way, a *repetitive* implementation of the gain enhancement technique can be obtained as shown in Fig. 2. The limitation on the maximum voltage gain is then set by factors such as leakage currents, weak avalanche, and thermal feedback. The implementation of the additional stage is discussed in Section V.

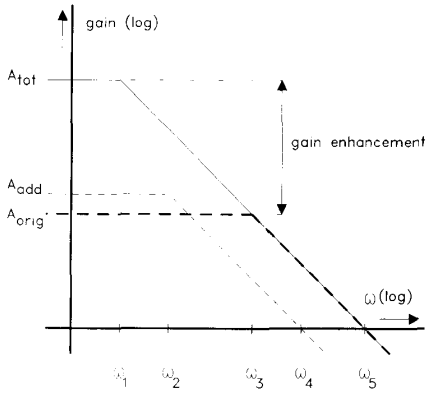

Fig. 3. Gain Bode plots of the original cascoded gain stage (A_{orig}), the additional gain stage (A_{add}), and the improved cascoded gain stage (A_{tot}).

III. High-Frequency Behavior

In this section we discuss the high-frequency behavior of the gain-enhanced cascode stage of Fig. 1. It is shown that for a first-order roll-off, the additional stage need not be fast with respect to the unity-gain frequency of the overall design.

In Fig. 3, a gain Bode plot is shown for the original cascoded gain stage (A_{orig}), the additional gain stage (A_{add}), and the improved cascoded gain stage of Fig. 1 (A_{tot}). At dc, the gain enhancement $A_{\text{tot}}/A_{\text{orig}}$ equals approximately $[1 + A_{\text{add}}(0)]$, according to (2). For $\omega > \omega_1$, the output impedance is mainly determined by C_{load}. This results in a first-order roll-off of $A_{\text{tot}}(\omega)$. Moreover, this implies that $A_{\text{add}}(\omega)$ may have a first-order roll-off for $\omega > \omega_2$ as long as $\omega_2 > \omega_1$. This is equivalent to the condition that the unity-gain frequency (ω_4) of the additional gain stage has to be larger than the 3-dB bandwidth (ω_3) of the original stage, but it can be much lower than the unity-gain frequency (ω_5) of the original stage. The unity-gain frequencies of the improved gain stage and the original gain stage are the same.

From the above, to obtain a first-order roll-off of the total transfer function, the additional gain stage does not have to be a fast stage. In fact, this stage can be a cascoded gain stage, with smaller width and nonminimal-length transistors biased at low current levels. Moreover, as the additional stage forms a closed loop with $T2$, stability problems may occur if this stage is too fast. There are two important poles in this loop. One is the dominant pole of the additional stage and the other is the pole at the source of $T2$. The latter is equal to the second pole ω_6 of the main amplifier. For stability reasons, we set the unity-gain frequency of the additional stage lower than the second-pole frequency of the main amplifier. A safe range for the location of the unity-gain frequency ω_4 of the additional stage is given by

$$\omega_3 < \omega_4 < \omega_6. \quad (3)$$

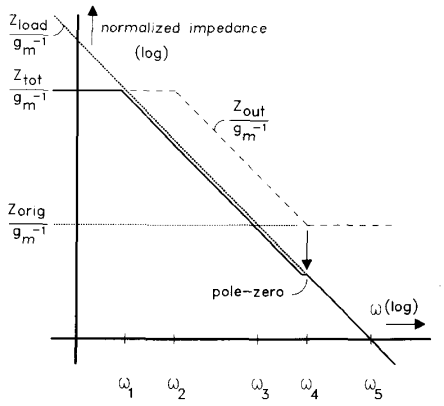

Fig. 4. Normalized output impedance as a function of frequency.

This can easily be implemented. From the above, we may conclude that the repetitive usage of the gain-enhancement technique yields a *decoupling* of the op-amp dc gain and unity-gain frequency.

IV. Settling Behavior

In this section, the settling behavior of the gain-enhanced cascoded amplifier stage is discussed. It is shown that a single-pole settling behavior demands a higher unity-gain frequency of the additional stage than a simple first-order roll-off in the frequency domain requires, as discussed in the previous section. The reason for this is the presence of a closely spaced pole and zero (doublet).

From (1), the gain-enhancement technique increases the output impedance Z_{out} by a factor approximately equal to $(A_{add}+1)$. The gain of the additional stage, A_{add}, decreases for frequencies above ω_2 (Fig. 3) with a slope of -20 dB/decade. For frequencies above ω_4, A_{add} is less than one, and the normal output impedance Z_{orig} of a cascode stage without gain enhancement remains. This is shown in Fig. 4. Also shown is the impedance of the load capacitor Z_{load} and the parallel circuit that forms the total impedance Z_{tot} at the output node. A closer look at this plot reveals that a doublet is present in the plot of the total output impedance near ω_4. It is well known that a doublet can seriously degrade the settling behavior of an op amp due to a slow settling component [17].

Our approach here is to make this "slow" settling component fast enough. If the time constant of the doublet, $1/\omega_{pz}$, is smaller than the main time constant, $1/\beta\omega_{unity}$, of the closed loop with feedback factor β, the settling time will not be increased by the doublet. This situation is achieved when the unity-gain frequency of the additional stage is higher than the -3-dB bandwidth of the circuit. On the other hand, for reasons concerning stability, the unity-gain frequency must be lower than the second-pole frequency of the main amplifier as indicated by (3). This results in the "safe" area for the unity-gain

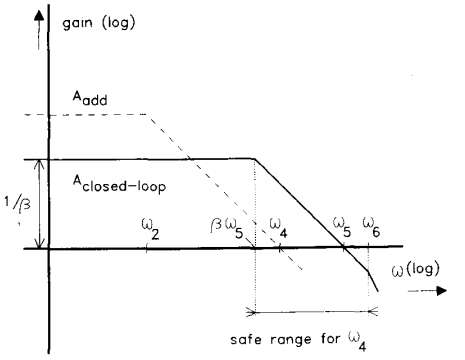

Fig. 5. The "safe" range for the unity-gain frequency of the additional stage.

frequency of the additional stage:

$$\beta\omega_5 < \omega_4 < \omega_6 \tag{4}$$

as shown in Fig. 5. Note that this safe area is smaller than given by (3). A satisfactory implementation, however, is still no problem because the load capacitor of the additional stage, which determines ω_4, is much smaller than the load capacitor of the op amp, which determines ω_5.

V. Circuit Implementation

In this section, the implementations of the main op amp and the additional gain stages are discussed. The main stage is a folded-cascode amplifier [2]. The simplest implementation of the additional stage is one MOS transistor [14]–[16]. We have chosen a cascode version because of its high gain and the possibility of repetitive usage of the gain-enhancement technique as discussed in Section II. The input stage design of the additional amplifier is determined by the common-mode range requirement, which is close to the V_{ss} if a large output swing is required. As a consequence, a folded-cascode structure with PMOS input transistors is chosen for the additional amplifier in Fig. 1. To realize very high output impedance, the current source in Fig. 1 is also realized as a cascoded structure with an additional gain stage. This implementation allows for an output voltage swing as large as 4.2 V at a 5-V supply. A fully differential version (Fig. 6) has been integrated in a 1.6-μm CMOS process. The two input transistors connected to V_{cm} have been added to control the common-mode bias voltage at the output. The die photograph of Fig. 7 clearly shows that the additional stages are much smaller in chip area than the main op amp.

VI. Measurement Results

As it is very difficult to measure differentially at high frequencies with sufficient accuracy, all measurements have been performed single ended. The output node of the additional amplifier in Fig. 1 is connected to a bond-

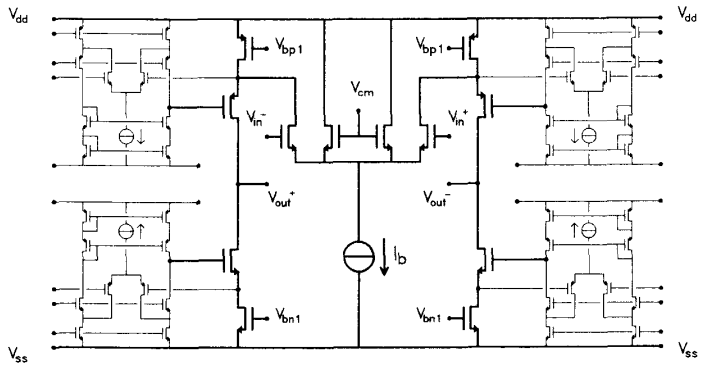

Fig. 6. Complete circuit diagram of the op amp.

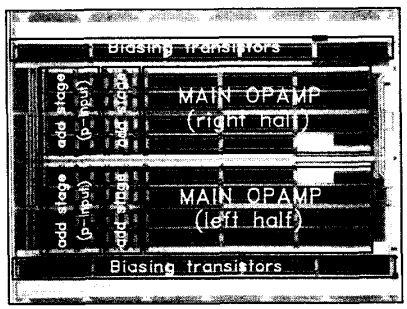

Fig. 7. Die photograph of the op amp.

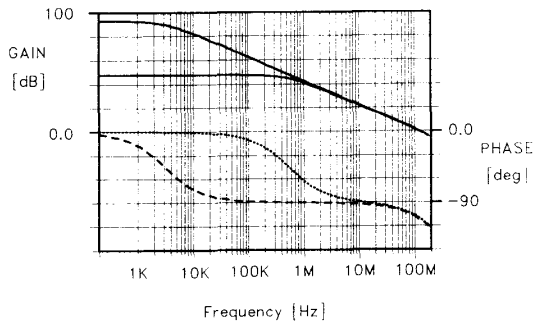

Fig. 8. Results of gain and phase measurements both with and without gain enhancement.

ing pad in order to be able to switch off the gain-enhancement technique. Results of gain measurements both with and without gain enhancement are shown in Fig. 8. A dc-gain enhancement of 45 dB was measured without affecting the gain or phase for higher frequencies, resulting in a total dc gain of 90 dB combined with a unity-gain frequency of 116 MHz. This shows a good agreement with Fig. 3. Note that when measured differentially, both the dc gain and the unity-gain frequency should be twice as high. The settling behavior is measured according to Fig. 9 by applying a step, ΔV_i, at the input. The resistors are needed for dc biasing of the op amp and have no influence on the settling behavior. The error signal V_- at the op-amp input, and the output signal V_o are shown in Fig. 10. In Fig. 10(a) and (b), $\Delta V_o = 1$ V, which is small enough to avoid slewing. With the gain enhancement switched off, an error signal of 4.75 mV is measured after settling (Fig. 10(a)). This corresponds to the measured dc gain of 46 dB. Switching on the gain enhancement reduces the error signal to a value smaller than 0.1 mV (Fig. 10(b)), which corresponds to a dc gain higher than 80 dB. In Fig. 9 the feedback factor β is given by

$$\beta = C_f/(C_i + C_p + C_f) \tag{5}$$

whereas the unity-gain frequency is given by

$$\omega_{\text{unity}} = g_m \frac{(C_i + C_p + C_f)}{C_o(C_i + C_p + C_f) + (C_i + C_p)C_f}. \tag{6}$$

The theoretical settling time constant τ can now be calculated:

$$\tau = \{C_p + C_i + C_o + (C_i + C_p)\cdot C_o/C_f\}/g_m. \tag{7}$$

In Fig. 9, $C_o = 20$ pF and $C_p = C_i = C_f = 22$ pF, which is relatively large due to probing. With $g_m = 0.012$ A/V, $\omega_{\text{unity}} = 54$ MHz, and $\beta = 1/3$, $\tau = 8.8$ ns. Settling to 0.1% takes $7\tau = 62$ ns and corresponds to a 1-mV error at the output. With a feedback factor $\beta = 1/3$, this corresponds to an error signal of $V_- = 0.33$ mV. From Fig. 10(b) the measured settling time for 0.1% accuracy is 61.5 ns, which is in agreement with the theory. In Fig. 11, the measured relative settling error is shown as a function of time. During the entire settling process, each 10-dB increase in settling accuracy takes approximately 8 ns. This clearly shows that there are no slow settling components. In Fig. 10(c) and (d), $\Delta V_o = 4$ V, $C_i = 33$ pF, and $C_f = 15$ pF, showing a normal slewing behavior and a large output swing. The main measured characteristics of the op amp are summarized in Table I.

VII. Conclusions

A technique is presented which decouples the dc gain and unity-gain frequency of an op amp. A very high dc gain can be achieved in combination with any unity-gain frequency achievable by a (folded-) cascode design.

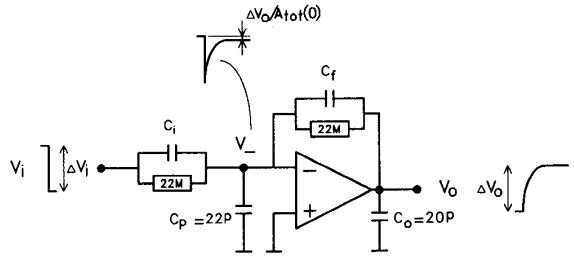

Fig. 9. Scheme for measuring settling behavior.

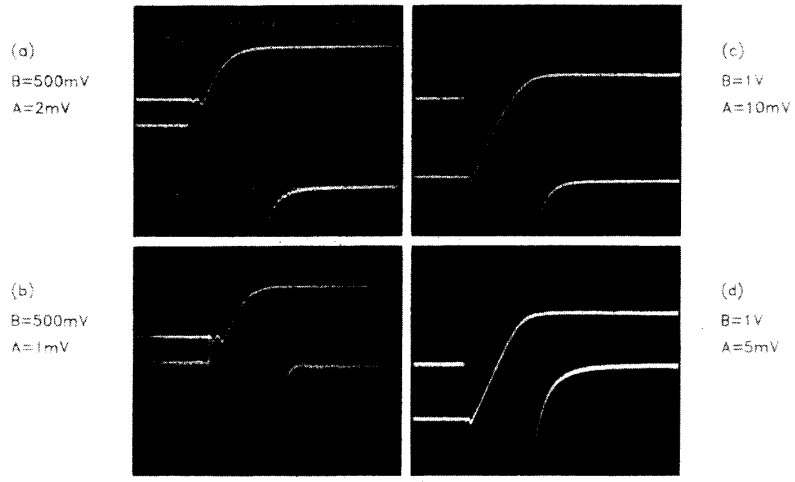

Fig. 10. Settling measurement results. The output signal (upper trace B) and the error signal at the op-amp input (lower trace A) with: (a) $\Delta V_o = 1$ V and gain enhancement switched off, (b) $\Delta V_o = 1$ V and gain enhancement switched on, (c) $\Delta V_o = 4$ V and gain enhancement switched off, and (d) $\Delta V_o = 4$ V and gain enhancement switched on.

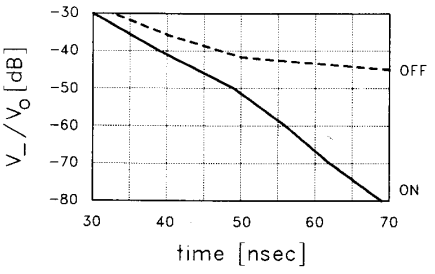

Fig. 11. Measured relative settling error as a function of time for both with and without gain enhancement.

TABLE I
MAIN CHARACTERISTICS OF THE OP AMP

Gain enh.	on	off
DC-gain	90dB	46dB
Unity-gain freq.	116MHz	120MHz
Load cap.	16pF	16pF
Phase margin	64deg.	63deg.
Power cons.	52mW	45mW
Output-swing	4.2V	4.2V
Supply voltage	5.0V	5.0V

With this technique an op amp was realized in a standard 1.6-μm CMOS process that had a dc gain of 90 dB together with a unity-gain frequency of 116 MHz. The op amp shows one-pole roll-off and a single-pole settling behavior.

This technique does not cause any loss in output voltage swing. At a supply voltage of 5.0 V an output swing of about 4.2 V is achieved without loss in dc gain.

The advantages above are achieved with only a 30% increase in chip area and a 15% increase in power consumption.

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