# A 1-GHz Bipolar Class-AB Operational Amplifier with Multipath Nested Miller Compensation for 76-dB Gain

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***Abstract*—A 1-GHz operational amplifier with a gain of 76 dB while driving a 50-$\Omega$ load is presented. The equivalent input noise voltage is as low as 1.2 nV/$\sqrt{}$Hz. This combination of extremely high bandwidth, high gain, and low noise is the result of a three-stage all-n-p-n topology combined with a multipath nested Miller compensation. Using 10-GHz $f_T$ n-p-n transistors, the realizable bandwidth could be of the order of 2–3 GHz. However, bond-wire inductances restrict the useful bandwidth to 1 GHz. The amplifier occupies an active area of 0.26 mm$^2$ and has been realized in the bipolar part of a 1-$\mu$m BiCMOS process.**

***Index Terms*— Analog integrated circuits, bipolar integrated circuits, frequency compensation, HF amplifiers, operational amplifiers.**

## I. Introduction

TRADITIONALLY, wideband amplifiers consist either of stages with local feedback, which reduce accuracy, or use feedforward techniques that introduce pole-zero doublets, which deteriorate the settling behavior [1]. Recently reported multistage compensation techniques, such as multipath nested Miller compensation [2], allow frequency compensation of cascaded gain stages with minimal reduction in bandwidth compared to single-stage amplifiers. This enables amplifiers to combine high gain and high bandwidth. This paper describes how multipath nested Miller compensation makes the realization of a general-purpose high-gain 1-GHz operational amplifier possible.

To obtain the highest possible bandwidth, only the device with the highest transit frequency, the n-p-n transistor, should be applied in the high-frequency signal path. Even in modern complementary processes, the n-p-n is a factor three faster than its p-n-p counterpart. Because of the fundamental difference in mobility of electrons and holes, this will not change in the future. Therefore, very wideband amplifiers should exploit an all-n-p-n topology [3]. For low frequencies, however, p-n-p transistors can be used. They are especially useful for obtaining the necessary dc levelshifts between n-p-n stages. A basic topology of a two-stage amplifier is shown in Fig. 1. The two-stage opamp has a gain only of the order of 40 dB when driving 50 $\Omega$. Darlington transistors cannot be allowed in the output stage at extremely high bandwidths. Therefore, a third stage is necessary in combination with multipath nested Miller compensation. A theoretical elaboration of the multipath nested Miller compensation for low-ohmic loads and very high frequencies is presented in this paper.

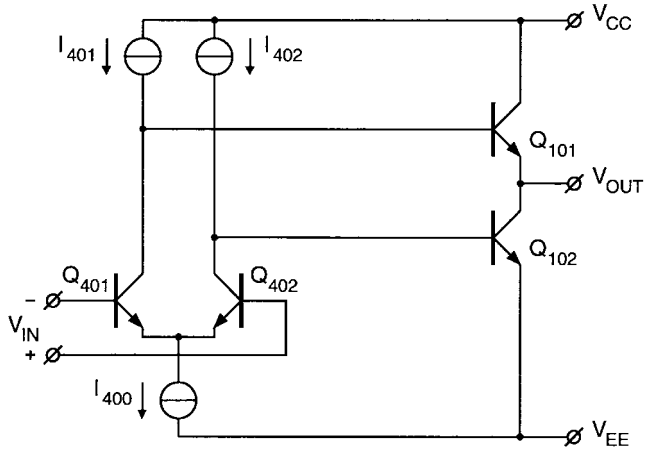


Fig. 1. Basic two-stage all-n-p-n topology.

The paper starts by examining the two-stage all-n-p-n topology in Section II. In Section III, the implementation of the all-n-p-n topology in a three-stage circuit using multipath nested Miller compensation is discussed. The complete circuit, the realization of the opamp, and the measurement results are presented in Section IV. Special attention is paid to the packaging and bonding of the amplifier. Finally, in Section V the conclusions are drawn.

## II. Two-Stage All-n-p-n Topology

### A. Principle of Operation

A simplified schematic of a two-stage all-n-p-n opamp is shown in Fig. 1. It consists of an n-p-n input stage $Q_{401}$, $Q_{402}$ and an n-p-n output stage $Q_{101}$, $Q_{102}$. Apart from the fact that only n-p-n transistors are used, the high-frequency behavior benefits from the very simple topology. Because the output stage consists of a follower $Q_{101}$ and an inverter $Q_{102}$, the output stage can be directly driven by the differential input stage $Q_{401}$, $Q_{402}$ without a mirror, which would have added

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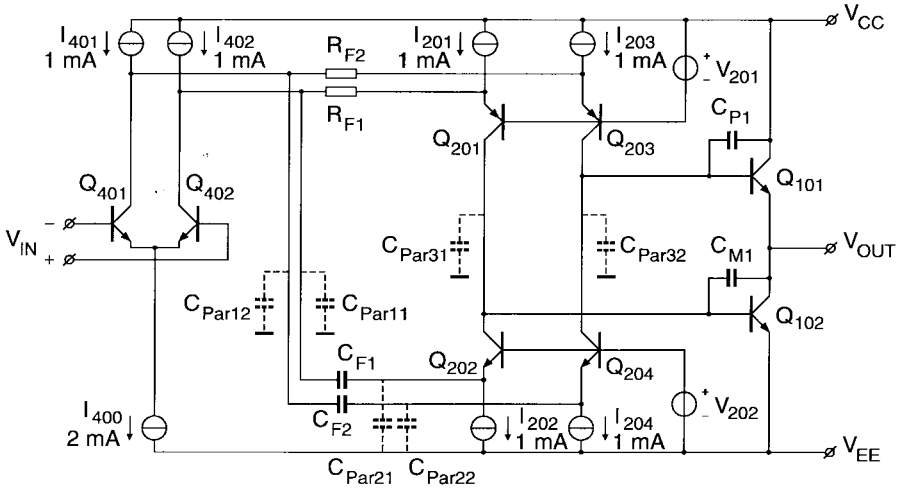



Fig. 2. Two-stage all-n-p-n opamp with level shift.

delay and parasitics. A practical implementation, however, gives rise to three main problems.

1) The common-mode input voltage of a general-purpose building block like an opamp should be independent of the biasing voltages of the output stage and the output voltage. To achieve this, a level-shift circuit between input stage and output stage is necessary. For the sake of good high-frequency behavior, the level shift should not introduce much delay and parasitic capacitance.
2) The output stage is asymmetric, with one output transistor being connected as a follower and the other output transistor as an inverter. To achieve good signal behavior, the push and pull output transistors should be balanced.
3) To be able to deliver sufficient output current without consuming a lot of quiescent current, the output stage should be biased in class AB. The class-AB control circuit should prevent cutoff of the output transistors and should not interfere with the signal path, in order to prevent delay and distortion.

### *B. Level Shift*

To realize a wideband level shift, p-n-p cascodes $Q_{201}$, $Q_{203}$ for low-frequency signals can be combined with n-p-n cascodes $Q_{202}$, $Q_{204}$ for high-frequency signals, when we split the input signal by RC all-pass networks $R_{F1}$, $C_{F1}$ and $R_{F2}$, $C_{F2}$ as shown in Fig. 2. If the turnover frequency $f_{TO} = 1/R_{F1}C_{F1}$ is much lower than the transit frequency of the p-n-p transistor, the response of the circuit is flat up to the transit frequency of the n-p-n transistor [3] without pole-zero doublets. Unfortunately, several nonidealities influence the behavior of the level shift. For low frequencies, the transfer function is attenuated by the current gain of the p-n-p transistor which is much lower than the current gain of the n-p-n transistor. For high frequencies, the transfer function is influenced by parasitic capacitances $C_{Par11}$–$C_{Par32}$, which are shown in Fig. 2. $C_{Par11}$ and $C_{Par12}$ attenuate the high-frequency transfer function. $C_{Par21}$ and $C_{Par22}$ are connected across the base-emitter capacitance of $Q_{202}$ and $Q_{204}$, and thus reduce the bandwidth. $C_{Par31}$ and $C_{Par32}$ load the output stage.

### *C. Output Stage Balancing*

The output transistors with their parasitics are shown in Fig. 3. Their nature is completely different because one is connected as a follower and the other as an inverter. However, it is possible to make the transfer function of the output transistors equal by making the capacitance across the base-collector junctions equal by adjusting $C_{P1}$, assuming the output transistors are driven by ideal current sources [3]. When we perform a detailed calculation, the transfer function from input voltage $V_{\text{in}}$ to output voltage $V_{\text{out}}$ of the follower is found as shown below in (1) where

- $j$ complex unit;
- $\omega$ frequency;
- $g_1$ transconductance of the output transistors;
- $g_2$ transconductance of the input stage;
- $\beta_F$ current gain of the output transistors;
- $R_L$ load resistance;
- $r_{be}$ small-signal base-emitter resistance of the output transistors;
- $C_{be}$ base-emitter capacitance of the output transistors;
- $C_L$ load capacitance.

$C_{P1}$ also includes the base-collector capacitance $C_{bc}$ and $C_{Par31}$. The transfer function of the inverter is found as shown

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{g_2\beta_F R_L\left(1 + j\omega\,\dfrac{C_{be}}{g_1}\right)}{1 + j\omega(r_{be}C_{be} + R_LC_L + r_{be}C_{P1} + R_LC_{P1} + \beta_F R_LC_{P1}) + (j\omega)^2 r_{be}R_L(C_{be}C_L + C_{be}C_{P1} + C_LC_{P1})} \tag{1}$$

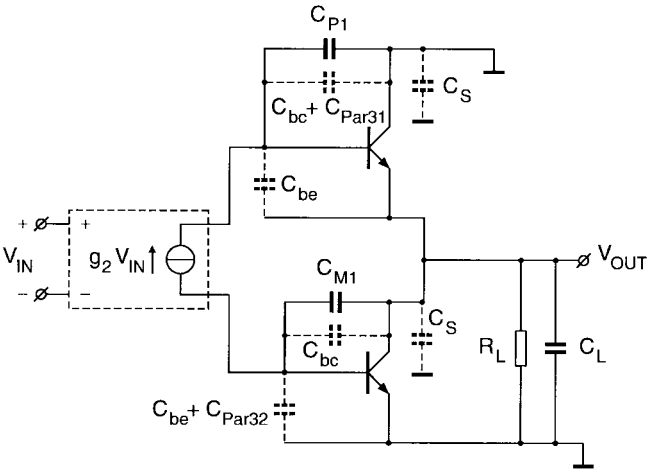



Fig. 3. Combination of output transistors.

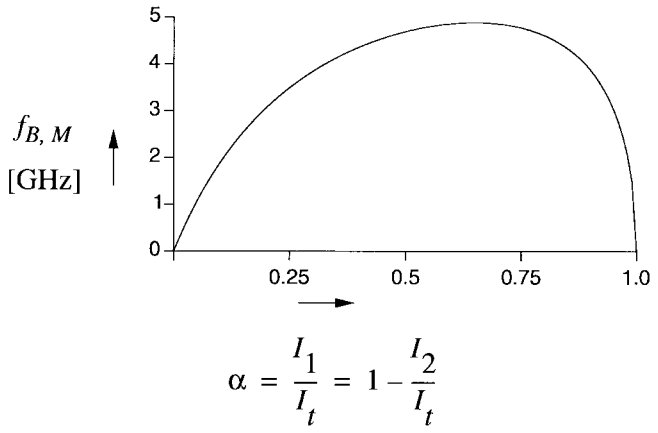



Fig. 4. Bandwidth $f_{B,M}$ of a Miller compensated opamp as a function of the fraction $\alpha$ of the total current $I_t$ used as bias current $I_1$ of the output stage.

in (2), at the bottom of the page, where $C_{M1}$ is the Miller capacitor. $C_{M1}$ also includes $C_{bc}$ and, $C_{be}$ includes $C_{Par32}$.

When both transistors are biased at the same current and all capacitors of the follower have been made equal to the capacitors of the inverter, the only difference that remains is that the zero of the follower is positioned in the left half-plane and of the inverter in the right half-plane. Due to the phase shift of the right half-plane zero, the bandwidth of the inverter is smaller than the bandwidth of the follower.

The unity-gain frequency $\omega_0$ for both circuits is found as

$$\omega_0 = \frac{g_2}{C_{M1}} \cdot \frac{1}{1 + \frac{1}{g_1 R_L} + \frac{1}{g_1 R_L}\frac{C_{be}}{C_{M1}} + \frac{1}{\beta_F}\frac{C_L}{C_{M1}}}. \quad (3)$$

The first part of (3) is well known and shows that the output transistor operates as an ideal integrator with input current generated by $g_2$ and integration capacitor $C_{M1}$. The second part is a correction term expressing the influence of the loop gain $g_1 R_L$ and capacitances $C_{be}$ and $C_L$. In the case of this design, where the load capacitance is small, the only necessity is that the loop gain $g_1 R_L$ must be large. Because of the low resistive load of 50 Ω, this means that the output transistors need a bias current of at least several milliamps. Then the correction term is close to one, and the bandwidth is accurately set by $g_2$ and $C_{M1}$

$$\omega_0 = \frac{g_2}{C_{M1}}. \quad (4)$$

When the output stage operates near the quiescent state, both output transistors work together. The transfer function of the combination has three poles. However, when the follower and inverter transistors are balanced, mainly by adjusting $C_{P1}$ so that $C_{P1} + C_P$ equals $C_{M1}$, one pole is exactly cancelled by a zero at

$$\omega_{PZ} = \frac{1}{r_{be}(C_{M1} + C_{be})}. \quad (5)$$

And the transfer function is found as shown in (6), at the bottom of the page. The zero disappears when $C_{be}$ equals $C_{M1}$. Then, the current through $C_{be}$ compensates the feedforward current through $C_{M1}$, thus removing the right half-plane zero much in the same way as with multipath Miller zero cancellation [4]. Because of the high bias current in the output stage, $C_{be}$ is of the order of $C_{M1}$ and the zero is shifted to very high frequencies. In cases where $C_{be}$ is too small, a resistor can be inserted in series with $C_{M1}$ to shift the zero to high frequencies. This has the disadvantage that the position of the zero changes as a function of the output current. However, due to the large quiescent current in the output stage, the inserted resistor is relatively small. Therefore, even at high output currents, the zero is situated at very high frequencies.

If $g_1 R_L$ is large, the unity-gain frequency of the combination is equal to that of the separate output transistors as given by (4). Thus, the signal behavior in quiescent state is the same as in the situation where high output currents are handled. This assures good high-frequency linearity.

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{-g_2\beta_F R_L\left(1 - j\omega\frac{C_{M1}}{g_1}\right)}{1 + j\omega(r_{be}C_{be} + R_L C_L + r_{be}C_{M1} + R_L C_{M1} + \beta_F R_L C_{M1}) + (j\omega)^2 r_{be}R_L(C_{be}C_L + C_{be}C_{M1} + C_L C_{M1})} \quad (2)$$

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{2g_2\beta_F R_L\left(1 + j\omega\,\frac{C_{be} - C_{M1}}{g_1}\right)}{1 + j\omega(r_{be}C_{be} + R_L C_L + 2R_L C_{M1} + r_{be}C_{M1} + 2\beta_F R_L C_{M1}) + (j\omega)^2 r_{be}R_L(C_{be}C_L + 2C_{be}C_{M1} + C_L C_{M1})} \quad (6)$$

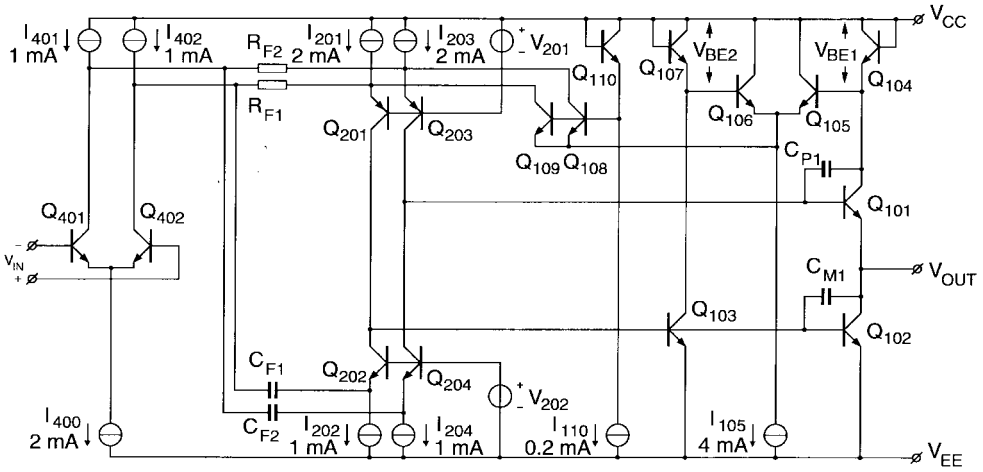



Fig. 5. Two-stage 1-GHz opamp.

### D. Frequency Compensation

The Miller capacitor $C_{M1}$ which is used to split the two poles of the two-stage opamp apart [5], [6] has to be chosen such that the unity-gain frequency is below the second pole. The second pole of the combination is given by

$$\omega_{p2} = \frac{g_1}{C_{be} + \dfrac{C_L}{2} + \dfrac{C_{be}C_L}{2C_{M1}}} \approx \frac{g_1}{C_{be} + \frac{1}{2}C_L}. \tag{7}$$

An opamp is usually compensated such that the poles reach Butterworth positions when a unity-gain feedback is applied. This is obtained when the unity-gain frequency of the open-loop response is positioned a factor of two below the second pole corresponding to a phase margin of 60°. Combining (4) and (7) gives the value of the Miller capacitor as

$$C_{M1} = 2\frac{g_2}{g_1}\left(C_{be} + \frac{1}{2}C_L\right). \tag{8}$$

The next step is choosing the bias current in the input stage and output stage in such a way that the highest bandwidth is reached. From (6), the bandwidth is found as

$$\omega_{B,M} = \sqrt{\frac{g_1 g_2}{\frac{1}{2}C_{be}C_L + \frac{1}{2}C_L C_{M1} + C_{be}C_{M1}}}. \tag{9}$$

Substituting (8) in (9) and writing the transconductance as a function of the current gives

$$\omega_{B,M} = \frac{1}{V_T}\frac{1}{\sqrt{C_{be}C_L}}\sqrt{\frac{I_1 I_2}{2 + \dfrac{I_2}{I_1}\left(2 + 2\dfrac{C_{be}}{C_L} + \dfrac{1}{2}\dfrac{C_L}{C_{be}}\right)}} \tag{10}$$

where $V_T$ is the thermal voltage, $I_1$ the bias current of the output transistors, and $I_2$ the tail current of the input stage. We can relate the bias currents of the input stage and the output stage to the total current $I_t$ by introducing a parameter $\alpha$

$$I_1 = \alpha I_t = \alpha(I_1 + I_2). \tag{11}$$

Further, the current dependency of the base-emitter capacitance can be introduced, and finally, the bandwidth as a function of $\alpha$ can be maximized. The bandwidth as a function of $\alpha$ is plotted in Fig. 4 for a total current $I_t$ of 7 mA and a load capacitance of 1 pF. The maximum is around $\alpha = 0.65$. This means that 65% of the current should be used to bias the output stage and 35% to bias the input stage. We need about 5 mA bias current in the output stage to obtain sufficient loop gain in the Miller loop and about 1 mA bias current per transistor in the input stage, because of noise considerations. Fortunately, this is close to the optimum. The resulting unity-gain frequency is 3.4 GHz using a Miller capacitor of 0.9 pF.

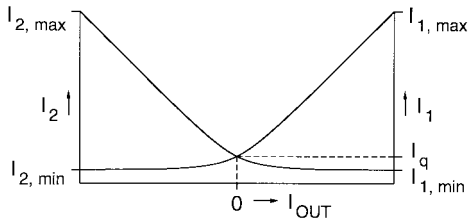



Fig. 6. Class-AB characteristic.

### E. Class-AB Control

The class-AB biasing of the output transistors can be easily implemented by using a feedback loop that controls the collector currents in such a way that no transistor ever cuts off [7]. An all-n-p-n version of the class-AB control circuit [2] is depicted in the complete two-stage opamp schematic given in Fig. 5. The transistors $Q_{107}$ and $Q_{104}$ sense the collector currents of the output transistors. A minimum selector $Q_{105}$, $Q_{106}$ drives transistors $Q_{108}$ and $Q_{109}$. These transistors complete the control loop by subtracting two equal currents from the inputs of the output stage through the level-shift stages. The result is that the lower of the collector currents of both output transistors stays above a certain minimum collector current, and thus cutoff of the output transistors is avoided. This is illustrated by the class-AB characteristic plotted in Fig. 6. The all-n-p-n circuit with minimum current control assures excellent linearity from low frequencies up to very high frequencies.

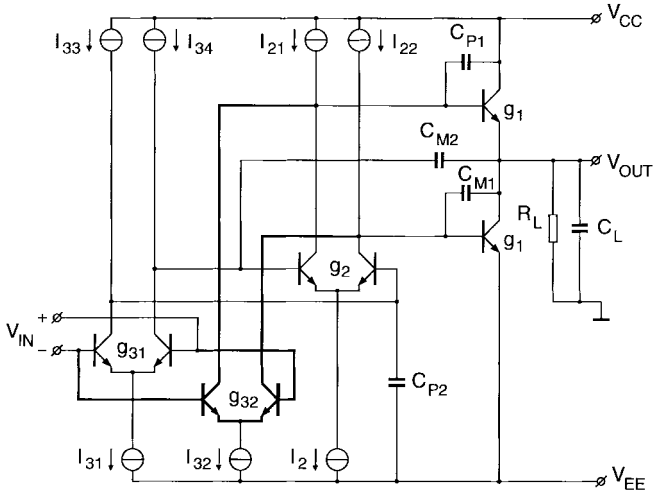



Fig. 7. Simplified three-stage amplifier with multipath nested Miller compensation.

### F. Gain

The dc gain $A_0$ of the two-stage opamp from (6) is found as

$$A_0 = 2g_2\beta_F R_L. \tag{12}$$

Using 1 mA bias current for the input transistors and with a load resistance of 50 $\Omega$ and a $\beta_F$ of 80, the dc gain equals 44 dB. This is not acceptable for a general-purpose wideband opamp. Therefore, a stage has to be added. By adding this stage between input stage and the level-shift stage, the noise contribution of the class-AB control transistors is reduced by the gain of this intermediate stage. This improves the noise performance by a factor of $\sqrt{2}$. The three-stage circuit is discussed in the next section.

## III. Three-Stage Multipath Opamp

In the previous section, we discussed a two-stage all-n-p-n topology for realizing a 1-GHz opamp. It was found that the gain was not sufficient. Therefore, a stage is added. To maintain a high bandwidth, the resulting three-stage circuit has to be efficiently compensated. A well-known solution is to apply nested Miller compensation [8]. However, when the outer Miller capacitor is inserted, the bandwidth has to be reduced by a factor of two compared to the two-stage Miller compensated circuit in order to avoid complex poles. To avoid the bandwidth reduction of nested Miller compensation, multipath nested Miller compensation has been devised [2], [9], taking advantage of the high gain of the three-stage circuit and the high bandwidth of the two-stage circuit. The circuit is shown in Fig. 7. To gain insight into the operation of multipath nested Miller compensation at very high frequencies, we calculate the transfer function of the circuit. By straightforward nodal analysis, the transfer function of the three-stage nested Miller circuit without feedforward is found. Omitting the less important terms results in (13), shown at the bottom of the page, where

- $g_2$ transconductance of the intermediate stage;
- $g_{31}$ transconductance of the input stage;
- $\beta_{F1}$ current gain of the output transistors;
- $\beta_{F2}$ current gain of the intermediate-stage transistors;
- $r_{be1}$ small-signal base-emitter resistance of the output transistors;
- $r_{be2}$ small-signal base-emitter resistance of the intermediate-stage transistors;
- $C_{be1}$ base-emitter capacitance of the output transistors;
- $C_{M2}$ second Miller capacitor.

The transfer function of the two-stage feedforward path is given by (14), shown at the bottom of the page, where $g_{32}$ is the transconductance of the feedforward input stage and $C_{be2}$ the base-emitter capacitance of the intermediate-stage transistors. The total transfer function is given by the summation of both transfer functions. A Bode plot of the low-frequency path and the feedforward path of a multipath nested Miller compensated amplifier is shown in Fig. 8. Because the feedforward signal goes through the same circuit as the low frequency signal, all the poles of the feedforward path are equal to the poles of the low-frequency path. The only difference between both paths is the dc gain and the zeros. The two zeros of nested Miller compensation are caused by direct signal transfer through the Miller capacitors. One of these zeros is in the right half-plane and the other one in the left half-plane. It is interesting to see that the feedforward path does not add a zero, but the left half-plane zero is moved to

$$\omega_z = \frac{1}{r_{be2}(C_{be2} + \frac{1}{2}C_{M2})}. \tag{15}$$

When this zero is positioned correctly, the feedforward path takes over exactly at the second pole $\omega_{p2}$, thus extending the $-20$ dB/dec slope toward the third pole $\omega_{p3}$. This is obtained when the unity-gain frequency of the low-frequency

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{2g_{31}\beta_{F1}\beta_{F2}R_L\left[1 + j\omega\dfrac{C_{be1} - C_{M1}}{2g_1} - (j\omega)^2\dfrac{C_{M2}}{g_2}\dfrac{C_{be1} + C_{M1}}{2g_1}\right]}{1 + j\omega(\beta_{F1}\beta_{F2}R_L C_{M2}) + (j\omega)^2 g_1 r_{be1} r_{be2} R_L C_{M1} C_{M2} + (j\omega)^3 r_{be1} r_{be2} R_L C_{M1} C_{M2}\left(C_{be1} + \dfrac{C_L}{2} + \dfrac{C_{be1}}{C_{M1}}C_L\right)} \tag{13}$$

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{2g_{32}\beta_{F1}R_L\left[1 + j\omega r_{be2}\left(C_{be2} + \dfrac{C_{M2}}{2}\right)\right]\left(1 + j\omega\dfrac{C_{be1} - C_{M1}}{2g_1}\right)}{1 + j\omega(\beta_{F1}\beta_{F2}R_L C_M 2) + (j\omega)^2 g_1 r_{be1} r_{be2} R_L C_{M1} C_{M2} + (j\omega)^3 r_{be1} r_{be2} R_L C_{M1} C_{M2}\left(C_{be1} + \dfrac{C_L}{2} + \dfrac{C_{be1}}{C_{M1}}C_L\right)} \tag{14}$$

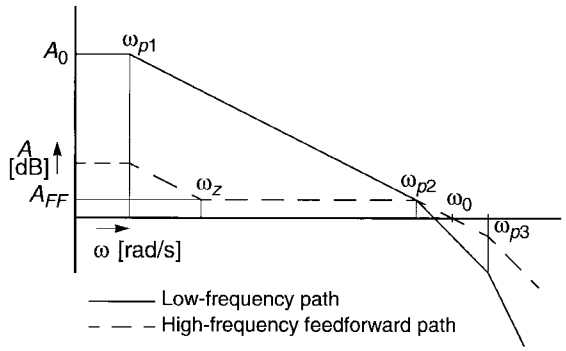



Fig. 8. Frequency response of three-stage amplifier with multipath nested Miller compensation.

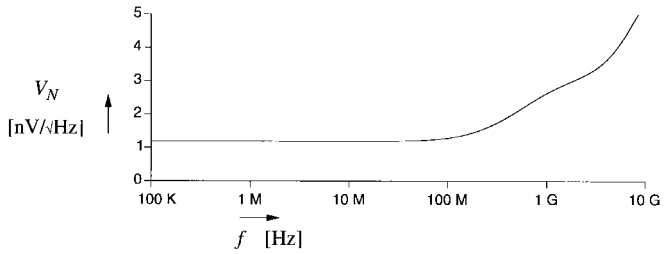



Fig. 9. Simulated noise characteristic of multipath nested Miller compensated 1-GHz opamp.

and high-frequency transfer function are equal [2]

$$\omega_0 = 2\,\frac{g_{31}}{C_{M2}} = \frac{g_{32}}{C_{M1}}. \tag{16}$$

In this case, a zero cancels one pole at $\omega_{p2}$ in the total transfer function. Equation (16) shows that the pole-zero doublet introduced by the feedforward path can be well controlled, because the pole-zero matching relies on the matching of transconductance and capacitors. Only one zero remains in the right half-plane. This zero can be removed by inserting a resistor in series with $C_{M1}$ in the same way as with the two-stage Miller compensated opamp. The result is a wideband transfer function with only two poles.

An additional requirement is that $\omega_{p2}$ and $\omega_{p3}$ are not allowed to be complex. When they are complex, the zero introduced by the feedforward path cannot cancel one of the poles, and the feedforward compensation no longer works. The feedforward path, therefore, should take over at a frequency below pole $\omega_{p3}$. To calculate the magnitude of the feedforward path $A_{FF}$, we combine the zero $\omega_z$ with the dominant pole $\omega_{p1}$ and the dc gain of the feedforward path, yielding

$$A_{FF} = \frac{g_{32}}{g_2}\left(1 + 2\,\frac{C_{b\epsilon 2}}{C_{M2}}\right) \approx \frac{g_{32}}{g_2}. \tag{17}$$

Since $\omega_{p3}$ is normally positioned a factor two above the unity-gain frequency, this yields the requirement to prevent complex poles as

$$\frac{g_{32}}{g_2} > \frac{1}{2}. \tag{18}$$

The pole $\omega_{p2}$ is found by calculating the crossing between the feedforward path and the $-20$ dB slope of the nested Miller characteristic, yielding

$$\omega_{p2} = 2\,\frac{g_{31}}{g_{32}}\,\frac{g_2}{C_{M2}}. \tag{19}$$

The bandwidth $\omega_{B,\,MNM}$ of the multipath nested Miller compensated circuit is calculated by dividing the product of the three poles by pole $\omega_{p2}$. When the transconductance of the feedforward input stage $g_{32}$ is equal to the normal input stage $g_{31}$, the result is

$$\omega_{B,\,MNM} \cong \sqrt{\frac{g_1 g_{32}}{C_{b\epsilon 1}C_L + \frac{1}{2}\,C_L C_{M1} + C_{b\epsilon 1}C_{M1}}}. \tag{20}$$

In contrast to nested Miller compensation, one pole is removed. This is induced by the feedforward path. The expression is therefore almost identical to the bandwidth expression of the Miller compensated circuit. Therefore, the bandwidth remains high and the bias-current considerations are similar to the bias-current considerations of the Miller compensated circuit. Thus, the input stage is biased at 1 mA per transistor and the output stage at 5 mA. Because of noise considerations, the feedforward input stage and the intermediate stage also need a high bias current as described below. In all cases, however, the requirement stated by (18) has to be satisfied. Further, although the bandwidth does not depend on the intermediate-stage transconductance $g_2$ in first order, the bandwidth reduces when $\omega_{p2}$ and $\omega_{p3}$ are too close to each other [2]. A compromise is found by biasing both the feedforward input stage and the intermediate stage at 1 mA per transistor. Altogether, the unity-gain frequency is 2.8 GHz. The value of $C_{M1}$ and $C_{P1}$ is 1.1 pF and the value of $C_{M2}$ and $C_{P2}$ is 2.2 pF.

*Noise Performance:* Since the source impedance in high-frequency systems is low, usually 50 Ω, the noise performance is dominated by voltage noise. The equivalent input noise voltage resistance of the opamp is dominated by that of the input pair

$$R_{\text{eqv}} = 2R_{B,\,400} + \frac{1}{g_{m,\,400}} + 2\,\frac{1}{g_{m,\,400}^2 R_P} \tag{21}$$

where $R_{B,\,400}$ is the base resistance of the input stage $Q_{400}$, $Q_{401}$, $g_{m,\,400}$ is the transconductance of the input stage $Q_{400}$, $Q_{401}$, and $R_p$ is the equivalent noise resistance of current sources $I_{405}$ and $I_{406}$. The first two terms originate from the input stage and the last term from the current sources $I_{405}$ and $I_{406}$. The last term can be made small by applying emitter degeneration. In this design, we allow a noise voltage of 1.2 nV/$\sqrt{\text{Hz}}$. Since 1.2 nV/$\sqrt{\text{Hz}}$ corresponds to a resistance of only 90 Ω, a very low base resistance $R_B$ and a very low emitter impedance $r_E$ are necessary. Therefore, very large input transistors should be used to realize a base resistance of the order of 30 Ω, and a high collector bias current of the input transistors of the order of 1 mA is required to achieve an emitter resistance $r_E$ of about 25 Ω at room temperature.

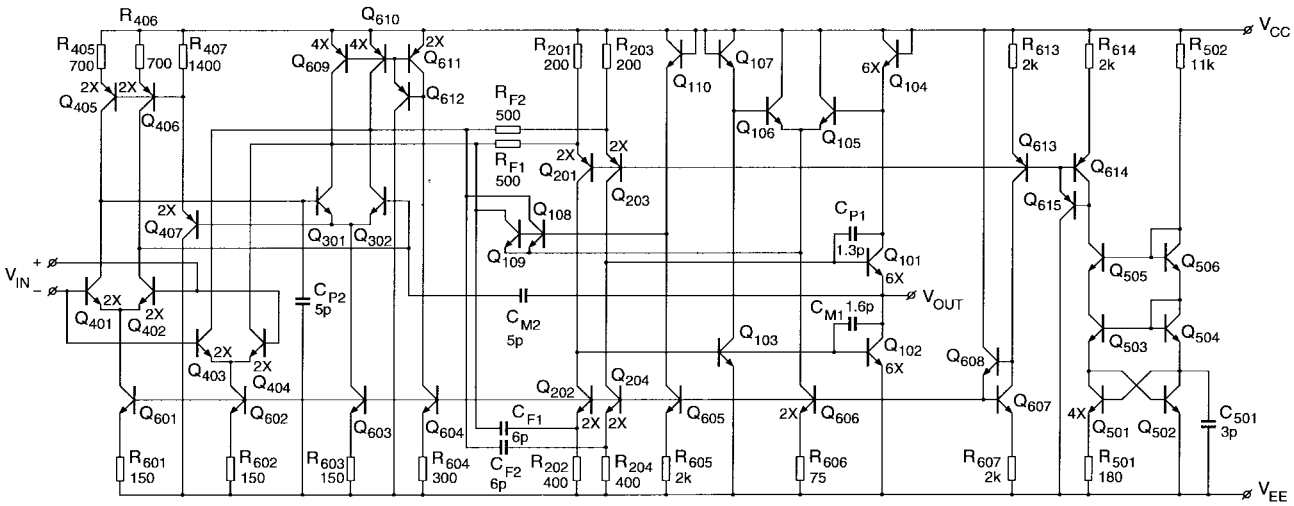
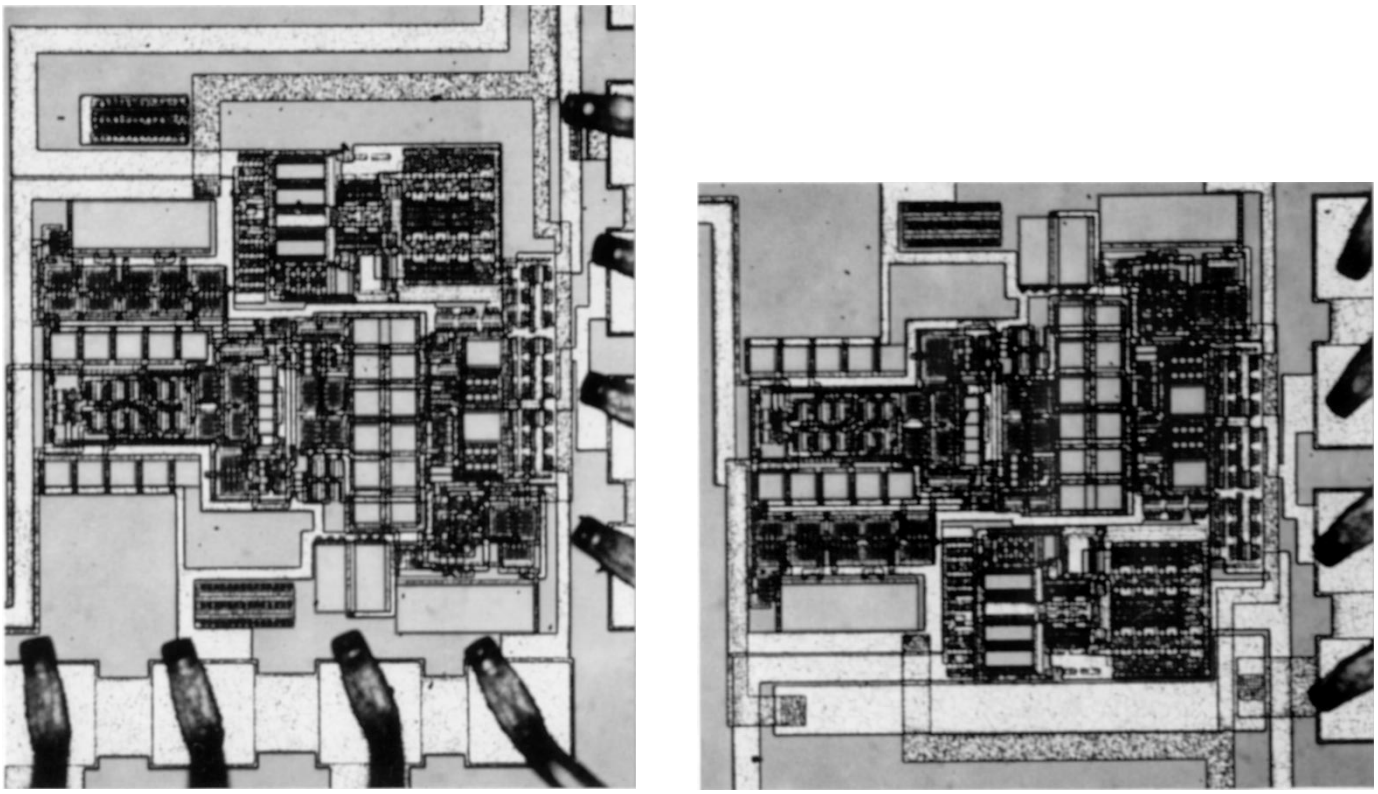



Fig. 10. Circuit diagram of complete three-stage 1-GHz opamp.



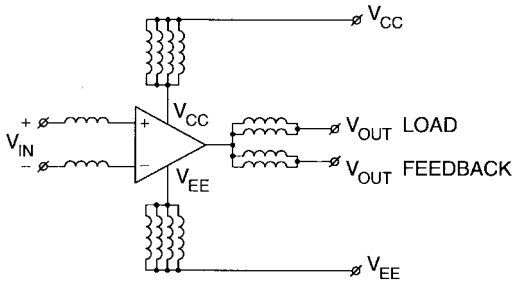
(a) (b)

Fig. 11. Photomicrographs of three-stage 1-GHz opamp: (a) open-loop version and (b) unity-gain version.

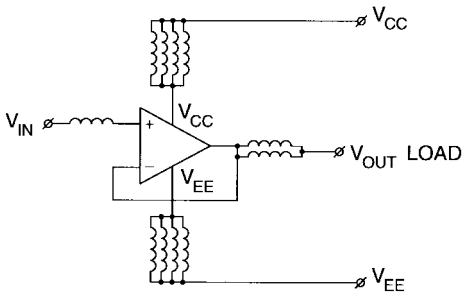
The feedforward input stage contributes to the noise at high frequencies. Although this seems to be less important, the affected frequency band can be very large. Therefore, the noise considerations also apply to the feedforward input stage and the takeover of the feedforward path should be at the highest frequency possible. Since the takeover is at $\omega_{p2}$, as given by (20), the transconductance $g_2$ of the intermediate stage must be large. In addition, this further reduces the influence of slow-settling components in the transient response caused by the pole-zero doublet [1]. The noise characteristic of the multi-path nested Miller compensated 1-GHz opamp illustrating the higher noise above the takeover of the feedforward path is shown in Fig. 9.

## IV. Realizations and Measurements

The realized circuits are discussed in this section. Two 1-GHz opamps have been designed and fabricated in a 10-GHz $f_T$ 1-$\mu$m BiCMOS process. The first opamp is based on the two-stage topology. Although the gain of this circuit is rather low, it is the first step toward a 1-GHz opamp. It is

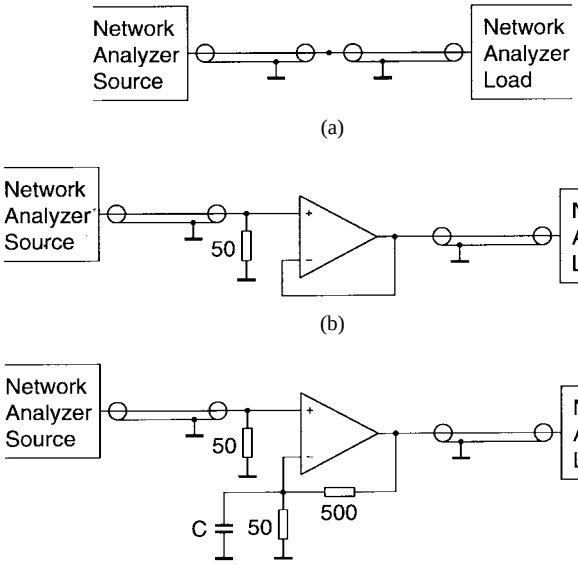



(a)




(b)

Fig. 12. Bonding schemes: (a) version for open-loop testing and (b) unity-gain version.




(a)

(b)

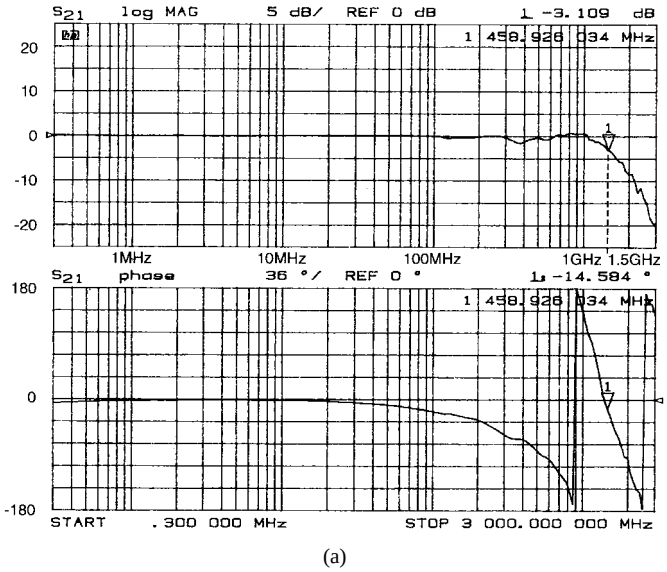
(c)

Fig. 13. Measurement setup: (a) calibration measurement, (b) unity-gain measurement, and (c) open-loop measurement.

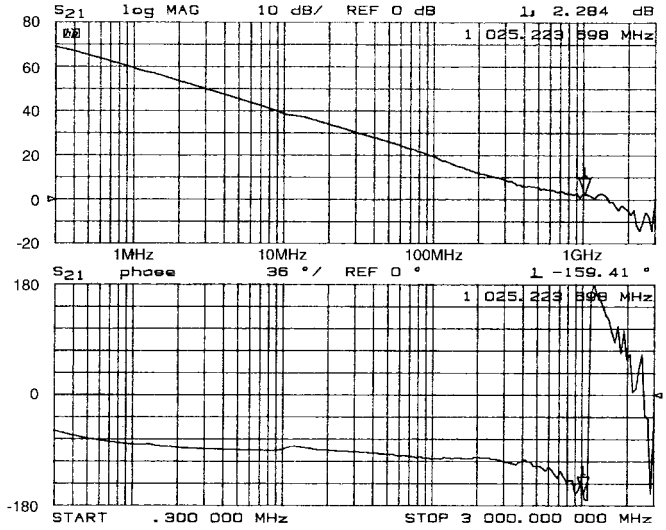
discussed only briefly. The second opamp is based on the three-stage topology with multipath nested Miller compensation. It combines high gain with very high bandwidth, and therefore, it is a useful high-frequency building block. Further, the bandwidth limitation of the package is considered and, finally, the measurement results are discussed.

### *A. Two-Stage 1-GHz Opamp*

The two-stage 1-GHz opamp is shown in Fig. 5. The input stage consists of transistors $Q_{401}$, $Q_{402}$. The input stage drives the level-shift stages consisting of transistors $Q_{201}$, $Q_{203}$ and $Q_{202}$, $Q_{204}$, resistors $R_{F1}$ and $R_{F2}$, and




(a)

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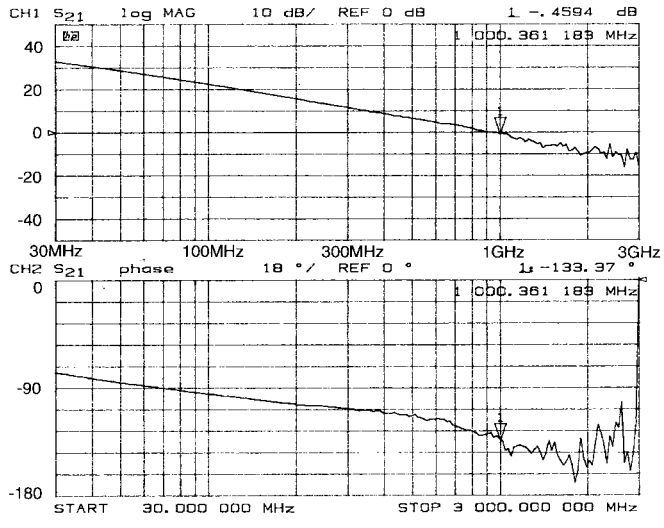
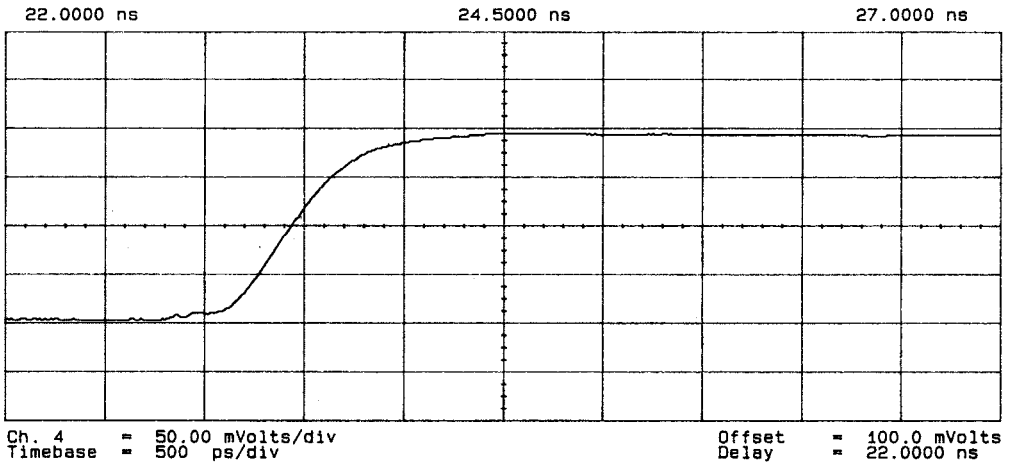
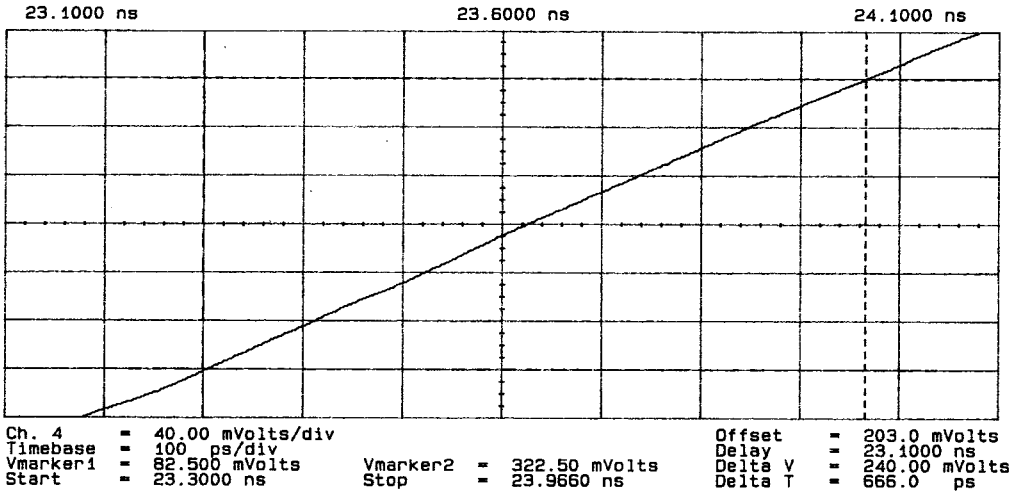



(c)

Fig. 14. Measured frequency response of three-stage 1-GHz opamp: (a) unity-gain frequency response, (b) open-loop frequency response, general overview, and (c) open-loop frequency response for determining the phase margin.




(a)




(b)

Fig. 15. Measured step response of three-stage 1-GHz opamp using unity-gain connected device: (a) response to a 200 mV step and (b) response to a 400 mV step, zoomed in to determine slew rate.

capacitors $C_{F1}$ and $C_{F2}$. The level-shift stages drive the output transistors $Q_{101}$, $Q_{102}$. The class-AB control circuit is implemented by transistors $Q_{103}$–$Q_{110}$. Miller compensation is used for frequency compensation. Although a possible unity-gain frequency of 3.4 GHz was predicted in Section II, the unity-gain frequency is set at 1 GHz. This bandwidth reduction is due to phase lag originating from the parasitic pole of the level-shift circuit and parasitic capacitance in the level-shift circuit and the output stage. Further, the bandwidth was reduced because of bonding-wire inductance.

### *B. Three-Stage 1-GHz Opamp*

The three-stage 1-GHz opamp is shown in Fig. 10. It basically consists of the two-stage circuit preceded by a double input stage. One of the input stages implements the feedforward path. The input stage consists of transistors $Q_{401}$, $Q_{402}$, which drives the intermediate stage $Q_{301}$, $Q_{302}$. Multipath input stage $Q_{403}$, $Q_{404}$ bypasses the intermediate stage and directly drives the output stage via the level-shift stages. The intermediate stage and the multipath input stage drive the level-shift stages consisting of transistors $Q_{201}$, $Q_{203}$ and $Q_{202}$, $Q_{204}$, resistors $R_{F1}$ and $R_{F2}$, and capacitors $C_{F1}$ and $C_{F2}$. The level-shift stages drive the output stage $Q_{101}$, $Q_{102}$. The class-AB control circuit is implemented by transistors $Q_{103}$–$Q_{110}$. The first Miller compensation around the output-stage transistors is formed by $C_{M1}$ and $C_{P1}$. $C_{M2}$ forms the outer Miller compensation loop. For balancing reasons, $C_{P2}$ connected to ground is added. Transistor $Q_{407}$ creates a common-mode feedback loop to fix the bias voltages of the intermediate stage $Q_{301}$, $Q_{302}$. A proportional-to-absolute temperature (PTAT) source consisting of transistors $Q_{501}$–$Q_{506}$ and resistors $R_{501}$, $R_{502}$ is used to bias the opamp [10]. To stabilize the PTAT source capacitor $C_{501}$ is added. The unity-gain frequency of this opamp is also set at 1 GHz. Two versions have been made, an open-loop version and a circuit with on-chip unity-gain feedback. Photomicrographs of the open-loop opamp and the unity-gain opamp are shown in Fig. 11. The active die area is 0.26 mm$^2$.

### *C. Packaging*

Apart from circuit design, packaging is a very important issue at these high frequencies. The inductance of the bond-

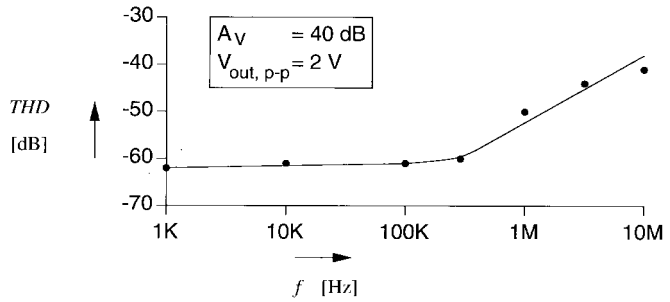



Fig. 16. Measured THD as a function of frequency using 1-GHz opamp connected as 100× amplifier with 2-V peak-to-peak output voltage.

ing wires is a potential cause of oscillation problems. Each bonding wire loaded by capacitance forms a resonator. When we consider a small bonding wire with an inductance of 3 nH loaded by a capacitance of 1 pF, the resonant frequency is about 3 GHz. This is very close to the bandwidth of our circuit! Such a resonator within the feedback loop would be disastrous. Therefore, the capacitive loading of the load was separated from the feedback path by making two output pins, one for the load and one for the feedback. In addition, double bonding wires are used on the outputs and four bond wires on the supply lines. Double bonding wires are not necessary on the inputs because the capacitive loading of the n-p-n input stage is very small. The pin connection scheme of the open-loop version is shown in Fig. 12(a). The pin connection of the unity-gain connected opamp is shown in Fig. 12(b). The chip is packaged in a small plastic surface-mounted device (SMD) package.

### *D. Measurement Results*

To test the circuit, the devices were mounted on a copper plate together with small SMD external components and high-frequency connectors connected as closely as possible to the pins. An HP8753A network analyzer was used to measure the frequency response. The measurement setup is shown in Fig. 13. To compensate for delay in the cables, first a calibration measurement was performed as shown in Fig. 13(a) with the source cable directly connected to the load cable. Then the setup as shown in Fig. 13(b) was used to measure the unity-gain connected device, and the setup shown in Fig. 13(c) to measure the open-loop opamp. Decoupling capacitor C consists of several types of capacitors to cover the whole frequency range. Using this method, an overview of the frequency response can be obtained, but it is not suited for determining the phase margin. In order to determine the phase margin, the voltage of the feedback output in Fig. 12(a) has to be examined. However, if a cable is connected to this node, the voltage is affected for high frequencies. Therefore, a separate measurement was performed to determine the phase margin, where the output of the opamp was loaded by a 50 Ω resistor connected as close as possible to the output pins. The measured frequency response of both three-stage devices is shown in Fig. 14. The Bode plot of the unity-gain buffer is shown in Fig. 14(a). The −3-dB frequency of the buffer is 1.5 GHz. Fig. 14(b) shows an overview of the frequency response from 300 KHz to 3 GHz of the open-loop version. The result of the more accurate measurement with resistive load to determine the phase margin is given in Fig. 14(c). The phase margin is 47°.

TABLE I
MEASURED SPECIFICATIONS OF TWO-STAGE 1-GHZ OPAMP $V_{PP} = 5$ V, $R_L = 50\ \Omega$, $T_A = 25°C$

| sym-bol | parameter | value | unit |
|---|---|---|---|
| $I_{PP}$ | supply current | 15 | mA |
| $A_{vol}$ | open-loop voltage gain | 38 | dB |
| BW | open-loop bandwidth | 1 | GHz |
| $V_N$ | Equivalent input noise voltage | 2.8 | nV/√Hz |

TABLE II
MEASURED SPECIFICATIONS OF THREE-STAGE MULTIPATH NESTED MILLER COMPENSATED 1-GHZ OPAMP $V_{PP} = 5$ V, $R_L = 50\ \Omega$, $T_A = 25°C$

| sym-bol | parameter | value | | | unit |
|---|---|---|---|---|---|
| | | min. | typ. | max. | |
| $T_{op}$ | temperature range | -55 | | 125 | °C |
| $V_{PP}$ | supply voltage range | 3.6 | | 5.5 | V |
| $I_{PP}$ | supply current | | 24 | | mA |
| $I_B$ | input bias current | | | 19 | µA |
| $V_{os}$ | offset voltage | | 0.2 | 0.5 | mV |
| $V_{CM}$ | common-mode input voltage range | 1.0 | | $V_{PP}$-1.0 | V |
| $I_L$ | peak load current, sink and source | 55 | 58 | 66 | mA |
| $A_{vol}$ | open-loop voltage gain | | 76 | | dB |
| $V_{out}$ | output voltage swing | 0.4 | | $V_{PP}$-1.2 | V |
| SR | Slew rate | | 360 | | V/µs |
| $S_{1\%}$ | 1% Settling time (200mV step) | | 3.4 | | ns |
| $S_{0.1\%}$ | 0.1% Settling time (200mV step) | | 6.0 | | ns |
| BW | open-loop bandwidth | | 1 | | GHz |
| $V_N$ | Equivalent input noise voltage | | 1.2 | | nV/√Hz |

The step response of the on-chip unity-gain device was measured using an HP54120A 20-GHz digitizing oscilloscope. This oscilloscope generates a 200 mV step in a 50-Ω load. The response to the 200 mV step is plotted in Fig. 15(a). Again, the opamp was loaded by a 50-Ω resistor. The 1% settling time is 3.4 ns and the 0.1% settling time is 6.0 ns. By removing the 50-Ω resistor at the input of the opamp, a 400 mV step is created in order to measure the slew rate. The result is shown in Fig. 15(b). The harmonic distortion of a 2-V peak-to-peak output voltage was measured using the opamp in a 100× configuration. The total harmonic distortin (THD) as a function of frequency is plotted in Fig. 16.

The most important parameters of the two-stage opamp are listed in Table I. Table II summarizes the measurement results of the three-stage 1-GHz opamp. The difference in bias current

is due to the added second stage and the extra input stage for the feedforward path generation. Both stages are biased at 1 mA per transistor. Further, the bias current of the output stage has been increased in order to accurately fix the bandwidth of the feedforward path.

## V. Conclusion

The design of wideband opamps requires, firstly, a three-stage topology to cope with the 50-$\Omega$ load and, secondly, an efficient frequency compensation technique. Multipath nested Miller compensation proves to be a very efficient frequency compensation scheme that operates up to very high frequencies, gaining a factor two in unity-gain frequency over nested Miller compensation. By applying nested Miller compensation to an all-n-p-n topology, a 1-GHz opamp has been fabricated with 76-dB gain and 1.2-nV/$\sqrt{}$Hz equivalent input noise voltage.

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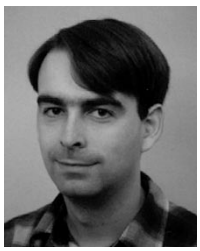

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