3. Elementary Electronic Circuits with a FET Transistor

Our main aim is to build all the possible practical amplifiers by using an FET transistor and resistor.

2.1. *FET transistors: symbols, physical structures, analytical models, and graphical characteristics*

The symbols of the *n*-channel junction field-effect (JFET) and metal-oxide-silicon field-effect (MOSFET) transistors and their physical structures are given in Fig. 1. We will analyze in the lectures only *n*-channel transistors. The only difference between the *n*-channel and *p*-channel transistors is in their static states: the static state of the *p*-channel transistors is inverse to that of the *n*-channel ones because of their opposite structures. There will be no difference in the small-signal models. The circuits analyzed in home exercises, the lab, and the exam *will* comprise both *n*-channel and *p*-channel transistors.

FET transistors have a channel, either built-in or induced, between the source and drain terminals (see Fig. 1). In JFETs the channel is isolated from the gate by the reverse biased *p*-*n* junctions, whereas in MOSFETs, the channel is isolated from the gate by a thin layer of silicon oxide, SiO_2. Note that the substrate (body) in MOSFETs should always be reverse biased to be isolated from the source, drain, and channel.

Let us start the analysis of the transistor physical structures assuming that their sources and bodies are grounded, and their drain potentials are zero.

The channels of the depletion-mode FETs are built in, whereas the channel of the enhancement-mode MOSFET is absent at v_{GS}=0. To obtain the channel in the enhancement-mode MOSFET, a great enough positive potential, v_{GS}, should be applied to its gate relative to the source, body, and drain. The positive gate attracts the electrons from the source, drain, where they are major charge carriers, and also from the body, where they are a minority. Let us denote the value of v_{GS} at which the channel just starts forming as V_t. Let us assume that for a v_{GS}=2V_t the enhancement-mode MOSFET has the same channel width as the depletion-mode transistors for v_{GS}=0.

Note now that the only difference between the enhancement- and depletion-mode FETs is in a 2V_t shift of their v_{GS} voltages. *Note also that the electric field across the gate-channel region controls the channel width of the FETs. This field (or voltage) is applied to the depletion regions of the JFETs and to the oxide layer between the gate and the channel of the MOSFETs.*

Other names for the depletion- and enhancement-mode transistors are normally-on (*n/on*) and normally-off (*n/off*) transistors since the first type does have a built-in channel at v_{GS}=0 and the other does not have it.

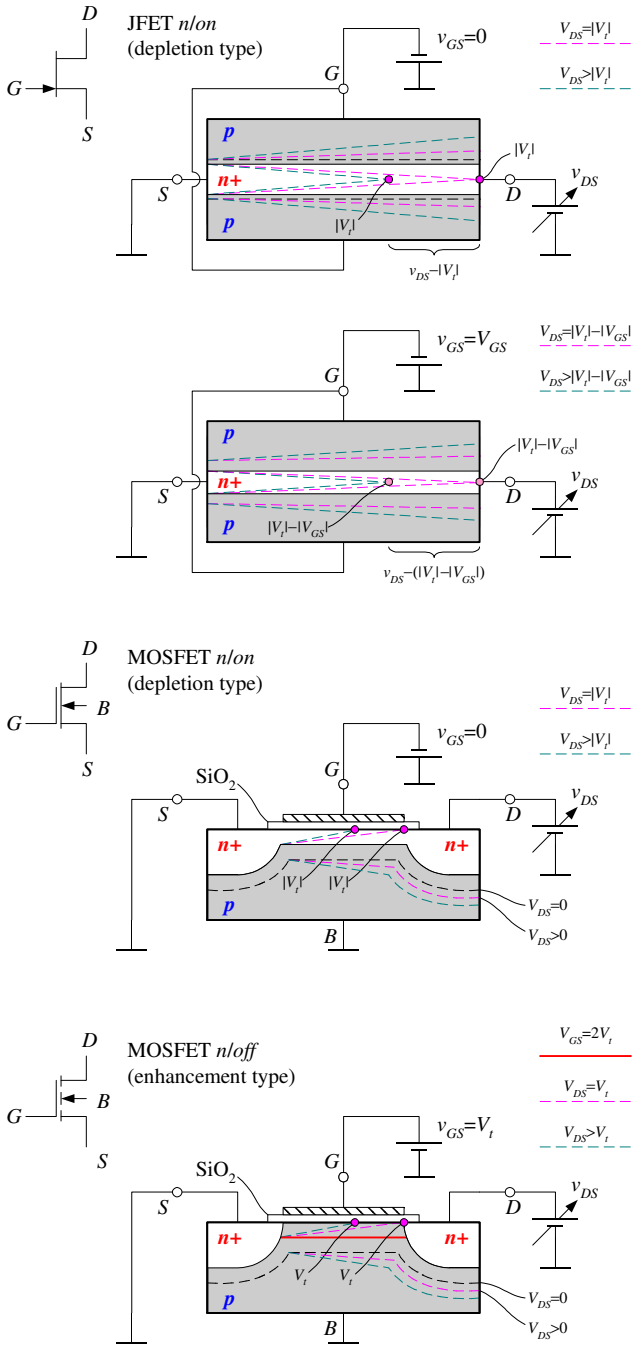

Fig. 1. The symbols of the JFET and MOSFET transistors (with the *n*-type channel) and their physical structures. For MOFETS, the operation only at V_{GS}=0 and V_{GS}=2V_t is shown for the *n/on* and *n/off* types, respectively. Note that for lower V_{GS}, the pinch-off voltage, for both the MOSFETs, will be V_p=V_{GS}–V_t, as shown for the JFET.

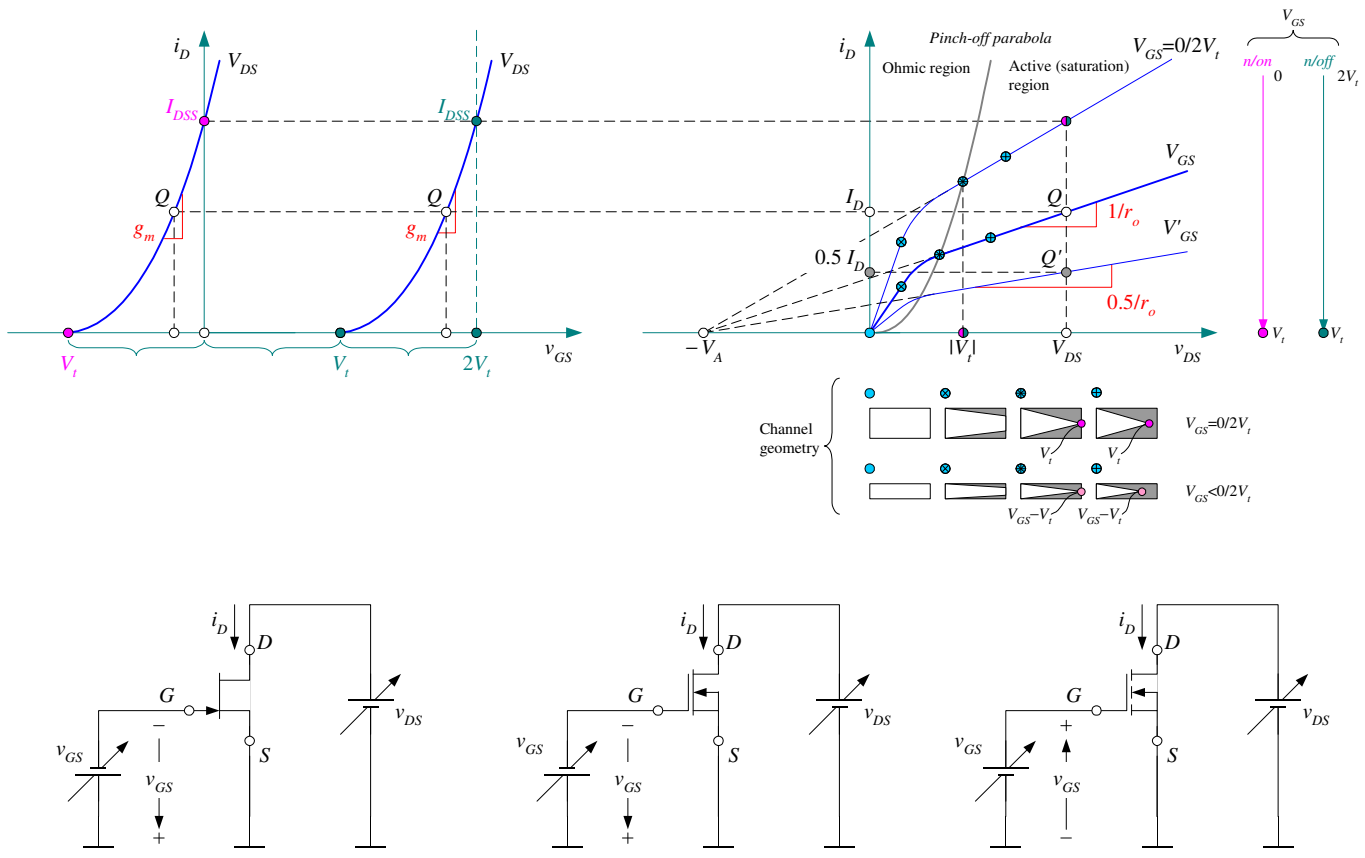

Fig. 2. Common-source characteristics of FET transistors.

For v_{DS}=0, decreasing the gate potential below v_{GS}=0/v_{GS}=2V_t increases the magnitude of the voltage controlling the channel width in *n/on* transistors and decreases this voltage in *n/off* transistors. In both these cases the channel width decreases and, at v_{GS}=V_t, reaches zero all over the channel length. *Remember this fact: if at some coordinate of the channel the magnitude of the voltage drop across the depletion regions in FETs or the magnitude of the voltage drop across the oxide layer in MOSFETs equals* $|V_t|$ *then at this coordinate the channel width equals zero.*

Let us now check for v_{GS}=0/v_{GS}=2V_t what will happen to the channel geometry when v_{DS} increases. Increasing v_{DS} increases the current flow through the channel. Due to the current, the channel potential increases over the channel length. Correspondingly, the magnitude of the voltage controlling the channel width increases in *n/on* transistors and decreases in *n/off* transistors. As a result, the channel width decreases over the channel length.

At v_{DS}=V_t, the channel width at the drain becomes zero, because the controlling voltage magnitude at this point is $|V_t|$. We will call the point where the channel width is zero as the "pinch-off" point. A further increase in v_{DS} shifts left the pinch-off point. This is because the excess, relative to $|V_t|$, part of the v_{DS} voltage drops over the depletion region, appearing instead of the channel fraction near the drain.

Note that for v_{GS}=0/v_{GS}=2V_t, the channel potential at the pinch-off point always remains V_p=$|V_t|$ relative to the source. Assuming that the maximum shift of the pinch-off point towards the source is small relative to the channel length, we can conclude that for a fixed potential at this point and for a given v_{GS}=0/v_{GS}=2V_t, the drain current is nearly constant for v_{DS}>$|V_t|$.

The drain current depends solely on the conductance of the channel region between the source and the pinch-off point and the voltage drop on it, which is proportional to the pinch-off potential $|V_t|$. When v_{DS} is greater than $|V_t|$, the rest of v_{DS} drops, as mentioned above, across the depletion region between the border of the conducting part of the channel and the drain, thus creating the electric field that *collects* (like in thee BJT-type transistor) the electrons *injected* by the conducting part of the channel. Note that in the BJT-type transistor the injection of *electrons* is controlled by the current of *holes* ("bipolar" in the abbreviation "BJT" means just this). Contrary to that, only one type of the charge carriers are involved in the operation of FETs: either electrons in the *n*-channel transistors, or holes in the *p*-channel transistors, and the injections of the charge carriers is controlled not by a current but rather by *voltage* or field (FET: field effect transistors). Note also that injection in BJTs is due to diffusion, whereas in the FETs it is due to drift.

Let us check what will happen to the channel when $v_{GS}<0/v_{GS}<2V_t$. In the JFET, decreasing v_{GS} will increase the controlling voltage magnitude, and, hence, decrease the initial (for $v_{GS}=0$) channel width. In *n/on* (depletion-mode) MOSFETs, decreasing v_{GS} will also decrease the initial width of their channels because some of the electrons will migrate from the channel to the either source, body, or drain because of the negative field of the gate. In *n/off* (enhancement-mode) MOSFETs, a lower v_{GS} will also decrease the initial width of the induced channel because a lower electric field of the gate attracts fewer electrons. As a result the pinch off will be reached at a smaller $V_p=|V_t|-|V_{GS}|$, or considering the signs of V_{GS} and V_t, $V_p=V_{GS}-V_t$, and the pinch-off potential will also become smaller: $V_p=|V_t|-|V_{GS}|$.

Note that for *n/off* MOSFETs, the decrease in v_{GS}, from $V_{GS}=2V_t$ to a lower value of V_{GS}, is $2V_t-V_{GS}$. As a result, the pinch-off will be reached at $V_p = V_t - (2V_t-V_{GS}) = V_{GS}-V_t$, which is the same as that for the *n/on* transistors.

For a smaller initial width of the channel (means smaller conductance or greater resistance) and smaller pinch-off potential, the source-drain current will also be smaller. It will also be less sensitive [1] to the shift of the pinch-off point towards source, caused by increasing v_{DS}. If we assume that this sensitivity decreases with the collector current [1], then, like in the case of the BJT transistor, the output characteristic, i_D–v_{DS}, of the FET transistors can be extrapolated to one and the same point, $-V_A$, on the v_{DS} –axis (see Fig. 2).

Analytical model: transistor equations

The simultaneous decrease of both the conductivity of the channel and the voltage drop across it causes a quadratic dependence of i_D on v_{GS}. From our previous analysis of the transistor structures, one can also see that $i_D=0$ for $v_{GS} = V_t$, and that all the extrapolations of the i_D–v_{DS} characteristics should become zero at $v_{DS} = -V_A$. Therefore:

$$i_D = K\,(v_{GS}-V_t)^2(1+v_{DS}/V_A)\,, \qquad (1)$$

where K is a coefficient that depends on the transistor geometry and technology.

Denoting (see Fig. 2) the static drain current at $V_{GS}=0$/ $V_{GS}=2V_t$ as I^*_{DSS} ("*I* drain-source saturation") that is measured (*by manufacturer) for a given V^*_{DS}, we can obtain the coefficient K as follows:

$$i_D\Big|_{\substack{V_{GS}=0/2V_t\\ V_{DS}=V^*_{DS}}} = K V_t^{\,2}(1+V^*_{DS}/V_A) \equiv I^*_{DSS}$$

$$\Rightarrow K = \frac{I^*_{DSS}}{V_t^{\,2}(1+V^*_{DS}/V_A)} \qquad . \qquad (2)$$

This provides us with another equation for i_D:

$$i_D = \frac{I^*_{DSS}}{V_t^{\,2}(1+V^*_{DS}/V_A)}(v_{GS}-V_t)^2(1+v_{DS}/V_A)$$

$$= \underbrace{I^*_{DSS}\,\frac{1+v_{DS}/V_A}{1+V^*_{DS}/V_A}}_{I_{DSS}}(1-v_{GS}/V_t)^2 \qquad . \qquad (3)$$

$$= I_{DSS}(1-v_{GS}/V_t)^2$$

As in the case of the BJT transistors, we will operate the FET transistors in the active (linear) region, where the drain current is nearly constant (saturated) and resembles a voltage controlled current source. As was explained in the previous section, the transistor channel should be pinched-off in this region. This is obtained when

$$V_{DS} \ge V_p = V_{GS} - V_t\,. \qquad (4)$$

with the border at $v_{DS}=v_{GS}-V_t$, or $v_{GS}=v_{DS}+V_t$. Considering this in (3) gives the border characteristic, so-called "pinch-off parabola" (see Fig. 2)

$$i_D = I_{DSS}\,\frac{v_{DS}^{\,2}}{V_t^{\,2}}\,. \qquad (5)$$

Note that the static V_{GS} for JFETs should *not* bias the gate-source junction in the forward direction in order to keep the gate current small. (In practice, a weak forward bias, say 0.5 V, for which the gate current is still low, can be allowed.)

FET transistors behave like a non-linear voltage-controlled resistor in the region on the left from the pinch-off parabola, hence, this region is called ohmic region. We will not study it in this course.

Small-signal parameters

Having all the needed transistor characteristics, we can define the small-signal gains as the slopes of the characteristic at the operating points.

The small-signal (mutual) conductance gain

$$|g_m| \equiv \frac{i_d}{v_{gs}}\bigg|_{Q,\,v_{ds}=0} = \frac{2}{|V_t|}I_{DSS}(1-V_{GS}/V_t)$$

$$= \frac{2}{|V_t|}\sqrt{I_{DSS}}\,\sqrt{I_D} \qquad . \qquad (6)$$

Note that g_m for FETs is proportional to $\sqrt{I_D}$, whereas for BJT, g_m is proportional to I_C. This not only provides larger gain for BJT amplifiers but also allows the linear control of the

gain. (BJTs also generate smaller noise than FETs, and especially than MOSFETs. The most important advantage of MOSFETs is their technological simplicity and smaller size. For this reason, MOSFETs replace BJTs wherever possible. One can read more on the BJT-MOSFET comparison at: http://www.ee.bgu.ac.il/~paperno/Analog_electronics.pdf)

The small-signal output resistance (note "*r-out*", *not* "*r-zero*"! **Those students who will continue using the wrong "*r-zero*" term for r_o will be asked to leave the class for 5 minutes!**)

$$r_o = \left.\frac{V_A + V_{DS}}{I_D}\right|_{I_D=1\,\text{mA},\,V_A=100\,\text{V}>>V_{CE}} = 100\,\text{k}\Omega\,. \quad (7)$$

"Large"- and small-signal models for the FET transistors

We develop a "large"-signal equivalent model (see Fig. 3) for the FET transistors the same way we did it for BJT transistors (we simply find an equivalent electric circuit having linear characteristics passing through the same operating points and having the same dynamic slopes at this points as the corresponding characteristics of the transistor).

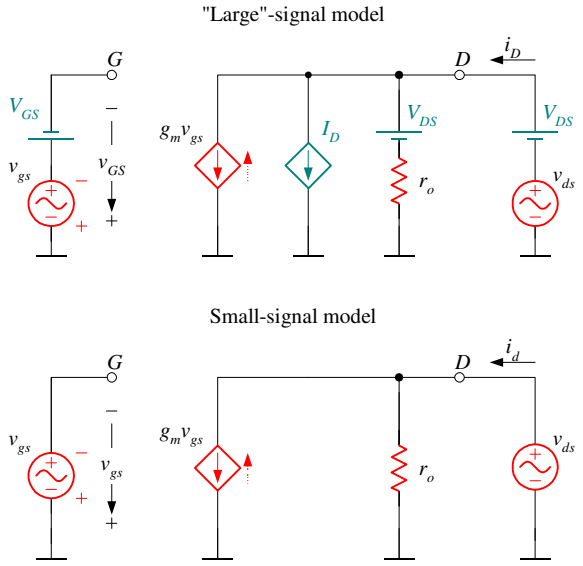

Fig. 3. "Large"- and small-signal models for the FET transistors. Note that the polarity of the small-signal source can be reversed and this will cause reversing the direction of the dependent current source $g_m v_{gs}$.

2.2. *Elementary single-transistor FET amplifiers*

Like in the case with the BJT transistors we will not use the drain as input and the gate as output. The first one is used only to collect the current of the channel and, thus, does not control the channel conductivity. The second one is either isolated from the channel by the reverse biased p-n junction in the JFET transistors or by the oxide (SiO_2) in the MOSFET transistors. The only remaining three options are shown in Fig. 4.

We will solve below only the CS amplifier. The CD amplifier will be solved in class exercises, and the analysis of CG amplifier will be given as a home work.

CS amplifier

As always, we start the circuit analysis from finding the static state (see Fig. 5). Assuming that I^*_{DSS}=16 mA at V^*_{DS}=5V, V_A=100V, V_t=–4V, V_{DD}=10V, and I_D=1mA, we first find

$$I_D = I^*_{DSS}\frac{1+V_{DS}/V_A}{1+V^*_{DS}/V_A}(1-v_{GS}/V_t)^2$$

$$= 16\text{mA}\,\frac{1+(\sim 5)/100}{1+5/100}\left(\frac{4}{4}-\frac{V_{GS}}{-4}\right)^2 \approx 1\text{mA}\,. \quad (8)$$

$$\Rightarrow V_{GS} \approx -3\text{V}$$

Second, we find the minimum value of V_O for which the channel, according to (6), is still pinched-off

$$V_{O\,\text{min}} = V_{DS\,\text{min}} = V_{GS} - V_t = -3-(-4) = 1\text{V}\,. \quad (9)$$

Third, we set V_O at the value for which the maximum range is obtained for both the positive and negative excursions of v_O:

$$\Delta_{\max}(v_O) = 0.5(V_{DD} - V_{O\,\text{min}}) = 0.5(10-1) = 4.5\text{V}$$

$$\Rightarrow V_O = V_{DS} = V_{O\,\text{min}} + \Delta_{\max}(v_O) = 4.5+1 = 5.5\text{V} \quad . \quad (10)$$

Having V_O, we find

$$R_D = \frac{V_{DD}-V_O}{I_D} = \frac{10\text{V}-5.5\text{V}}{1\text{mA}} = 4.5\text{k}\Omega\,. \quad (11)$$

We will choose R_D at the nearest available value 5kΩ, instead of 4.5kΩ, at some expense of the range for the negative excursions of v_O. Correspondingly for I_D=1mA, V_O and V_{DS} will become 5V.

Now we can find the small-signal parameters:

$$|g_m| = \frac{2}{|V_t|}\sqrt{I_{DSS}}\sqrt{I_D} = \frac{2}{|-4|}\sqrt{16\text{mA}}\sqrt{1\text{mA}} = 2\text{mS}\,, \quad (12)$$

and

$$r_o = \frac{V_A+V_{DS}}{I_D} = \frac{100\text{V}+5\text{V}}{1\text{mA}} \approx 100\text{k}\Omega\,. \quad (13)$$

Having g_m and r_o, we can solve the small-signal equivalent circuit in Fig. 5 for:

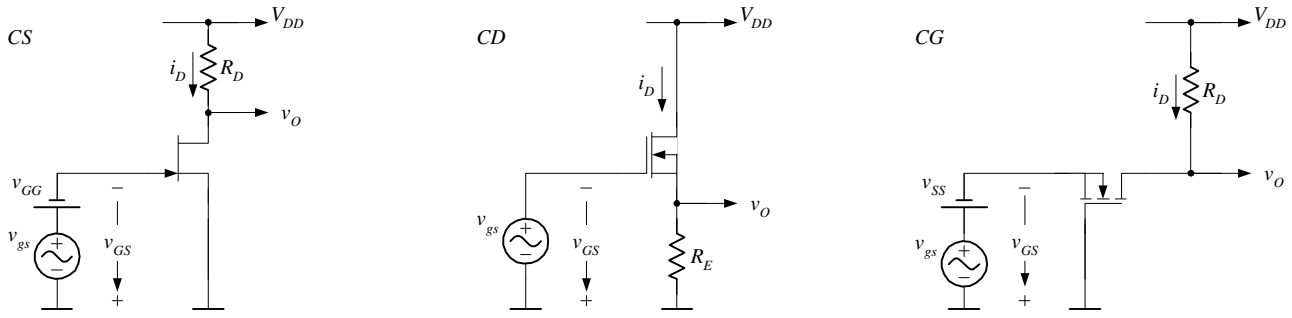

Fig. 4. Elementary single-transistor FET amplifiers.

$$A_v \equiv \left.\frac{v_o}{v_s}\right|_{v_s=1} = -\,|\,g_m\,|\,(R_D \parallel r_o) \approx -2\text{mS}\,5\text{k}\Omega = -10\,, \tag{14}$$

$$A_i \equiv \left.\frac{i_o}{i_s}\right|_{i_s=0} = -\infty\,, \tag{15}$$

$$A_p = A_v A_i = \infty\,, \tag{16}$$

$$R_{in} = \infty\,, \tag{17}$$

$$\begin{aligned} R_o &= R_D \parallel r_o \\ R_o(R_D) &= r_o \end{aligned}\,. \tag{18}$$

As one can see from (14)–(18), the elementary CS amplifier has a voltage gain $|A_v|$=10. Note that, although this gain *is* greater than 1, it is by an order of magnitude smaller than that of the elementary CE amplifier (200).

The CS amplifier reverses the phase of the small-signal output voltage compared to the input small-signal voltage. Due to the very small input current (<10 fA, not considering the gate leakage), the CS amplifier has the current and power gains magnitudes and also the input impedance approaching infinity. The output impedance of the CS amplifier, seen by the load R_D, is high, but not especially high (100 kΩ), compared to the output impedance that can be achieved in the CG amplifier having r_s>>1/g_m.

HOME EXERCISE

Prove that $R_o(R_D)$ of the elementary CG amplifier with r_s>>1/g_m can be by two or even three orders of magnitude higher than that obtained for r_s=0.

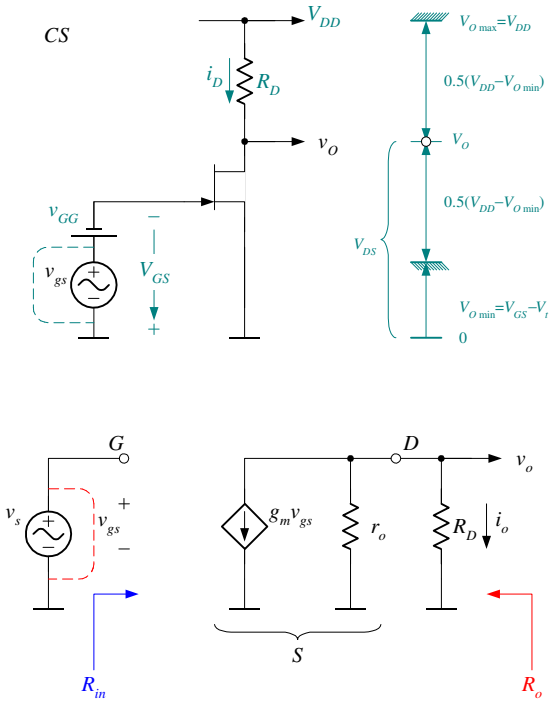

Fig. 5. Elementary CS amplifier: the static state and the equivalent small-signal circuit.

REFERENCES

[1] A. S. Sedra and K. C.Smith, *Microelectronic circuits*.