Electronic Design Project 2
Cadence OrCAD PCB Designer 16.3

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Objectives

After completing these laboratories, you should be able to:

- analyse by hand, capture, simulate and lay out a simple, one-transistor amplifier on a one-sided printed circuit board (PCB) with manual routing
- lay out an instrumentation amplifier based on three op-amps, comparing one-sided and double-sided boards with automatic routing, and produce photomasks for production
- lay out a mixed-signal system, comparable with the final project in this course, following standard procedures for schematic capture.

Preamble

Please ensure that you have the following two items for every laboratory.

- A bound, A4 laboratory notebook for making notes, recording results and storing printouts. You will get no marks if you don't have a book with you.
- University (Novell) printer credits so that you can print the circuits, layouts and the results of your simulations. Printouts should be attached firmly into your laboratory book for future reference.

The first part of these laboratories, which is a 'pencil and paper' analysis of a one-transistor amplifier, must be written up in your laboratory book as you do it. The remaining parts do not need much of a record to be kept but you will find it useful to make a note of tricks and tips for using OrCAD. This will be valuable when you have to design your own circuits later this year and in subsequent projects.

These laboratories form part of your professional development because it is expected that every electronic engineer should be able to design, populate and test a printed circuit board (PCB). You must therefore complete the first two designs to be awarded credit. Most of the marks are awarded simply for completion but extra marks will be awarded for good layouts. Late work will be considered for credit but marks will not be awarded.

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1 Introduction

These exercises introduce you to schematic capture, simulation and PCB layout using Cadence OrCAD PCB Designer with PSpice. This suite comprises three main applications.

- **Capture** is used to draw the circuit on the screen (schematic capture). It is easy to incorporate changes to the design and to correct errors. (On the other hand, it is much faster to develop the outline of a circuit using pencil and paper, as we shall do for the first exercise.)
- **PSpice** simulates a captured circuit so that you can investigate its performance. Plots were produced by a separate application called **Probe** in the past and I'll stick to this name, although this functionality has long been integrated into PSpice.
- **PCB Editor (Allegro)** is the application for laying out a printed circuit board. It includes an automatic router that works out the arrangement of tracks needed to connect your components on the PCB. The output is a set of files that can be sent to a manufacturer or printouts for the electronics workshop in the Rankine Building.

The first two applications should be familiar from last year but the third is new. These programs can be used on networked Windows PCs throughout Engineering. Unfortunately the licensing arrangements do not permit access from outwith the School. A demonstration version on DVD is available; please ask.

OrCAD PCB Designer is the most basic version of Cadence's Allegro suite for PCB design and much of the documentation refers to 'Allegro' rather than 'PCB Editor'. Allegro is widely used in industry and is similar to the Cadence software for laying out integrated circuits (ICs), which you will experience in Digital Circuit Design 3.

Fixup. The libraries for Capture and PCB Editor have some incompatibilities that must be corrected by *Fixups*. I hope to find smoother ways around these difficulties in the future. I'd also be grateful for suggestions for improving these instructions. ❦

1.1 Libraries, files, directories and design rules

Three types of information are needed for each component, corresponding to the three main applications listed above.

- **Electrical symbols** are used to draw the circuit in Capture.
- **Electrical models** allow you to simulate the circuit in PSpice.
- **Footprints** or **package symbols** show the physical size and shapes of the pads (where the pins are soldered to the board) and the outline of the package. They are used to lay out the circuit in PCB Editor.

These are stored in different sets of libraries and you must select the files needed for a particular design. You might wonder why footprints are needed as well as electrical symbols. The reason is that components with the same electrical behaviour come in different packages. For example, an integrated circuit might come in two versions:

- a traditional, plastic dual-in-line package (PDIP) with pins $0.1''$ apart
- a smaller, surface-mount device (SMD) with pins only 0.5 mm apart, if it has pins at all

The opposite is also true: resistors of a particular shape come in a wide range of values.

Further information is needed to describe the characteristics of the printed circuit board on which the components are mounted. The details are important for high-speed designs but we need to know only the number of layers of copper, called *etch* in PCB Designer. This tutorial covers only single-sided boards, which have components on top and copper on the bottom, and double-sided boards, which have copper on both surfaces. Fancier boards often have two internal planes of copper used for power and ground; complex designs need further layers.

Design rules are required to lay out the circuit on the PCB. The full details are complex but the basic rules specify the minimum width of tracks and the gap between them. Manufacturers often express these numbers in the format 10/8, meaning minimum widths of 10 for tracks and 8 for gaps (although the numbers are usually the same). The units are almost always *mils*, which mean thousands of an inch; see section 4.4 on page 13. We use 25/25 rules, which are extremely coarse by modern standards but produce boards that are easy for inexperienced students to solder.

1.2 Help!

Extensive documentation is provided with OrCAD. Please try this before asking a demonstrator – it is part of the learning process. Most professional software is so complicated that even experts make regular use of the help files. An unhelpful feature of the Cadence help system is that it opens only with the page associated with the most recent action rather than offering the full range of documents. Go to the menu bar of the Cadence Help page and choose View >

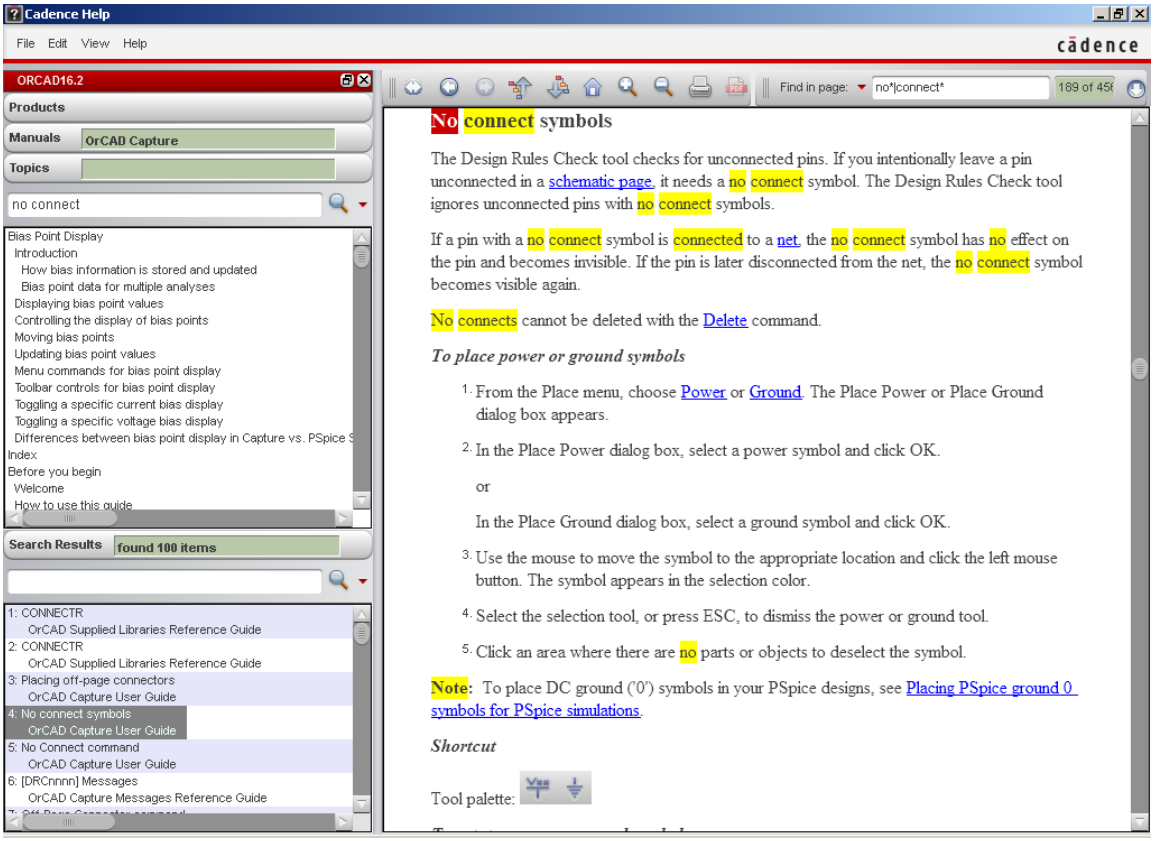


Figure 1. Cadence Help system with the Navigation pane opened.

Navigation > Show, which produces a screen like that in figure 1. Use the navigation panel on the left to choose the appropriate product and type the desired topic into the Topics box.

You should know this by now but a reminder is never a bad idea: **Save your work frequently and take regular backups of important circuits.**

2 One-transistor amplifier: simple analysis

Figure 2 shows the circuit of a simple amplifier with one transistor. It is intended to amplify audio signals, say from 20 Hz – 20 kHz. The first step in any design is to sketch the circuit using pencil and paper and estimate whether it is likely to work correctly. You will not learn how to design this particular circuit until Analogue Electronics 2 later in the year so we shall 'reverse engineer' it instead. The calculations are simple and should be done in your laboratory book. You should be pleasantly surprised to find that you don't need to know much about transistors to analyse this. In fact you did most of it in Electronic Engineering 1Y. Make sure that you recognise the emitter, base and collector of the transistor.

We first find the *bias point*, also called the operating point or quiescent point. This means the conditions when no signal is applied and the circuit is 'resting'. The 10 mVac source can therefore be ignored.

1. Resistors R_1 and R_2 form a simple potential divider if we ignore the other components

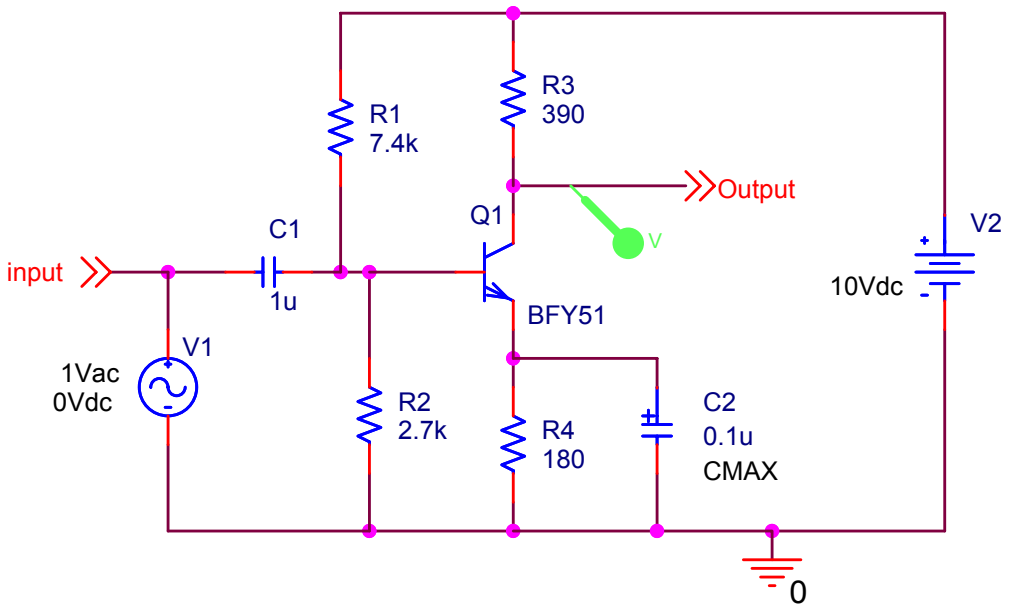


Figure 2. A simple, one-transistor amplifier that can be simulated using Spice.

attached to them. (We should go back and check this assumption when the currents are known.) Calculate the voltage on the base of the transistor Q_1.

2. The base–emitter junction of a transistor is a forward-biassed diode (hence the arrow on its symbol) and therefore has a voltage of $V_{\text{be}} \approx 0.7\,\text{V}$ across it. Use this to calculate the voltage on the emitter.

3. We now know the voltage across the resistor R_4. Calculate the current through it.

4. The current into the base of a transistor is much smaller than the other two currents, so the current flowing into the collector is nearly equal to that flowing out of the emitter. Calculate the voltage dropped across R_3 and hence the voltage on the collector.

This has shown why the four resistors are needed but not the capacitors. What is the expression for the impedance of a capacitor (remember that it is complex) and how does its magnitude depend on frequency? The capacitors in this circuit allow high frequencies to pass – the signals that we wish to amplify – but block the steady voltages that set the bias point.

- We have seen that the base of the transistor is kept at a particular voltage by the potential divider, which sets the bias point. The capacitor C_1 on the input isolates this voltage from the previous stage of the system but lets the signal through.

- Look at the circuit through which the input signal flows. It passes ‘through’ the capacitor C_1, the base–emitter junction of the transistor, R_4 and C_2 in parallel, and back to the ground connection of the input. Only the part of the voltage across the base–emitter junction gets amplified; the rest is wasted and should therefore be made as small as possible. This means that we would like to get rid of R_4 but this cannot be done because

it is needed to set the bias point – it determines the current through the transistor, as you saw above.

The solution is to put the bypass capacitor C_2 across the resistor. The bias has zero frequency so it all flows through the resistor. The signal has a 'high' frequency so most of it flows through the capacitor, which must therefore have a much smaller impedance than the resistor.

Ideally the impedance of C_2 should obey $|Z_C(f)| \ll R_4$ for all frequencies in the signal. Is this true for the values in figure 2?

Finally, estimate the voltage gain of the circuit. This needs some background on transistors that you have not yet covered so I'll just quote the result. The gain is given by

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -g_{\text{m}} R_3 \tag{1}$$

where g_{m} is called the *transconductance* of the transistor, defined by $\partial I_{\text{c}}/\partial V_{\text{be}}$. Its value is given by

$$g_{\text{m}} = \frac{I_{\text{c}}}{V_{\text{T}}} \tag{2}$$

where I_{c} is the collector current at the bias point, which you have calculated already, and V_{T} is called the *thermal voltage*. This is in turn given by $V_{\text{T}} = k_{\text{B}} T/e$ where k_{B} is Boltzmann's constant (remember this from physics courses?), T is the absolute temperature and e is the magnitude of the electronic charge. Don't worry about the formula because $V_{\text{T}} \approx 25\,\text{mV}$ at room temperature, which is easy to remember. Now you can calculate the transconductance and voltage gain. Express the gain both as a ratio and in decibels (dB).

☛ **Milestone**: Show your results to a member of staff and be prepared to explain them.

An interesting feature is that we haven't used any details of the transistor at all! This makes it easy to design circuits based on bipolar junction transistors, to give them their full name.

Now we'll capture the circuit in OrCAD, simulate it and check these estimates.

3 Schematic capture and simulation

***Always* create a fresh folder (directory) for every new project in OrCAD** otherwise you will encounter strange errors, from which it seems impossible to recover. It also keeps your work organised.

Select Start > Programs > OrCAD 16.3 > OrCAD Capture. I use '>' throughout this document to show the levels of a hierarchical menu. There will be a short delay while the software is loaded and the licence server is accessed. Alternatively, you will be asked if you wish to use Demo mode if no licence can be found. You may be offered a Cadence Product Choices box, in which case you should choose OrCAD PCB Designer with PSpice. The screen eventually shows the OrCAD Capture main window with a menu bar and tool bar. A sub-window at the bottom shows the session log.

3.1 Create a project

The first step in any design is always to create a project in OrCAD.

1. Create a new folder in Windows to hold all files for the project. I suggest that you first go to My Documents, create a new folder for this course, then create a folder within this folder for each design.

2. Select File > New > Project from the menu bar of Capture.

3. In the New Project dialog box:

   - Select an Analog or Mixed A/D project. This choice is essential or you will not be able to simulate the circuit.
   - Click on the Browse key, select your H drive and navigate to the new directory that you created for this design. Click OK.
   - Give the project a meaningful name.
   - The path and directory now show in the location box (if you can see them – they are usually too long). Click OK in the New Project dialog box.
   - Click Next.

4. Select the Create a blank project button in the small dialog box that appears and click OK.

5. Your project will now be created. The Project Manager window at the top left shows the files associated with your design and the resources used, such as library files. Its title is the full pathname of your project, which is usually far too long to fit. Check that the File tab is selected if the view looks unfamiliar.

6. Expand the Design Resources folder in the project, then the design (called *./project-name*.dsn, where *project-name* is the name of your project), then the SCHEMATIC1 folder and finally double-click PAGE1 to open the schematic page for your design. Locate the Title box in the lower right-hand corner, double-click on the placeholders, which are in angle brackets <>, and replace them with a descriptive title and so on.

3.2 Draw the circuit

Lay out the circuit in figure 2 on page 5. The method is exactly the same as last year but here are a few tips in case you have forgotten.

Jargon: The label that identifies each component on the schematic drawing is called its *reference* or *refdes*, short for *reference designator*. For example, the transistor has refdes Q1. Each refdes must be unique, meaing that no other component can be called Q1. Capture assigns a unique refdes automatically: **do not change it!** ❦

- Libraries must be chosen from the pspice folder, otherwise the components will not have PSpice models and you will not be able to simulate them.

- Basic components like resistors are in the analog library, sources such as VDC are in source and the param block is in special. Use Search if you can't guess where a component is located. You will probably need to do this for the transistor.
- The capacitor C_2 is an *electrolytic* type, which must be installed with the correct polarity or it will explode. Its parameter CMAX is the maximum working voltage, which is not needed for simulation but important when you pick out a real component. Set it to 16 V, which is a common value.
- Always join components with wires, not by placing them so close that their pins overlap.
- All circuits must have a ground node called 0 (zero) for simulation. Use Place > Ground... from the menu bar or the ground button on the right.
- PSpice is unhelpful about notation. Usage like 10^6 doesn't work but it won't tell you! (It will just stop at the caret and take the value as 10.) Use 1e6 or 1Meg instead – not 1M because a single m or M means milli, not mega.
- Wires and components sometimes become joined incorrectly if you move them about. Use Place > Junction or the junction tool from the buttons on the right to eliminate spurious connections.
- I like to use off-page connectors to label nodes such as input and output, where the voltages will be plotted. Place them from the menu or button. The names appear in Probe and make it much easier to identify the traces.

3.3 Simulate the circuit

Set up a Simulation Profile to make an AC Sweep of the circuit from 10 Hz to 100 kHz. The sweep should be logarithmic in decades with 10 points per decade. Run the simulation. Go back to Capture and click the V button to Enable Bias Voltage Display. Do the values agree with the pencil-and-paper calculations? Check the current through the transistor too.

Next, plot the voltage gain in decibels (dB). You may remember how to do this from the *RC* filter last year but here is a short cut in Capture.

1. Choose PSpice > Markers > Advanced > dB Magnitude of Voltage from the menu bar and click on the output from the amplifier. This places a marker labelled VDB.
2. You should now find a decibel plot in PSpice. This requires an input voltage of 1 Vac.

Does the gain match the estimated value and is it reasonably constant with frequency?

I found that the gain did not behave as expected (so now I have given you the answer to the first question!) and suspect that the capacitor C_2 across the emitter resistor R_4 is too small. Check this by simulating the circuit for a set of values of C_2. This requires a *parameter*. You should remember how to do this but the procedure is clumsy so here is a reminder.

1. Place a param block on your schematic from the special library.
2. Open the Property Editor for the param block with one of these three methods (I'll only mention one in future): choose Edit > Properties... from the menu bar, select the Edit Properties... contextual menu item or double-click the block.

3. Choose Add row... (or column, depending on the orientation of your spreadsheet) to create the parameter. Give it a name, such as Cap2, and a default value (use its previous, fixed value). Click OK to get rid of the dialog box.

4. The parameter does not appear on the schematic by default so you must select the newly added row/column in the spreadsheet, click the Display button, select Name and Value and click OK. Close the Property Editor. You should now see your parameter in the block.

5. Change the value of C_2 from a fixed value to the parameter. Remember that the parameter must be enclosed in curly brackets {} in the Value field.

6. Create a new simulation profile with the same frequency sweep plus a parametric sweep on Cap2 from 0.1 µF – 1000 µF. Use a logarithmic sweep with one value per decade. Run the simulation and make a plot in decibels as described above. Print the plot and label the curves with the corresponding values of Cap2 by hand (the software cannot do this). The printout looks better if you make the lines thicker. (If you print in black and white, set the number of trace colours to zero so that the curves show up.)

Does a larger value of C_2 improve the performance? What value would you recommend?

☛ **Milestone**: Explain your results and recommended value of C_2 to a member of staff.

4 Preparation for PCB layout

Once the design of the circuit has been finalised, it can be laid out on a printed circuit board (PCB). This takes a few steps before you leave Capture. The overall *design flow* for making a PCB is shown in figure 3 on the next page with a summary in section B on page 48.

4.1 Edit the circuit

First, the 'virtual components' in the schematic must be replaced by real components. Here this means the voltage sources and param block. Sometimes a battery is mounted on a PCB to supply power but you cannot build a real circuit with a param block! (Well, you could use a pair of sockets and unplug the component to change it.) The real circuit requires connectors for input, output and power as shown in figure 4. The types of connector are HEADER 2 and the like. They are in the connector library, which is in the directory one level above the pspice directory (OrCAD16.3/tools/capture/library/). The connectors are oriented so that pin 1 is connected to ground in both cases. It is shown by a square marker on the PCB. Change the 'values' of the connectors to make them more descriptive than the defaults. For example, I changed HEADER 2 to Input for J1. *Do not change the refdes* – only the value. Add text to label the pins of each connector and put your name on the circuit, or you won't be able to identify it when it comes out of the printer.

Fixup. The electrolytic capacitor C_elect in the analog library is incompatible with its footprint. The pins of the footprint are numbered 1, 2 but those of the capacitor are p, n. This means that the software cannot match the capacitor to its footprint. Edit the electrolytic capacitor and change the numbers of its pins to resolve this.

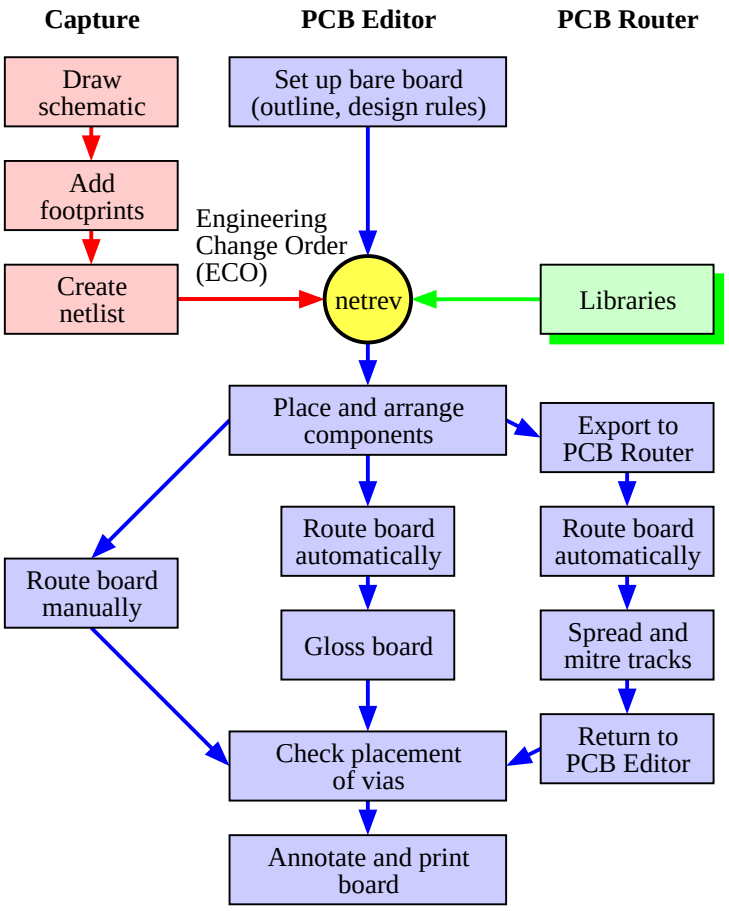


Figure 3. Design flow for making a PCB with Capture and PCB Editor. The three paths for PCB Editor depend on whether the tracks are drawn manually (as in the first design), automatically within PCB Editor, or by running the automatic router as a separate application.

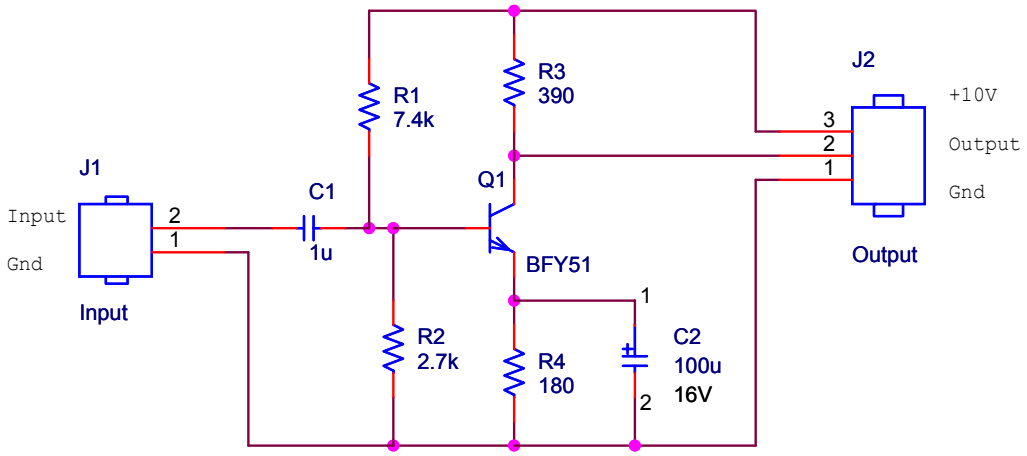


Figure 4. The simple, one-transistor amplifier with only real components, ready for layout. The pin numbers on the electrolytic capacitor are not normally visible but are shown to illustrate a fixup.

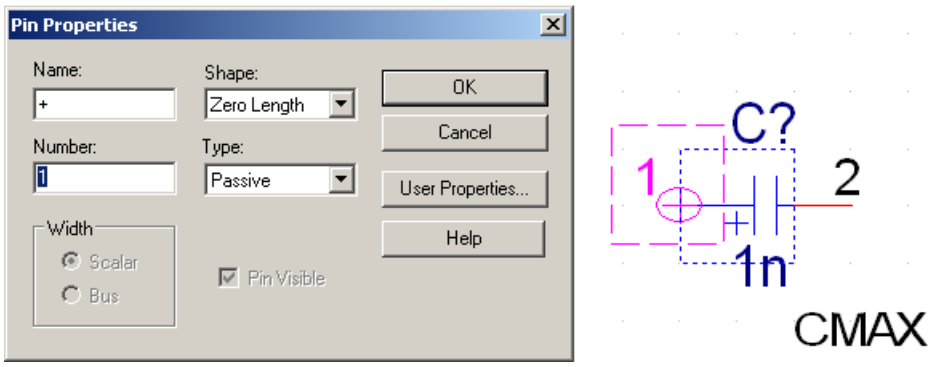


Figure 5. Edit Part window and Pin Properties dialogue box for correcting the numbering of the pins of the electrolytic capacitor.

1. Select the electrolytic capacitor and choose Edit > Part from the menu bar. A window opens with an enlarged view of the capacitor.

2. The positive pin is shown as a circle on the left. Select it and and choose Edit > Properties. . . . This brings up the Pin Properties dialogue box, shown in figure 5.

3. Change the Number to 1 and click OK. Don't worry about the name of the pin.

4. The negative pin is shown as a red line on the right. Change its Number to 2.

5. Choose File > Close. You have the choice of updating this part alone, or all 'part instances' – that means all C_elect components in your design. There is only one so it doesn't matter whether you choose Update Current or Update All in this case.

I made the pin numbers visible for the electrolytic capacitor in figure 4 on the preceding page as a reminder of this fixup. You need not do this. ❦

Print the schematic drawing and stick it into your laboratory book. The circuit takes up only a small part of the page so it is a good idea to choose File > Print Area > Set and mark out a rectangle that includes only the part of the page that you wish to print.

☛ **Milestone**: Have your drawing checked before you go any further. It is much easier to correct mistakes at this stage.

4.2 Add footprints

The main task in preparing the design for layout is to associate a *footprint* with each component. The footprint shows the physical outline of the components including the copper *pads* to which the pins are soldered. Most pads are either circular or oval except for pin 1, which has square corners to identify it. The components in the pspice library have footprints already but unfortunately they are mostly wrong. We must therefore enter the correct footprints, which are listed in table 1 for this circuit. Please type carefully and don't muddle the letter 'O' with the numeral '0'.

Table 1. Components, names in Capture and footprints for the one-transistor amplifier. The names are not case-sensitive.

Part	Capture name	Footprint name
Resistor	R	GU-RC400
Capacitor	C	GU-RC500
C, polarised	C_elect	GU-CAPCYL200
Connector	HEADER 2	GU-MOLEX2
Connector	HEADER 3	GU-MOLEX3
Transistor	BFY51	GU-TO5 (letter 'oh' not number zero)

1. Drag the cursor over your schematic drawing so that all the components are enclosed in a rectangle. Do not include the title box.
2. Choose Edit > Properties... from the menu bar, which brings up the Properties spreadsheet.
3. Type each name into the PCB Footprint field of the Properties spreadsheet. All the resistors have same footprint so use copy and paste for speed.

A problem with footprints...

PCB Editor comes with a library of footprints but they are intended for commercial production and are unsuitable for boards made in the university. Mr I. Young of the SPEED group has therefore designed a more suitable set of footprints, whose names begin with GU- to distinguish them. A catalogue is included at the end of this handout, which you should be able to match with components kept in stores.

4.3 Design rules check

The next step is a Design Rules Check to ensure that no errors have been introduced.

1. Click on the Project Manager window and highlight your design (with extension .dsn).
2. Select Tools > Design Rules Check... from the menu bar.
3. Under Design Rules select both Run Electrical Rules (probably selected already) and Run Physical Rules (probably not).
4. Click OK. A dialog box may report One or more errors or warnings were encountered. Do you wish to view the messages in the session log? Agree to this and review the report in the Session log window. No positive message is given to confirm that all rules have been passed successfully, just an absence of complaints. *Ask for help if you do not understand a message* – don't just ignore it.

5. Return to your drawing and correct any errors, shown by green circles (a strange choice of colour). Repeat until the Design Rules Check runs silently.

6. You may wish to run the Design Rules Check and select Action > Delete existing DRC markers to get rid of the green circles. They do not vanish by themselves.

4.4 Make an empty board in PCB Editor

The simplest way of creating a PCB is first to set up an empty PCB, then to add your components and connections to the board. This follows the design flow shown in figure 3 on page 10.

First create a directory allegro within your directory for the current project. PCB Editor likes to keep its files in a directory with this name. Then choose Start > Programs > OrCAD 16.3 > OrCAD PCB Editor, which opens the OrCAD PCB Designer application (Cadence seem muddled about the name). I'll leave the details of the interface until later because we need only two dialogue boxes for this step.

Set up the search paths for footprints

I mentioned above that we use a local library of footprints rather than those supplied with PCB Editor and must therefore tell the applications where to find our library. You should only have to do this once.

1. Choose Setup > User Preferences... from the menu bar, which brings up the User Preferences Editor.

2. Expand Paths in the list of Categories and choose the Library folder.

3. First change psmpath, where PCB Editor looks for package symbols (footprints). Click on the Value button, which shows only '...', to bring up a box entitled psmpath Items.

4. Click the New (Insert) button (the leftmost one), which adds an empty item to the list with another '...' button. Click this button, which brings up the usual Windows Select Directory box.

5. Navigate to the Q drive, find the allegro directory, then pcb_lib and finally symbols. Click OK to select this directory.

6. Next we must tell PCB Editor to look in our local directory before the default libraries, denoted by $psmpath. Click on $psmpath followed by the Move Down arrow. The psmpath Items box should now look like figure 6 on the following page except that your directories are different (my computer is not on the same network). Click OK.

7. Follow the same procedure for padpath to add the padstacks directory within pcb_lib. This is the information for the *padstacks*, the copper islands used for mounting components, including holes for pin-through-hole components.

8. Click OK to dismiss the User Preferences Editor.

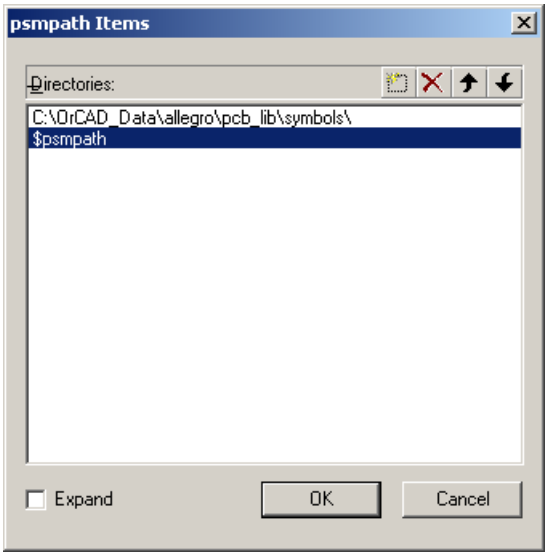


Figure 6. Completed dialogue box for setting up psmpath. Your directory path is different.

Define the board

Choose File > New... from the menu. In the first dialogue box, set the Drawing Type to Board (wizard). Click Browse..., navigate to your new allegro directory and give the board a name such as bare.brd. Click Open then OK to bring up the new board wizard. This takes you through several screens to define the parameters of the PCB. Some of these are obvious, such as the size of the board, while others set up the *design rules* – the width of tracks on the PCB, how much space must be left between them, and so on.

1. The first screen is purely descriptive. Read it, then click Next >.

2. This asks for a board template. We don't have one so select No (probably the default) and click Next >.

3. You are next asked for a 'tech' file. This is short for a *technology* file, which specifies the design rules – number of layers, widths and separation of tracks and so on. We won't use one for this design so select No and click Next >.

4. This asks for a board symbol. We don't have one so select No again and click Next >.

5. We now reach the screens for the parameters that must be set up. The units should be Mils. These are not millimeters but the American term for thousandths of an inch; 1 mm $\approx$ 40 mils. All dimensions are given in these units so get used to them.

   Leave the drawing size at A. This is an American size but you aren't allowed European A4 if the units are mils. Leave the origin at the centre.

6. Set the grid spacing to be 100 mils.

   The Etch layer count is the number of copper layers on the board – the number of layers of tracks for signals and power. Leave this at 2, although we shall use only one layer in the first design.

Don't worry about the artwork films – we don't use them.

7. Leave the names of the layers as Top and Bottom and their types as Routing Layer.

8. Enter 25 for the Minimum Line width (in mils). This value will propagate into the other boxes. It means 0.025″ or about 0.64 mm, which is very wide for a track nowadays but makes the board easy to produce and solder by hand.

   For the Default via padstack, click on the button with ... and choose GU-VIA80. This design is far too simple to need vias, which carry a signal from one layer of the PCB to another, but they may be required in future projects.

9. Rectangular board (it's curious that a circular board is the default).

10. Enter a width of 3000 and height of 2000 mils. This defines the board outline as $3'' \times 2''$. There is no corner cutoff.

    Specify the Route keepin distance as 100. A *keepin* means that objects must be kept inside the specified region. In this case it means that tracks cannot go any closer than 100 mils to the edge of the board. It gives a border around the PCB to aid handling and manufacture. (We'll encounter keepouts as well later.)

    Set the Package keepin distance to 250. Components must be placed within this keepin and therefore cannot be closer than 250 mils to the edge of the board. The gap between the two keepins allows you to run tracks around the outside of all the components, which is often helpful on a more complicated board.

11. Click Finish – that's it.

This has set up the design rules and made an empty board, which you can see in the main window of PCB Editor, shown in figure 8 on page 18. Three rectangles are visible for the board outline, route keepin and package keepin. Choose File > Save and close PCB Editor.

The next step is to return to Capture and send the circuit to PCB Editor so that it can be added to the empty board.

4.5 Create a netlist

The information about your design is sent from Capture to PCB Editor in the form of a *netlist*, which contains a description of the circuit and its components. (The netlist comprises three files but you don't need to look at them.)

1. Highlight your design (the object whose name ends in .dsn) in the Project Manager window of Capture.

2. Select Tools > Create Netlist... from the menu bar, which brings up a dialogue box as in figure 7 on the following page. Make sure that the PCB Editor tab is active.

3. Check that the PCB Footprint box contains PCB Footprint.

4. Check that the box underneath for Create PCB Editor Netlist is selected.

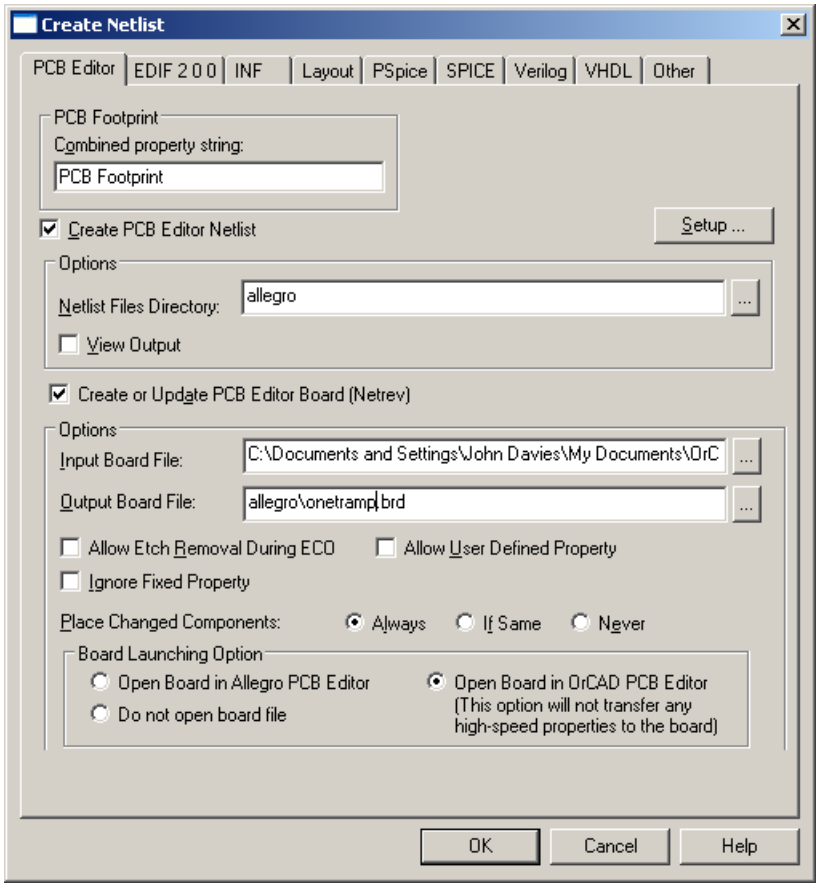


Figure 7. Completed dialogue box for netlisting the design and sending it to PCB Editor. Your file names will be different.

5. Under Options, the Netlist Files Directory should be shown as allegro. Select Create or Update PCB Editor Board (Netrev).

6. For Input Board File, choose the empty board that you have just set up. Click on the '. . . ' button to navigate.

7. The Output Board File usually shows something sensible automatically; edit it if not. It should use the new allegro directory.

8. Under Board Launching Option, select Open Board in OrCAD PCB Editor because our licence doesn't cover the full version of Allegro.

9. The entries in the dialogue box should now resemble figure 7 except for the pathnames. Click OK to dismiss this dialog box and start the netlister.

You are warned that your design will be saved by Capture, then a Progress box shows the various processes needed: Netlisting the design followed by Updating OrCAD PCB Editor Board. PCB Editor is then launched with your new board.

- A Warning box may tell you that Netrev succeeded with warnings. Check the Session Log if this happens. Messages about RVMAX and CMAX can be ignored; these are

maximum voltage ratings of the components and are not important for this circuit. *Pay attention to any others* and seek advice if they are unclear.

- OrCAD PCB Editor gives you a warning that Database was last saved by a higher tier tool, which you can ignore.

You should now see your empty board outline on the screen of PCB Editor again; the components are invisible at this stage.

5 OrCAD PCB Editor

OrCAD PCB Editor is the basic version of the Allegro PCB Editor from Cadence. Despite being 'basic' it is vastly more powerful than is needed for the simple designs that we shall lay out in this course. Its interface may feel unfamiliar because the application was originally developed for unix and has been ported to Windows with minimal changes. Some distinctive features are obvious almost immediately.

- The design window, which shows your board, has no scroll bars.
- One design is always open; you cannot open more than one, nor close the current design without opening a new one or exiting the application.
- There is no 'null' tool, such as the pointer shown by most drawing applications when no other tool is selected.

An important aspect of the interface is that tools can be used in two ways.

- First choose a command, either from the menu bar or by clicking a button, then the element of the design on which the tool should operate.
- Select the object first, then the command from the contextual menu by right-clicking.

I shall use both methods in the tutorials, picking whichever seems most natural at the time. However, confusion can arise when you change from one method to the other. It is therefore a good idea when switching to disable any active tool (right-click and choose Done if it is offered) and clear any selection (left-click outside the board or right-click and choose Selection Set > Clear All Selections).

5.1 The screen

PCB Editor needs a big screen – the elderly laptop that I have used to illustrate these instructions is not large enough to show all the toolbars! The main elements of the application are shown in figure 8 on the following page.

- **Design window**, occupying most of the screen, where you lay out the PCB. It always shows the board viewed from the top; the bottom layer is seen through the board as if it were transparent.
- **Menu bar** along the top as usual.

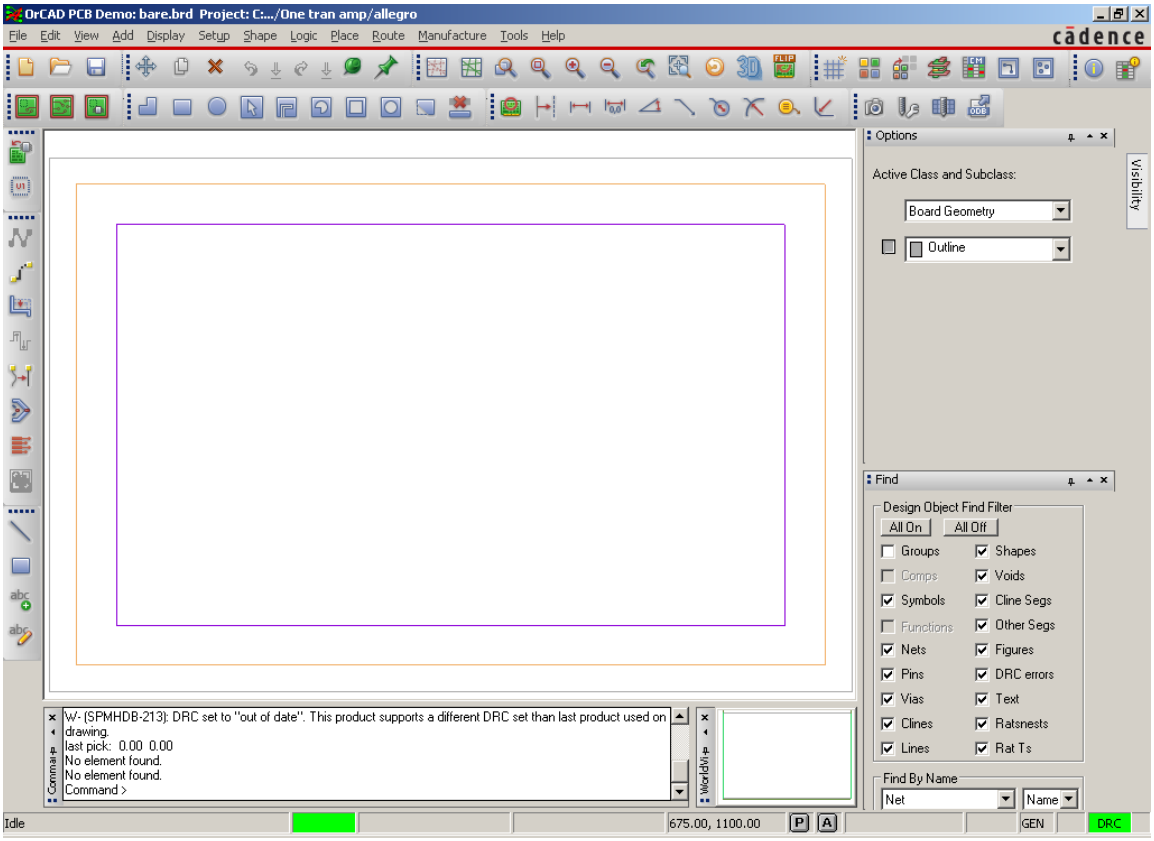


Figure 8. Screenshot of OrCAD PCB Editor with an empty board; the black background has been changed to white for a clearer printout. The rectangles show the board outline (outer), route keepin and package keepin (inner). The Find and Options control panels have been pinned open on the right.

- **Toolbars** in two rows under the menu bar and a further column down the left-hand side. Their arrangement depends on the size of the screen. Hover the pointer over a button to reveal its function.
- **Control panels** with tabs on the right-hand side. Each panel pops out when you move the pointer over its tab. Click the pin to lock a panel open.
  - **Find** selects the type of object that is highlighted when you move the mouse around the drawing.
  - **Options** changes according to the current mode and command; it selects the active class and subclass when PCB Editor is idle, then offers appropriate options when a command is chosen.
  - **Visibility** hides layers of etch while routing the board.

  I strongly recommend that you keep the Find and Options panels pinned open as in figure 8; Visibility is less useful in boards with only one or two layers of etch.
- **Command console window** at the bottom left of the screen. This prints a running log

of your actions and is useful to show when Allegro is waiting for input from you. It also displays the output from commands such as Design Rules Check.

- **Worldview window** at bottom right shows how the relation between the board outline and the view in the main design window. It is useful for moving the design window around the board as we shall soon see.

- **Status bar** at the bottom of the screen. It shows the coordinates of the pointer (crosshairs). The P (Pick) button is useful for typing coordinates instead of clicking with the mouse if your hand is unsteady.

  At the far right is a coloured block called DRC, which stands for Design Rules Check. It may be yellow because checking is not up to date. Usually it should be green to show that automatic checking is turned on and that no errors are detected.

A lot of jargon is associated with Allegro. It often refers to your design as the *database*, because that's what it is from the point of view of the computer. The various elements of the design are classified into *classes* and *subclasses*, which I'll write as class/subclass in the instructions. Here are some common examples.

- The **Etch** class includes the regions of copper that act as pads for the components and the tracks that carry the signals between them. Our designs have two subclasses of etch, **Top** and **Bottom**. They are coloured green and yellow respectively.

- The **Board Geometry** class includes the **Outline**, which we have already seen. Subclasses **Silkscreen_Bottom** and **Silkscreen_Top** are used for text to annotate the board.

- We have also seen the **Package Keepin** class, used to prevent components being placed too close to the edge of the board. It has no subclasses.

The active class and subclass can be chosen in the Options control panel but PCB Editor usually selects them automatically when you make a tool active.

5.2 Moving around the design

Two methods can be used to *pan* or *roam* around the design – move the display to the region of interest.

- Use the arrow keys on the keyboard.

- Hold down the middle button of the mouse and drag. A confusing feature of this is that *it drags the window over the design*. This means that the design moves in the *opposite* direction to your drag. It is the reverse of the hand 'grabber' in applications such as Acrobat, which drag the design under the window.

  But I have only a two-button mouse! Many two-button mice have a scroll wheel, which acts as the middle button when pressed.

You will also need to *zoom* into the design to concentrate on small details or zoom out to review the complete layout. Again there are two methods.

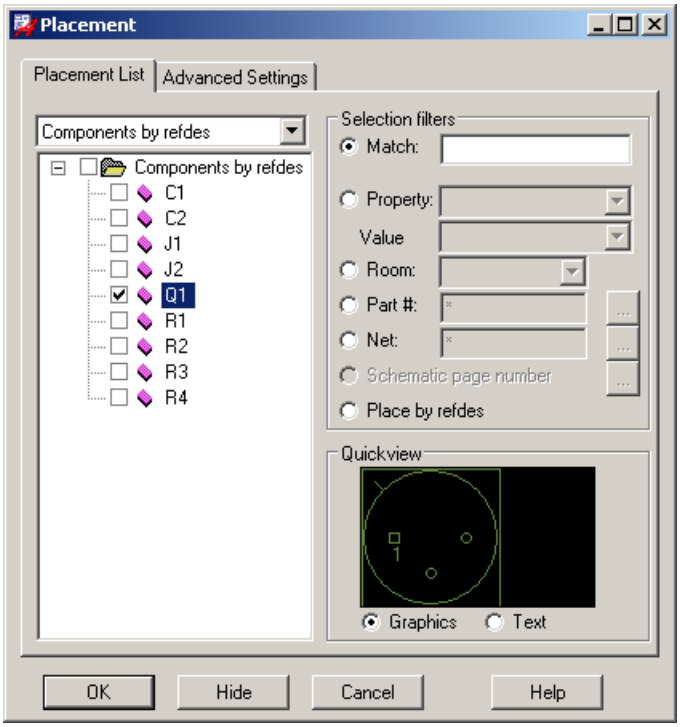


Figure 9. The Placement dialogue box, showing the components for the one-transistor amplifier. Transistor Q1 is ready to be placed on the board.

- Use the commands under the View menu or the corresponding buttons and shortcuts. Zoom Fit fills the window with your complete design, which is often helpful.
- The scroll wheel of the mouse zooms in and out, centred on the current position of the pointer.

The WorldView window can also be used to zoom and pan. If you drag a rectangle here, that becomes the area shown in the main window.

I could write a lot more about the interface but it is more fun to place the components and route the PCB.

5.3 Place and arrange the components

Choose Place > Manually... from the menu bar to start placing the components. This brings up the Placement dialogue box shown in figure 9. The Placement List tab should be active and the list should show Components by refdes with the components in your design listed below.

It is straightforward to place the components for this simple design. See figure 10 on the following page for guidance.

1. Start with the transistor. Click the box next to Q1 in the Placement dialogue. Its outline appears in the Quickview box.
2. Move the cursor out of the Placement box on to your design. The outline of the transistor is attached to the cursor. Left-click to place it centrally on your board. The outline will be filled in and a small P for 'placed' appears in the Placement box next to the refdes.

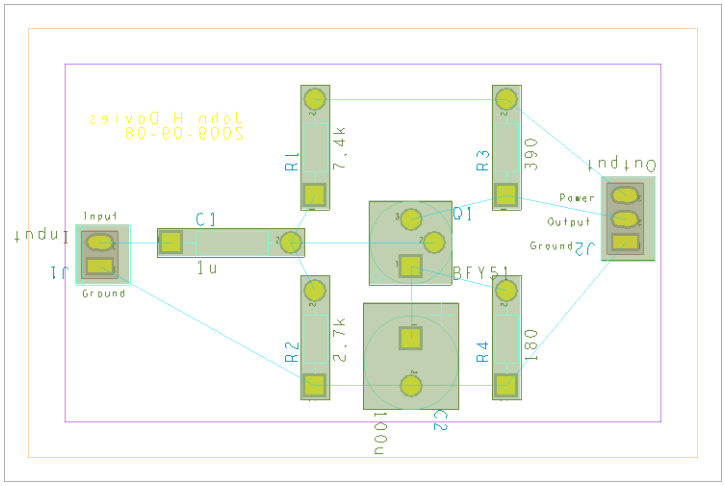


Figure 10. Screenshot of the board for the simple, one-transistor amplifier after all components have been placed and arranged. Cyan lines of the ratsnest show the connections between components.

3. Place the connectors for input and output next. Select the boxes for both J1 and J2. Move the mouse onto the design and a two-pin header for J1 appears on the cursor. Click somewhere near the left-hand side to place it. Don't worry about its orientation for now.

4. The outline of J2 now appears automatically on the cursor; place this on the right-hand side.

5. Next place the four resistors. Put them in the same positions relative to the transistor that they have on your schematic drawing. This makes the circuit easier to wire. Refer to your schematic drawing to identify each resistor.

   Keep all components inside the inner purple rectangle, which shows the Package Keepin. It turns green if you try to place any part of a component outside it.

6. Place the two capacitors in the same way. This completes the placement so dismiss the dialogue box.

The components are joined by a set of cyan lines called the *ratsnest* to show their logical connections. These lines will be turned into copper tracks when you *route* the board. The lines of the ratsnest simply take the shortest path between components and therefore cross other lines. Real tracks cannot do this. It is therefore vital to adjust the orientation and position of the placed components to reduce the number of crossings in the ratsnest and make routing easier.

Before doing this, experiment by moving the mouse around the design window without clicking. Elements of the design are highlighted and an explanatory note appears as the mouse passes over; there is no need to click on an object to highlight it as in many drawing programs. If you hover the cursor over the outline of the transistor, for example, the message Component Instance "Q1" is shown. The mouse may highlight the outline of a component, its pins, text or lines of the ratsnest. How can we be sure to move a *complete* component, not just a part of it? Moving a pin by itself would be a seriously bad idea, for example.

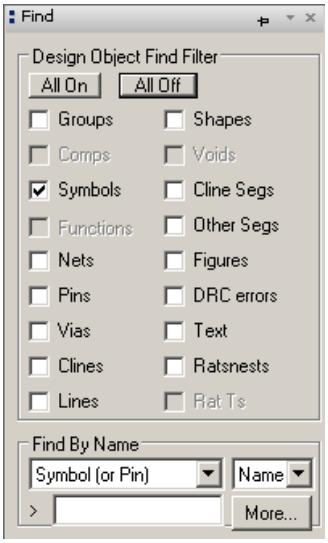


Figure 11. The Find control panel set up so that only symbols can be selected.

This is where the Find control panel is useful. Open it by moving the mouse over its tab if it is not pinned open already, click the All Off button, then select Symbols as in figure 11. Only complete symbols for components are now highlighted under the mouse. Individual pins are no longer selected, for instance. This makes it much easier to move and rotate components.

- The simplest way of moving a component is to left-click on it and drag, holding the mouse down.
- Alternatively, move the mouse over a component, right-click and choose Move from the contextual menu. Left-click in its final location.
- To rotate a selected component, right-click, choose Spin and move the mouse around to get the desired orientation.
- Both of these actions can also be chosen from the Edit menu and the toolbar has a Move button.
- Do *not* use the Mirror command, which is different from the commands in Capture. Here it moves the component from the top to the bottom of the PCB. This design is not that ambitious.

Move and rotate the components to simplify the ratsnest. This design is easy because no crossings are required if you follow the schematic drawing, which makes routing trivial.

When you have placed and arranged all the components, update the design rules check by choosing Tools > Update DRC from the menu bar. The DRC block near the bottom right of the window turns green and the Command window shows No DRC errors detected if everything is correct. If you have placed a component outside the keepin, for example, the message would be DRC done; 1 errors detected. The error is shown by a tiny red 'butterfly' marker on the design. Move the component inside the keepin and the marker disappears.

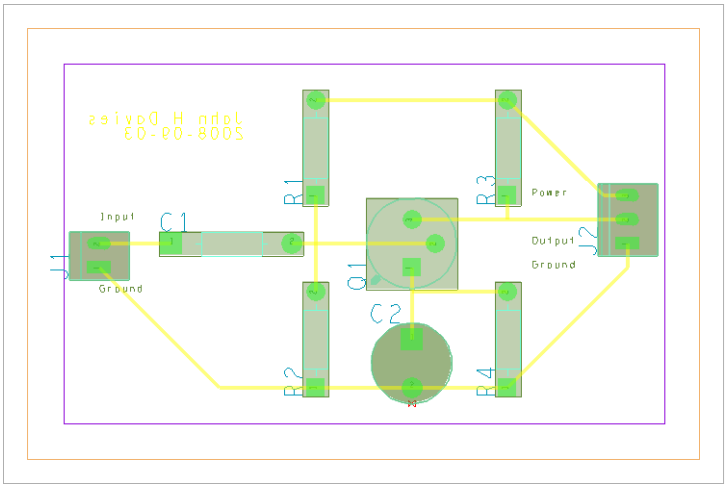


Figure 12. Screenshot of the routed board for the simple, one-transistor amplifier. The tracks are yellow, which shows that they are on the bottom of the board. Your screen may not match this image exactly because it depends on which classes are active at the time.

Save your design with a new name for the populated board. Unusually, Allegro asks you if you wish to overwrite an existing file when you Save it. You may wish to save successive versions under different names in case you need to go back and repeat a step. Allegro does not save backups automatically.

5.4 Route the board

The electrical connections depicted by the ratsnest must now be replaced by copper tracks on the PCB. This procedure is called *routing* the board. The layers of copper are called *etch* in Allegro because of the usual manufacturing process. Tracks should be drawn on the bottom of the board with the components on the top (where they go by default). The wires from the components pass through the holes in the pads and are soldered to the tracks on the bottom of the board.

Jargon: *cline* is short for *connecting line*, a segment of a copper track. A plain line may show the edge of the board or the outline of a component and is not a conductor.

Keep the layout of tracks as straightforward as possible – imagine that you are soldering the board yourself. Do not make life difficult by running tracks unnecessarily close to pads, for instance. You should aim for something like the layout shown in figure 12 but there is no need to follow this precisely.

Draw the tracks as follows. Before starting, check that no objects are selected (left-click outside the board or right-click and choose Selection Set > Clear All Selections) and that no tool is active (right-click and choose Done if it is offered). Pin the Find and Options control panels open, which makes it easier to control the tools.

1. Choose Route > Connect from the menu bar.

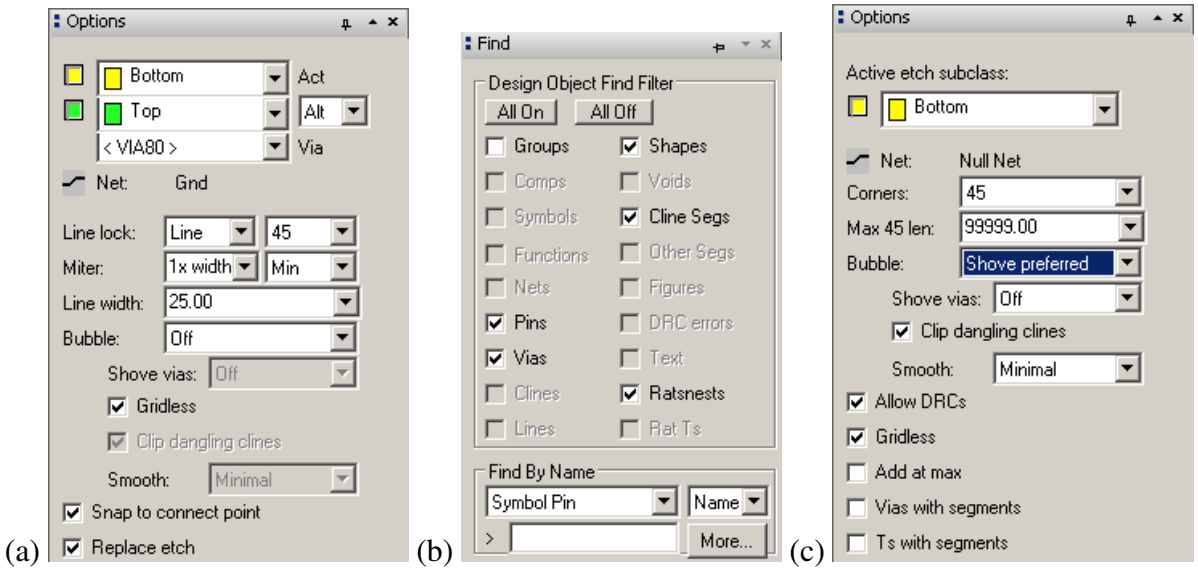


Figure 13. (a) Options and (b) Find control panels for the Add Connect command, and (c) Options for Slide.

2. The Options control panel changes to reflect the current activity and it now shows the layers available for routing. We want all the tracks to go on the bottom of the board so change the Act (active) layer to Bottom, which is painted yellow. You can also change the Alt (alternate) layer to Top, which is painted green, but we need only one layer for this circuit. Line lock should be 45 (degrees), which determines the allowed change in direction of a track. See figure 13(a).

   The Find control panel (figure 13(b)) is automatically configured to select the relevant objects for routing: pins, vias, shapes, cline segments and ratsnests. (*Shapes* are typically areas of etch, which is why they are active.)

3. Left-click on a pin to start routing a segment – the part of a track that runs from one pin to another. A segment of the ratsnest highlights to show that it is available for routing.

4. Move the mouse towards the pin at the other end of the highlighted ratsnest. A thick yellow line is drawn to show the copper track and replaces the line of the ratsnest.

5. Click at intermediate points to fix corners. These automatically turn through 45°, which is good practice. It is a bad idea to draw 90° corners because they are prone to breakage during etching.

6. Click on the destination pin to complete the track.

7. Repeat to route all segments of the ratsnest. Right-click and choose Done when you have finished.

Run a design rules check to detect any problems with routing. For further details, choose Display > Status... from the menu bar. The section on Symbols and nets should show that everything has been placed and routed, while DRC errors should be shown as Up To Date with no errors. Save your board.

Oops! – I made a mistake

There are several ways of undoing an error.

- Right-click the mouse and choose Oops. This undoes the most recent partial action, such as drawing the last segment of a track.
- Right-click and choose Cancel, which undoes the last complete action.
- Try Edit > Undo to go further back.
- If you have made a complete mess, go to the menu File > Recent Designs and reload your design *without* saving changes (there is no Revert to Saved command). This abandons all changes since you last saved the file, which I hope was not too long ago. . . .

My tracks don't look very good: How can I improve them?

PCB Editor offers many ways of adjusting the tracks. First make sure that you are not still using the Connect tool by right-clicking and choosing Done if this appears on the contextual menu. Small adjustments to routed tracks can be made with the Route > Slide tool, which loads the Options control panel as shown in figure 13(c) on the preceding page. I suggest that you change Bubble from its default of Shove preferred, because this encourages Allegro to move tracks around in a startling manner; Hug only is more gentle. Click and release the mouse button on a segment to select it, slide it around and click again when you are satisfied with the result. Other helpful tools include Edit >Vertex and Edit > Delete Vertex.

For larger changes, you might wish to remove part of a track or the complete track and redraw it. Proceed as follows.

- Move the mouse over a cline segment, which should highlight. If it does not, open the Find control panel and choose All On.
- You can delete the etch at three levels using the contextual menu:
  - Delete removes the segment – a single straight line of track between corners or pins.
  - Connect Line > Delete removes the complete track (cline) between the two nearest pins or junctions.
  - Net > Ripup etch unroutes the complete net.
- Use Route > Connect to redraw the track.

This nicely illustrates the way in which PCB Editor allows a hierarchy of selections: just a segment, a complete line, or the whole net.

Aaarghh! – I've just spotted an error in the circuit

If you spot an error in the circuit, rather than the layout, follow the instructions in section A on page 47. You can correct the schematic drawing in Capture and send a new netlist to PCB Editor, which makes only the minimum number of alterations to your board. It is *not* necessary to repeat the whole layout. This is one of the advantages of computer-aided design.

5.5 Add text

Next add some text to the board to make it easier to fabricate and use. In particular, all connectors (headers) must have the function of each pin identified as on the schematic. Your name would be useful too. There is no need to add a label for each component because the refdes and value are shown automatically. Text and the outlines of components are printed on a commercial board using ink or paint as a layer called the *silkscreen*. We cannot produce a silkscreen in the university and text must therefore be placed on the copper layers.

1. Start by putting your name on the board, which is always a good idea if you want to claim it. Choose Add > Text from the menu.

2. Use the Options control panel to select the destination for the text. You are probably getting the hang of the interface by now: choose a command, select options, then do it.

   - Put essential text such as your name on the bottom layer of copper because this is part of every board. The Active Class should therefore be Etch and the Subclass should be Bottom.
   - Text on the bottom of the board should be mirrored so that it reads correctly from below, so select the Mirror box.
   - Text block is a confusing way of specifying the size of text. A larger number for the block produces larger text. Something like 4 is about right for your name.

3. Click in the design where you would like the text and type. Hit Return (Enter) to get a new line. Click to begin a new block of text elsewhere or right-click and choose Done when you have finished.

4. Now add some text on top of the board to identify the connectors. Again choose Add > Text but this time set the active class and subclass to Etch/Top. Turn off the mirroring and reduce the size to 2.

   Add text for Input and Ground near the input connector and Power, Output and Ground by the output connector. Keep the text away from the pads: It is printed in copper and could cause a short circuit.

Congratulations! – you have finished your first PCB. Don't forget to save it.

5.6 Print the design

The simplest way of printing the design is to 'plot' it (the usage goes back to the days of pen plotters). Select File > Plot Setup... from the menu and choose the following settings.

- Usually the Plot scaling should be unity so that the size of the printout matches that of the PCB. This board is so simple that it is better to enlarge the drawing so enter 2 instead.
- Change the Default line weight to 10, otherwise the outlines are thin and indistinct.
- Select Auto center under Plot orientation.
- Set the Plot method to Color and close the dialogue box.

Open the Options control panel and set the active class to Etch/Bottom. This emphasizes the most important features. Now print your layout with File > Plot....

- Click on the Setup... button. Check that the paper size is correct and is in landscape orientation. Confirm also that the correct (colour) printer is selected.
- Choose OK to print your layout.

The image should resemble figure 12 on page 23 except that colours on the plot are opaque. Stick the output in your laboratory book.

This plot is not useful for manufacturing the PCB. In the next design I'll show you how to get printouts that can be used to make your PCB in the university.

☛ **Milestone**: Ask a member of staff to assess your finished design.

6 Instrumentation amplifier – single-sided board

The second design is another classic circuit, shown in figure 14 on the next page. This is an *instrumentation amplifier* based on three op-amps. You will study its operation in Analogue Electronics 2. Its main characteristics are as follows.

- Both inputs have a high input resistance because each is connected directly to the non-inverting input of an op-amp.
- The third op-amp acts as a subtracter to pick out the difference between its inputs (it can provide gain as well but I have chosen not to do this).
- The gain for *differential* signals (the difference $V_+ - V_-$) can be adjusted with the single resistor R_2.
- The gain for *common-mode* signals (where $V_+ = V_-$) is very low.

The circuit is used to amplify a small difference in voltage between its two inputs while rejecting a large background or noise voltage that affects the two inputs equally. This is often needed with sensors, so remember this in Team Design Project 3. It may also be helpful later this year.

In practice it is unlikely that the circuit would be built using three separate packages with single op-amps as in this design. Complete instrumentation amplifiers are available in 8-pin packages. Even if these were unsuitable, a quad package that contains four op-amps could be used although these lack the pins for trimming the offset voltage. We shall not simulate this circuit, just lay out the PCB. The LF411 is a widely used op-amp.

6.1 Schematic capture

Create a new directory for this design, as always, and start a new project in Capture. Place the components on the schematic but do not connect them yet. The only unfamiliar component should be the potentiometer, which is called POT – search for it.

Power supply rails are normally hidden to simplify schematic drawings. Here the power pins of the op-amps are connected to named *power symbols*. Capture considers all power

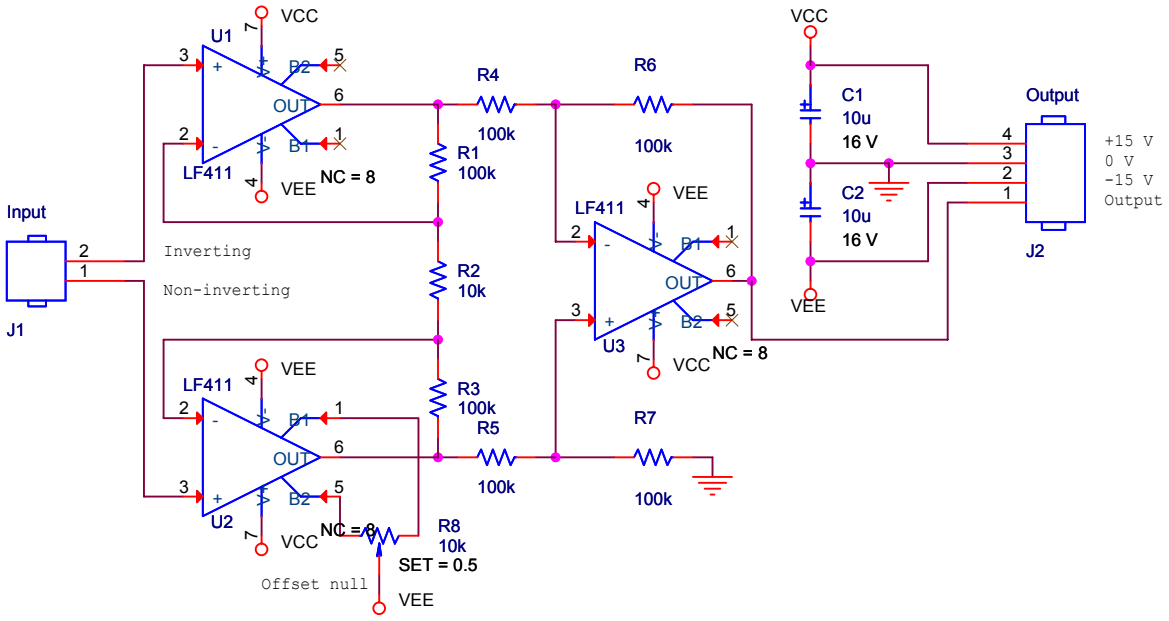


Figure 14. Instrumentation amplifier based on three op-amps. The label NC = 8 on the op-amps is not normally visible and will be explained later.

symbols with the same name to be connected together. Ground (earth) symbols work in the same way. (Often the power pins themselves are hidden, as we'll see in the final design.) Connect the power supplies as follows.

1. Select Place > Power... or click the power symbol button on the toolbar and select VCC_CIRCLE from the CAPSYM library. Use the same symbol for both +15 V and −15 V supplies. Place one near each power pin, mirror it vertically if necessary and connect it to the pin with a short wire.

2. Double-click the name of each power symbol in turn and change the name to VCC for positive and VEE for negative supplies respectively. This is a standard usage (but there are many others). Check the orientation of the op-amps carefully! Some are mirrored vertically to make the circuit clearer and this reverses the power connections as well.

3. In the same way, select Place > Ground... or click the ground button. Use GND from CAPSYM for the ground (earth) symbols. These symbols must have the same name throughout your drawing or they will not be linked.

Wire the components and add text to identify the pins of the two connectors.

Two of the op-amps have unconnected pins. This is deliberate because they are for offset adjustment and it is only necessary to do this on one op-amp. PCB Editor must be told about this, otherwise it assumes that you omitted the connections by mistake and flags an error. Show that the pins are deliberately unconnected by choosing Place > No Connect from the menu bar or clicking the button, then clicking on the pins. A small cross appears as in figure 14. PCB Editor requires every pin to be connected or explicitly marked as not connected.

Next enter the footprints. *You must work out which to use for yourself.* The real components are available in the laboratory and you must match them to the catalogue of our local library,

which is shown at the end of this handout. It is best to install ICs in sockets for student projects, rather than soldering them directly to the PCB, so choose one of the GU-DIPSOCK footprints for the op-amps.

Fixup. Incompatibilities between Capture and PCB Editor must again be corrected before making the netlist. First, the pins of the electrolytic capacitors are wrongly numbered. Repeat the instructions in section 4.1 on page 9 to fix this. ❦

Fixup. A new problem is that only 7 pins are defined on the electrical symbols for the op-amps but the package has 8 pins. You might hope that the software would assume that undefined pins are not connected but it does not: It must be told this formally.

1. Select one of the op-amps and choose Edit > Part, which brings up the Part Editor.
2. Choose Options > Part Properties. . . , which brings up the list of User Properties.
3. Click the New. . . button. Give the new property the name NC, which stands for No Connect, and the value 8, which is the number of the unconnected pin. (Use a list separated by commas, such as 7,8, if more pins are not connected.)
4. Click OK to get rid of the dialog boxes and close the Part Editor. Choose Update All so that this change is applied to all LF411 parts in your design.

The NC property was made visible on the schematic in figure 14 on the preceding page, which therefore shows NC = 8, but you need not do this. ❦

Run a Design Rules Check and correct any errors. Print your schematic when it has been completed and survived the DRC.

☛ **Milestone**: Have your drawing checked before you go any further.

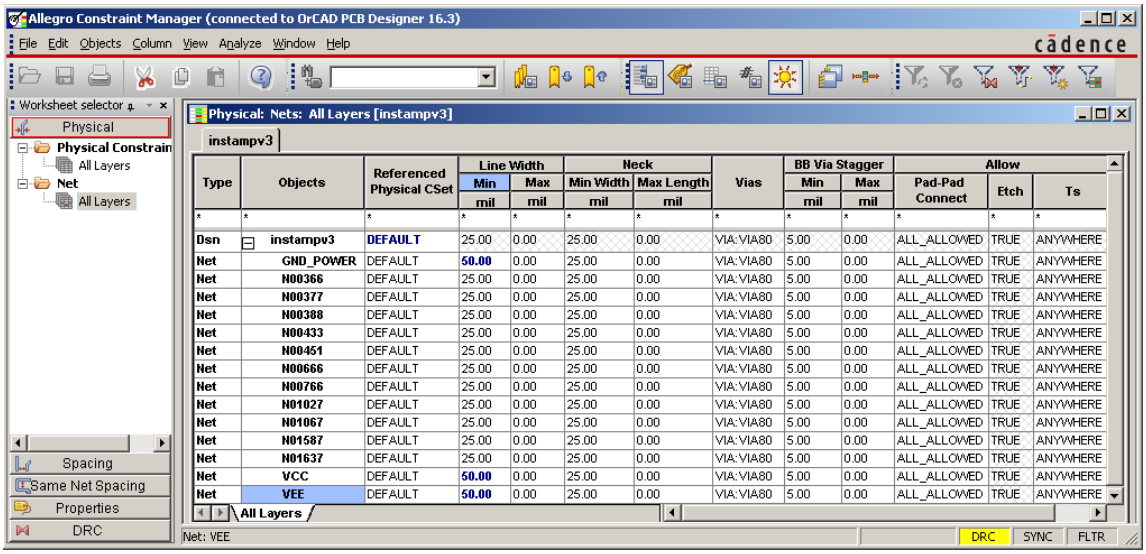
6.2 Create the PCB and place the components

Remember to make an allegro directory first. Set up the board as before (section 4.4 on page 13) but make it $3.5'' \times 2.5''$, which gives you plenty of room for the larger number of components. Save the board and quit from PCB Editor. Back in Capture, create a netlist and send the design to PCB Editor as before. Check the Session Log: Ignore any warnings about RVMAX but investigate any others.

We'll place the components using a different technique this time. Choose Place > Quickplace. . . from the menu bar. The defaults should be suitable (Place all components, Around package keepin, Top). Click Place then OK. Your components are now arranged at the top of the board, ready for you to move them into position.

Move the components onto the board, arrange them to resemble the schematic drawing and adjust them to make the ratsnest simple with as few crossings as possible (it is not possible to eliminate all of the crossings). *This step is really important.* It is easy to route the tracks on a well-placed board; conversely, a poorly-placed board needs long, convoluted tracks or may even be unroutable.

Run a Design Rules Check when the components have all been placed and save your board.



Type	Objects	Referenced Physical CSet	Line Width Min	Line Width Max	Neck Min Width	Neck Max Length	Vias	BB Via Stagger Min	BB Via Stagger Max	Allow Pad-Pad Connect	Allow Etch	Allow Ts
			mil	mil	mil	mil		mil	mil			
*	*	*	*	*	*	*	*	*	*	*	*	*
Dsn	instampv3	DEFAULT	25.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	GND_POWER	DEFAULT	50.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	N00366	DEFAULT	25.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	N00377	DEFAULT	25.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	N00388	DEFAULT	25.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	N00433	DEFAULT	25.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	N00451	DEFAULT	25.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	N00666	DEFAULT	25.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	N00766	DEFAULT	25.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	N01027	DEFAULT	25.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	N01067	DEFAULT	25.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	N01587	DEFAULT	25.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	N01637	DEFAULT	25.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	VCC	DEFAULT	50.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	VEE	DEFAULT	50.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE

Figure 15. Constraint manager after changing the widths of the three power nets but before correcting the vias.

6.3 Add mounting holes

Most PCBs need to be mounted inside a piece of equipment and therefore need holes for fixings. Mounting holes and similar features are called *mechanical symbols* and are placed in a slightly different way from electronic components because they are not part of the netlist.

1. Select Place > Manually... to open the Placement dialogue box, bring the Advanced Settings tab forward and choose to Display definitions from Library. This is necessary because the symbols are not in the database imported from Capture.

2. Return to the Placement List tab and select Mechanical symbols from the drop-down list.

3. Use the same procedure as before to place a GU-MOUNTING156 symbol near each corner of the board. This is a hole of diameter 156 mils or $\frac{5}{32}''$. Do not place the holes too close to the edge or the board may break when it is drilled.

Mounting holes are shown on my routed PCB in figure 20 on page 35.

6.4 Preparation for routing

Power tracks are usually made wider than signal tracks because they have to carry more current. Our tracks are already so wide that it's barely necessary but we'll do it for future reference.

1. Choose Setup > Constraints > Physical... from the menu bar. This brings up the Constraint Manager and a Tip of the Day if you are unlucky (sigh).

2. The left-hand part of the window shows the various properties that can be edited. Click on All Layers under Net. See figure 15 on the previous page for guidance.

3. The main part of the window now shows a list of the nets in your design. Most of them have random-looking numbers, such as N00451, but a few are named. These are the nets that carry power, to which we assigned names in Capture: VCC, VEE and GND or something similar, depending on the symbol that you chose.

4. Change the minimum width for these three nets from 25 to 50 mil.

5. Choose File > Close to return to PCB Editor.

Save a copy of your board before routing so that you can use it for double-sided routing.

6.5 Autorouting a single-sided board

The instrumentation amplifier is simple enough that it is easy to route the tracks by hand. However, manual routing is impracticable for large boards and we shall therefore use the OrCAD PCB Router to gain experience of the procedure. You will do this twice: first as a single-sided board, as in the one-transistor amplifier, and later as a double-sided board. It is possible to route all tracks on the single-sided board if you have laid it out well but the double-sided board should have a simpler layout with a smaller total length of track.

Two approaches are available for automatic routing, both shown in figure 3 on page 10. Everything can be done from within PCB Editor or you can run PCB Router as a separate application. The first is more convenient (when it works) but the second offers finer control.

Autorouting from within PCB Editor

Choose Route > PCB Router > Route Automatic... from the menu bar. This brings up the Automatic Router dialogue box shown in figure 16 on the next page. Unfortunately it often causes a fatal error message similar to SPECCTRA quit unexpectedly with an exit code of 3, in which case you must use the second method – jump to the next heading.

Select Use smart router for the Strategy. For a single-sided board deselect the box next to the TOP Routing Subclass. You might wish to experiment with the Routing Direction for the bottom layer. Click Route and wait for the results to come back. Use the Results button to get a report on the routing and check the Completion percentage to ensure that all nets were routed successfully. Confirm this with Display > Status... and save your board.

If you can't locate DRC errors, choose Tools > Quick Reports > Design Rules Check Report from the menu bar. This gives a table of all errors including hyperlinks to their location.

After all tracks have been successfully routed, choose Route > Gloss... from the menu bar. *Glossing* means to tidy up the design. This includes spreading tracks apart where possible and replacing 90° corners by 45° bends (mitering). Accept the defaults and gloss your design. Finally, use Tools > Quick Reports > Etch Length by Layer Report to find the lengths of the tracks and add them up. In general, a better design has shorter tracks.

Autorouting with OrCAD PCB Router

Use the manual equivalent of the flow described in the previous section if automatic routing does not work from PCB Editor. It's a bit clumsier but gives better control over the process and makes it easier to experiment with different settings.

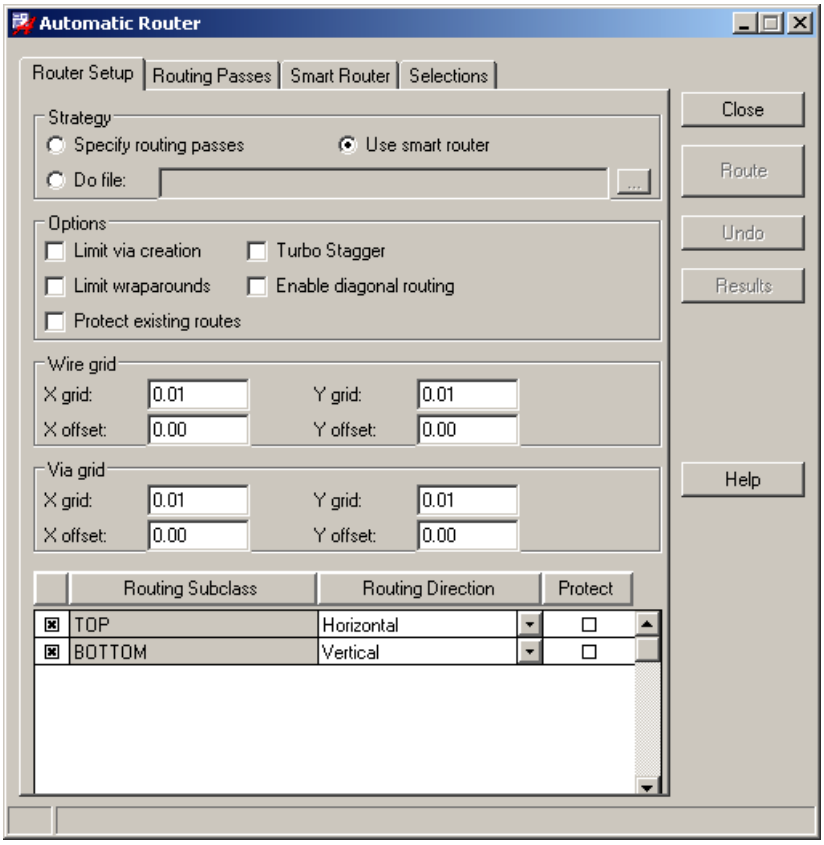


Figure 16. Dialog box for running the autorouter from within PCB Editor.

Note. At some point you may get a Licensing Error warning from PCB Router. Click Ignore Feature for This Session if it appears. ❦

1. Choose File > Export > Router from the menu bar of PCB Editor. It asks you for a name for the Auto-Router Design file and you can probably accept the suggestion. Click Run. You may be warned about overwriting the file, which isn't a problem. A message Translation Completed should appear, after which you can close the box.

2. Start OrCAD PCB Router from the Windows Start menu. You are presented with the fairly complicated dialogue box shown in figure 17 on the following page. Use the Browse... buttons to open the following two files.

   - For the Design / Session File (the first), choose the file that you just exported from PCB Editor.
   - For the Do File (the last), choose the file with _rules appended to the name of your board file.

   Click Start Allegro PCB Router to dismiss the box. PCB Router starts and you should now see your components joined by the ratsnest within the outline of the route keepin as in figure 18 on the previous page. Some components have shaded footprints, which I'll explain later.

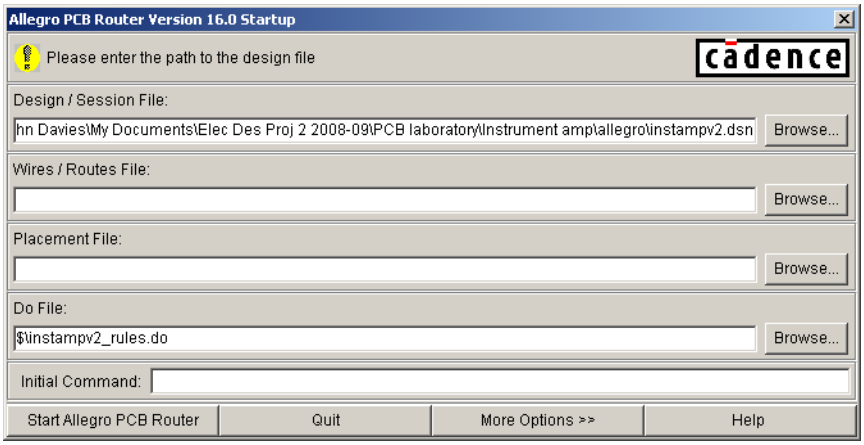


Figure 17. Startup dialogue box for importing a design into PCB Router.

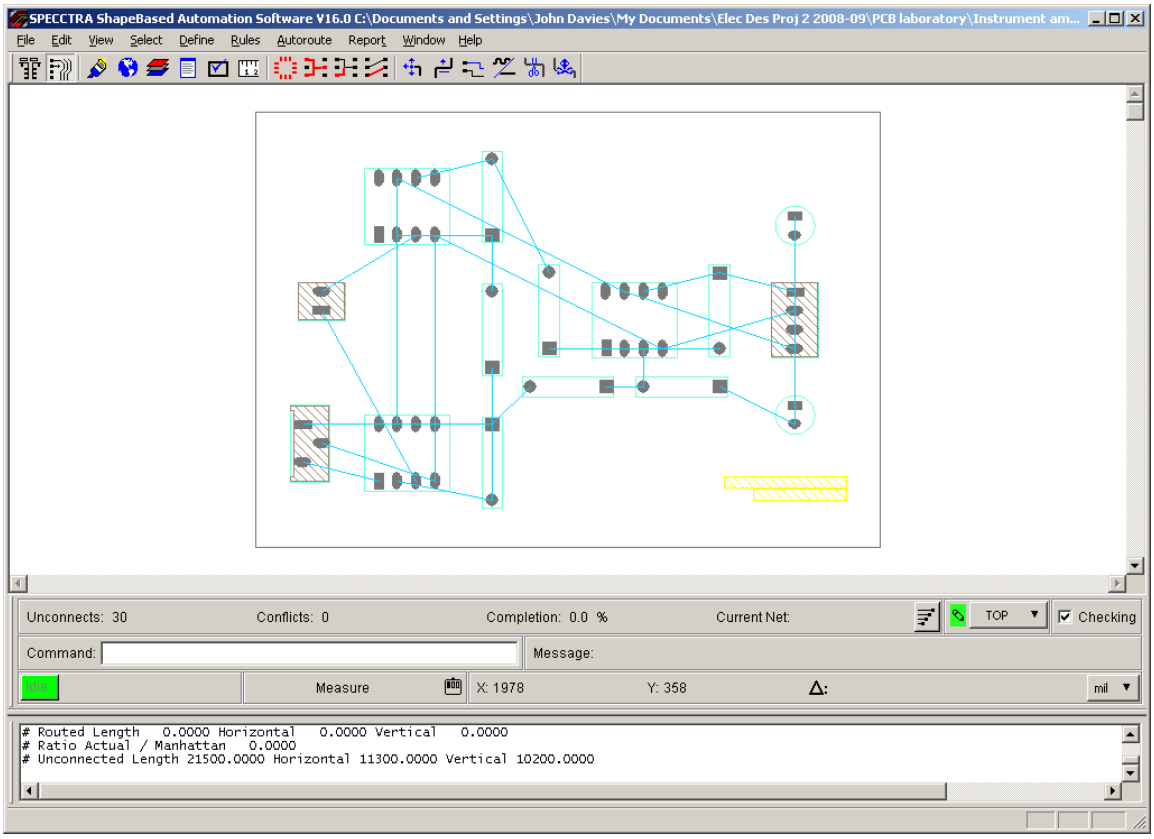


Figure 18. Screenshot of PCB Router, ready to route the instrumentation amplifier. I have changed the background of the window to white for a clearer printout.

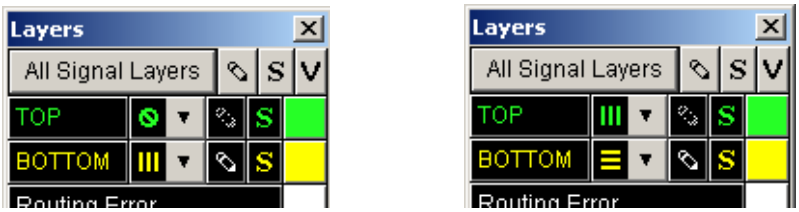


Figure 19. Settings in the Layers box for single-sided routing on the bottom layer and double-sided routing on both layers.

3. Tell PCB Router to route only the bottom layer. Choose View > Layers... from the menu bar. Turn routing off for the top layer by clicking on the drop-down menu next to TOP as shown in figure 19 and selecting the ⊘ symbol. You might like to experiment with the setting of the BOTTOM layer. The directions are hints to the router but in practice tracks will be drawn in both directions. Click Close when you have finished.

4. Choose Autoroute > Route.... Leave Smart selected and click OK. The autorouter will work away and you will see Message: Smart_route finished, completion rate: 100.00% if all is well. The tracks should be in colour, yellow for the bottom, if they are routed successfully. Sometimes they are drawn white, which should indicate a design rules error, even when they appear to be correct – I don't know why.

   See the suggestions below if the autorouter is unable to route your board.

5. Two further commands improve the tracks for assembly. First choose Autoroute > Post Route > Spread Wires... and accept the defaults. This spreads the tracks away from each other and from the solder pads.

6. You'll have noticed that the autorouted board has 90° bends in the tracks, which I told you to avoid when you routed the board by hand. We'll now sort this out. Run Autoroute > Post Route > [Un]Miter Corners... and accept the defaults. The corners will be rounded off and tracks run diagonally where possible.

7. To see the details of the finished layout, choose Report > Route Status. This will show a lot more than you want to know! Look near the bottom and confirm that the Unconnected length is zero. Record the Routed length in your notebook.

8. Choose File > Quit... and agree to Save and Quit. This writes a *session* file that describes the routed tracks.

9. Return to PCB Editor and choose File > Import > Router.... Locate the Session File whose name matches your board and click Run. You should see a message Translation Completed. Close the box.

10. The window now shows your design with tracks instead of the ratsnest. Save it under a different name to preserve the unrouted board for later.

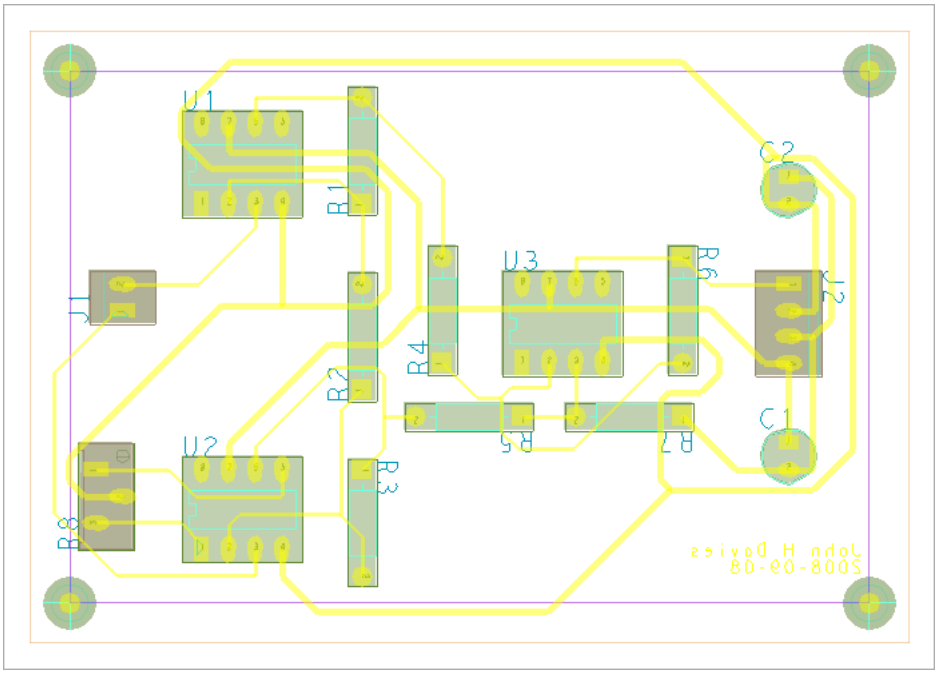


Figure 20. My one-sided layout after autorouting. The total routed length was 29.3″.

Help! – My board won't route

Here are some suggestions for helping the autorouter.

1. If routing has almost worked (only one or two unrouted segments), try changing the hints given to the router. For the one-sided board there is only the suggested direction of tracks. It is best to unroute the board and begin afresh. Choose Edit > Delete Wires > All Wires from the menu bar of PCB Router or reload the unrouted version of your board in PCB Editor.

2. If you are far from success, look at the layout to see where the problems lie. Often one particular track prevents successful routing. Can you rearrange the components to solve the problem?

   Quit from PCB Router *without* saving, or reload the previous version of your board in PCB Editor. Rearrange or reorientate components to make the ratsnest simpler and ease the problem before trying the autorouter again.

If none of this works, get advice from a demonstrator.

6.6 Final touches

Put your name on the bottom etch layer, run a final design rule check, save your routed board and make a coloured plot as before. My layout is shown in figure 20 on the previous page. It is a poor board in many respects despite the successful routing. The power tracks are excessively long in particular. It is not hard to see how the components could be rearranged to improve the layout.

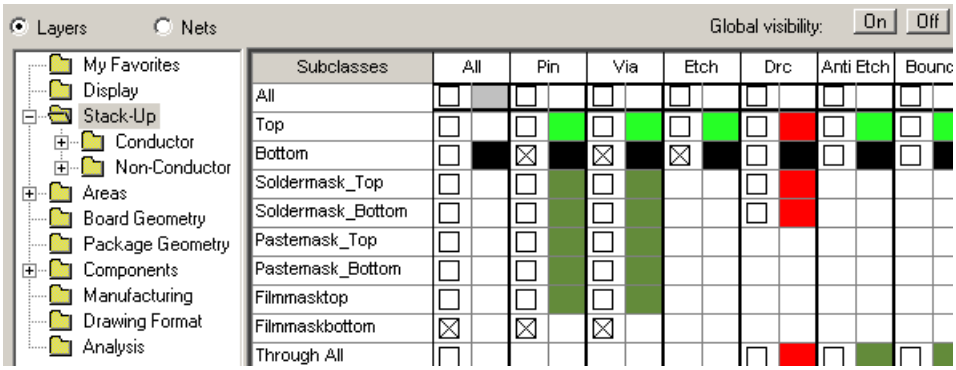


Figure 21. Part of the Color Dialog box, showing the settings for the Stack-Up to plot the bottom layer.

6.7 Photomask

This section explains how to get a black-and-white plot that can be used as a photomask to manufacture your board in the university. I'm afraid that the procedure is complicated because Allegro is not intended for such a primitive process. A further difficulty is that we need holes in the pads to guide the drill. The general idea is to hide unwanted elements of the design and to colour the desired features black. *Save your design first.*

1. Open the Color Dialog box with Display > Color/Visibility... from the menu bar.

2. Click the button to turn Global Visibility Off, agree to Make all classes invisible in the small dialogue and click Apply in the main dialogue (this is needed after every change to see the effect). The design vanishes from the design window.

3. Click the Display folder in the list on the left. We must change the Background colour of the window so that tracks show up after their colour has been changed to black. Click on the white swatch in the Color swatches (samples of each colour) near the bottom of the window, then click the swatch next to Background, which turns white. Click Apply to update the design window, which also turns white.

4. Now we need make the desired features visible again and paint them black. Start by selecting Board Geometry from the list on the left. This brings up a set of Subclasses to the right. Select the checkbox next to Outline to turn it on. Change its colour to black by clicking in the black swatch in the Color region, then the swatch next to Outline. Finally, click Apply and the board outline becomes visible in the design window.

5. This must be repeated for all the features that we wish to print. For the bottom of a PCB these are Stack-Up/Conductor/Bottom/Pin, Via and Etch. Activate and make them black as shown in figure 21 on the preceding page. Click Apply and your tracks appear.

6. Finally we must make the drill holes white. They are normally hidden in a layer called the filmmask, which must be made visible. Click All for Filmmaskbottom to activate it and change its colour to white. Click OK to close the Color Dialog.

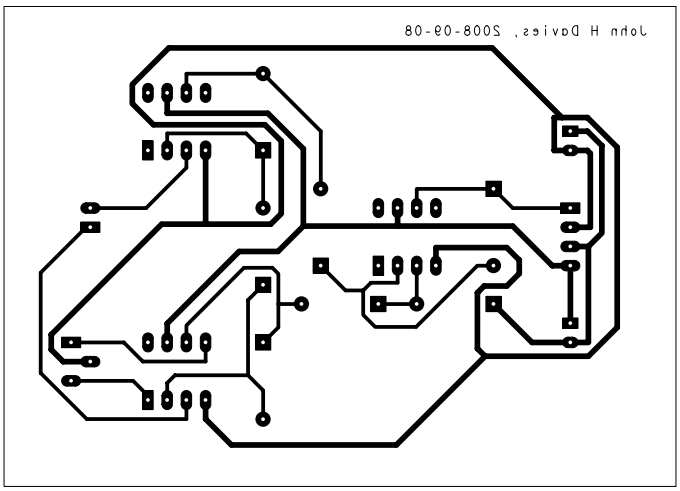


Figure 22. Printout at actual size for manufacturing a single-sided board (bottom layer) with holes in the pads to guide the drill.

7. The holes do not yet appear on the screen because they are 'under' the etch. Go to the Options control panel and choose the Pin/Filmmaskbottom class, which makes it active and draws it on top of everything else. Pale holes appear on the pads as desired. This completes the bottom of the PCB.

8. Check the Plot Setup. Set the Scaling factor to 1.00 so that the mask has the correct dimensions for the finished PCB. Leave the Default line weight as 10 or text may be too thin for reliable etching.

9. Finally, choose File > Plot... as usual and you should get a beautiful picture with the board outline and etch as in figure 22.

After all this, quit from PCB Editor *without saving* (or reload your design) to avoid messing up the colours next time you use it.

☛ **Milestone**: Ask a member of staff to assess your design.

7 Instrumentation amplifier – double-sided board

We will now route the board using both sides. This makes it easier to lay out more complicated boards and the university can produce both single and double-sided PCBs. However, *use a single side for your designs wherever possible*. Many problems occur with double-sided PCBs, mostly from badly placed vias, as I'll now explain.

Figure 23 shows a cross-section of a double-sided PCB. Commercially produced PCBs have *plated-through holes* (PTHs), which means that the copper plating extends through the holes and joins the pads on the two sides of the board. A *free via* is a hole that is used purely to move a track from one side of the board to the other, rather than to mount a component. The plating carries current between the layers. Unfortunately we cannot plate through holes in the

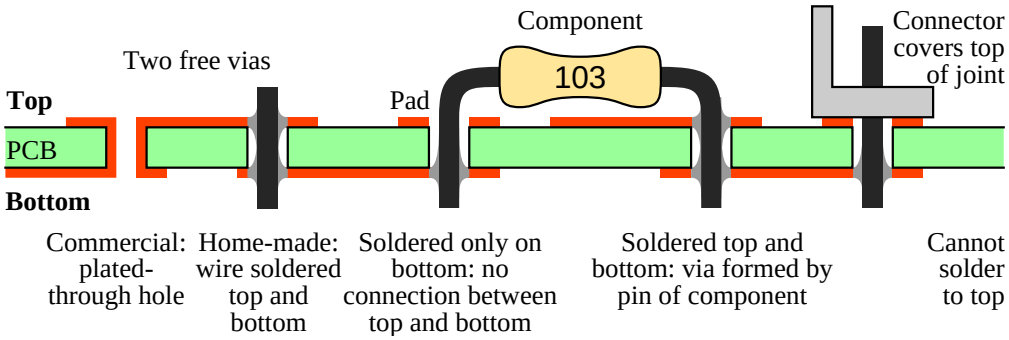


Figure 23. Cross-section of a double-sided printed circuit board showing free vias formed by a plated-through hole and a wire through a non-plated hole soldered top and bottom. A via can also be formed using a pin-through-hole component but not at a connector because it covers the top pad.

university, which means that vias need more effort: A wire must be pushed through each hole and soldered top and bottom to join the layers of etch. You may remember this from the novelty lights in Electronic Engineering 1X.

The wires of through-hole components can also be used as vias. This works well for some components, such as resistors and capacitors. However, it fails for others, such as connectors, because it is impossible to solder the pad on top of the board – it is hidden under the base of the connector. The pins of an integrated circuit can be used as vias if they are soldered directly to the board but it is safer to put ICs in sockets for PCBs that are assembled by hand and these hide the pads too. *Vias must therefore be placed with great care if the PCB does not have plated-through holes.*

To illustrate these problems, figure 24 on the next page shows a poor two-sided layout. It obeys the design rules but is hard or impossible to assemble by hand.

- The board has five free vias, far too many for a board that could be routed successfully with only one layer. The worst via is under U3, which is unacceptable for a home-made via because the wire in the via would obstruct the integrated circuit. (There would be no problem on a commercial board with plated-through holes.) Another via is very close to the trimmer (R8) and it would be difficult to solder this without damaging the trimmer. You would have to solder the via first and keep it neat.

- Several pins of resistors act as vias – R3 has two, for instance. These are easy.

- Some pins of the integrated circuits are connected to tracks on both the top and bottom. This is not a problem if the IC is soldered directly to the board but won't work if it is in a socket.

- The connectors (J1 and J2) and the trimmer (R8) have tracks only to the bottom of their pins. This is why the via is needed near R8. No tracks run to the top because the symbols for these components have *route keepouts* on the top, which forbid the router from placing tracks there. The footprints have diagonal shading in PCB Router to show this, visible in figure 18 on page 33.

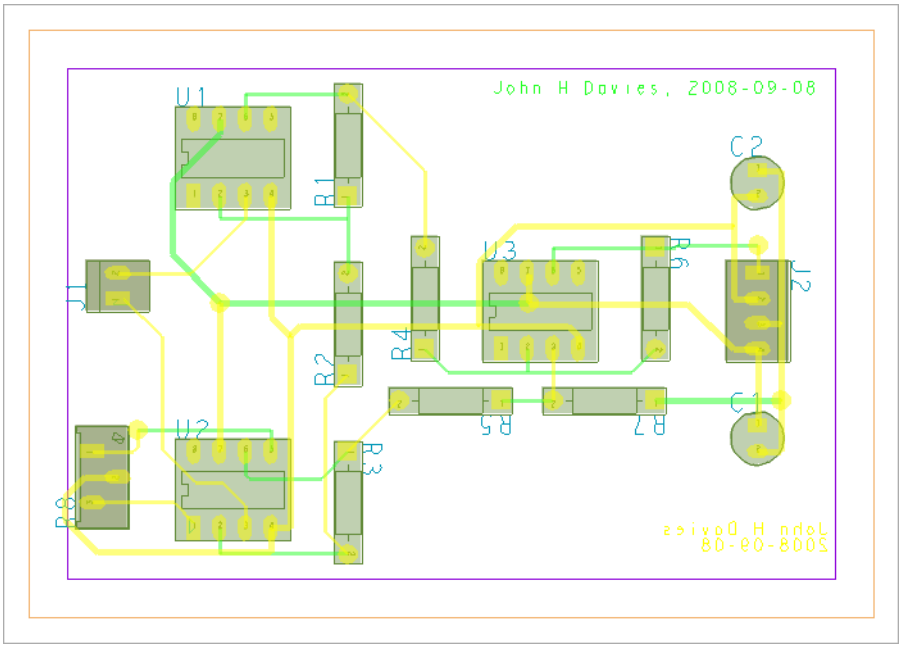


Figure 24. Screenshot of a poor double-sided layout with several badly-placed vias.

The general rule is to *avoid vias wherever possible*. Every via requires two soldered joints (top and bottom), which dramatically reduces reliability.

Re-open the unrouted version of your board and route it using both sides.

1. Remember the Default via padstack when you used the new board wizard? We specified GU-VIA80. Unfortunately another type of via called simply VIA appears in the design and is used by default. It is too small to be soldered by hand and must be removed.

   Fixup. Choose Setup > Constraints > Physical... from the menu bar. Select Physical Constraint Set > All Layers to bring up the spreadsheet shown in figure 15 on page 30. The column headed Vias for the DEFAULT row probably has VIA:GU-VIA80. Highlight this cell and choose Edit > Change.... Remove VIA from the Via list on the right and click OK. The cell now contains only GU-VIA80, which is what we want. Close the Constraint Manager and return to PCB Editor. ❦

2. The new board wizard set up several spacings based on the minimum line width of 25 mils. Unfortunately it does not set up the spacing around vias, which is only 5 mils by default. This is too small for reliable construction by hand and should be increased to match the other spacings.

   Fixup. Choose Setup > Constraints > Spacing... from the menu bar to open the Constraint Manager and select All Layers > Vias as in figure 25. Drag the mouse to select all the cells under Thru Via To in the DEFAULT row. Type 25 and hit Enter, which copies this value into all cells selected. Close the Constraint Manager and save your board. ❦

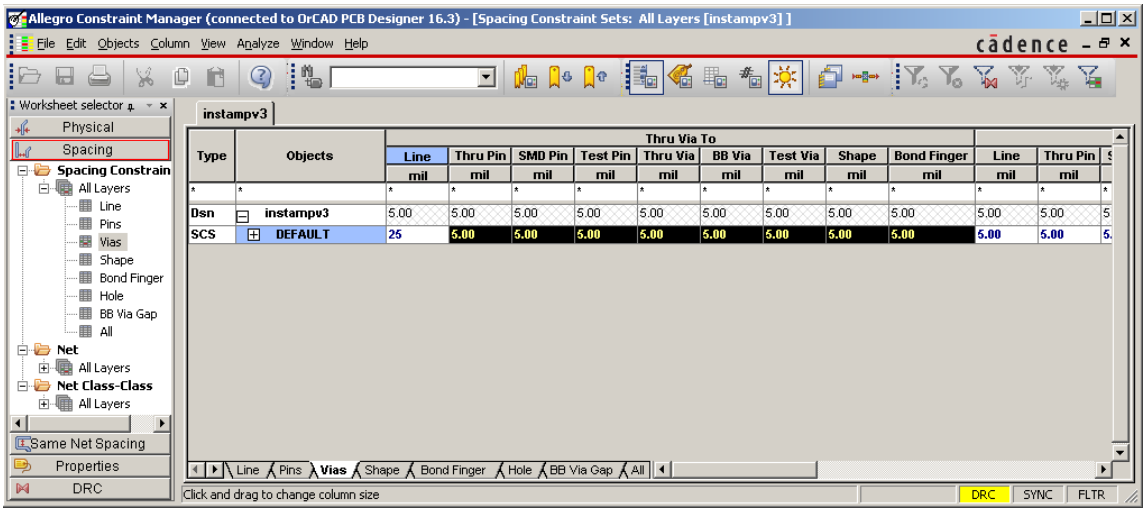


Figure 25. Constraint manager for changing the spacing around vias. The row of cells under Thru Via To has been selected and the value 25 typed into the first cell. This will fill the other cells selected after hitting the Enter key.

3. Run the autorouter from within PCB Editor or export the board to PCB Router as before. This time you should allow routing on both layers, which is the default. You might like to experiment with the directions. Note the routed length and the number of vias; a good design may have none at all, which is a bonus. Remember to gloss or space and mitre the tracks.

4. Import the tracks into PCB Editor if you used PCB Router. Save the routed board under a new name.

Move any vias in inconvenient places, such as that under U3 in figure 24 on the previous page. If you are lucky you may be able to Slide the via but it is often better to rip up the complete track and re-route it by hand. Other tracks must often be moved to create space for the via.

- Select the cline or net with the offending via, right-click and choose Delete or Ripup etch from the contextual menu.
- Select the connect tool and check in the Options control panel that the active and alternate layers are correct.
- Draw out the segments of the track as usual.
- Double-click when you reach the point where a via is needed. A via is inserted and routing switches to the alternate layer.
- Continue routing to complete the track.

I made several changes to my board to get the final version in figure 26.

- The via was moved from under U3 to a clear region of PCB.
- Another via was moved away from R8.

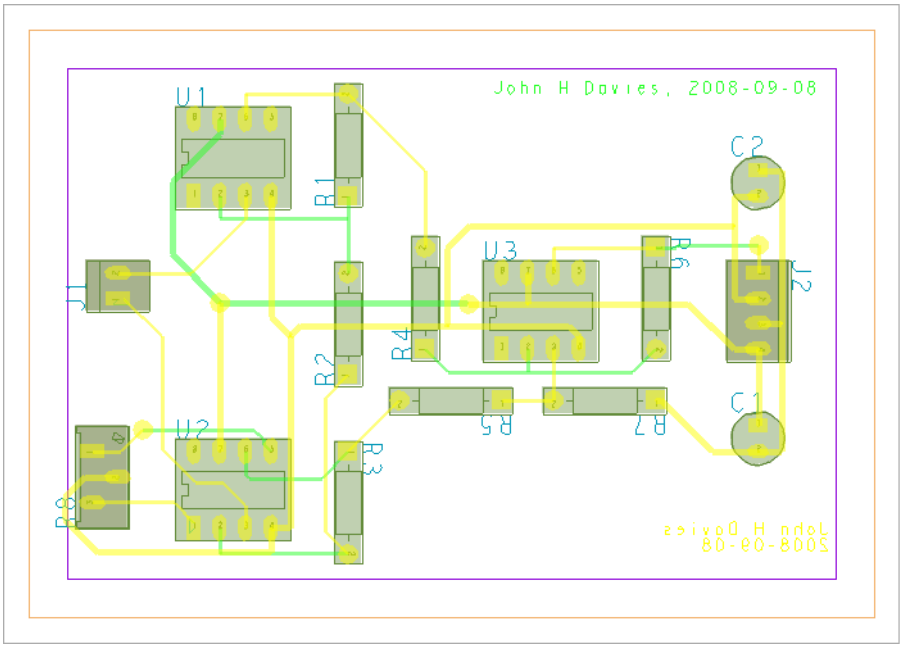


Figure 26. Double-sided layout after improving the layout and moving the badly-placed vias.

- The via near C1 was eliminated by rerouting the tracks slightly.
- Several tracks were moved from the top to the bottom, which makes the board easier to solder by hand.
- It would have been better to edit the board further so that all tracks leave the ICs on the bottom of the board. This would require extensive rerouting and more vias to be inserted. I also prefer to avoid vias in the tracks for power and ground.

The GU-DIPSOCK footprints have route keepouts on the top that force all tracks to use the bottom pads.

Finally, add your name to both layers of etch (mirrored on the bottom but not on the top) to identify them. Plot the finished board in colour with a scaling factor of 2 for clarity.

☛ **Milestone**: Ask a member of staff to assess your finished design.

Photomasks for double-sided boards

This is for future reference only; you are not required to produce photomasks for the double-sided design in this laboratory.

Separate masks for the top and bottom layers are required for production. Follow the instructions in section 6.7 on page 36 for the bottom and repeat the process with two small changes for the top photomask.

1. Activate and colour the top subclasses instead of the bottom subclasses.
2. Open Plot Setup and choose Mirror under Plot orientation.

The top plot must be mirrored because the printed side of the mask is turned over and placed next to the copper when the photoresist is exposed. A good check is that text should be mirrored on both masks for a double-sided board. (The text on the bottom is also mirrored on your computer's screen but the text on the top is mirrored only on the plot.)

8 A mixed-signal system

The final design is a *mixed-signal* system, which means that it includes both analogue and digital components. This design was one approach to the project for EDP2 in 2007–08, which was an electronic weight scale. Students had to design and build the electronics required between the sensor and a microcontroller. Their PCB was joined by a 16-way cable to a SofTec MC9S08GB60 demonstration board and the display module from Embedded Processors 2. Figure 27 on the following page shows the circuit. These are its principal features.

- An *instrumentation amplifier* (again) amplifies the small signal from the weight sensor. It includes adjustments for the gain and offset voltage.
- The output of the instrumentation amplifier enters an *analogue-to-digital converter* (ADC, part TLC549), which converts the analogue voltage to a digital value.
- The digital value is transferred to a GB60 microcontroller on a Softec board through a *serial peripheral interface* (SPI). Its signals are called MISO, MOSI (not used here), SCLK and $\overline{\text{CS}}$; the last is active low so I called it nSS on the diagram.
- Two pushbuttons *Tare* (set to zero) and *Calibrate* the system. They are connected to general-purpose input/output (GPIO) pins on port E of the microcontroller.
- The PCB takes its power from the SofTec board (pins VCC and ground on J2).

A 4-way Molex connector is required for the weight sensor and a 8×2 header (just two rows of pins) for a ribbon cable to the SofTec board.

8.1 Schematic drawing

The schematic drawing in figure 27 is not complete. You need to make some changes and additions to it. It is not just a copying exercise!

Several new aspects of standard practice are illustrated on the schematic drawing. The most important is the treatment of power pins. These can be connected to the supply rails in three ways, shown in figure 28.

(a) Complete wires are drawn, which rapidly gets clumsy in larger circuits.

(b) Power pins are wired to power symbols, whose names match corresponding symbols on the power rails. These are VCC and VEE here.

(c) Power pins have no wires at all; they are connected purely by name. Power symbols with the same names as the power pins must be connected to the appropriate supply rail. These are V+ and V– here (typical for op-amps). Sometimes the pins and their names are not shown at all.

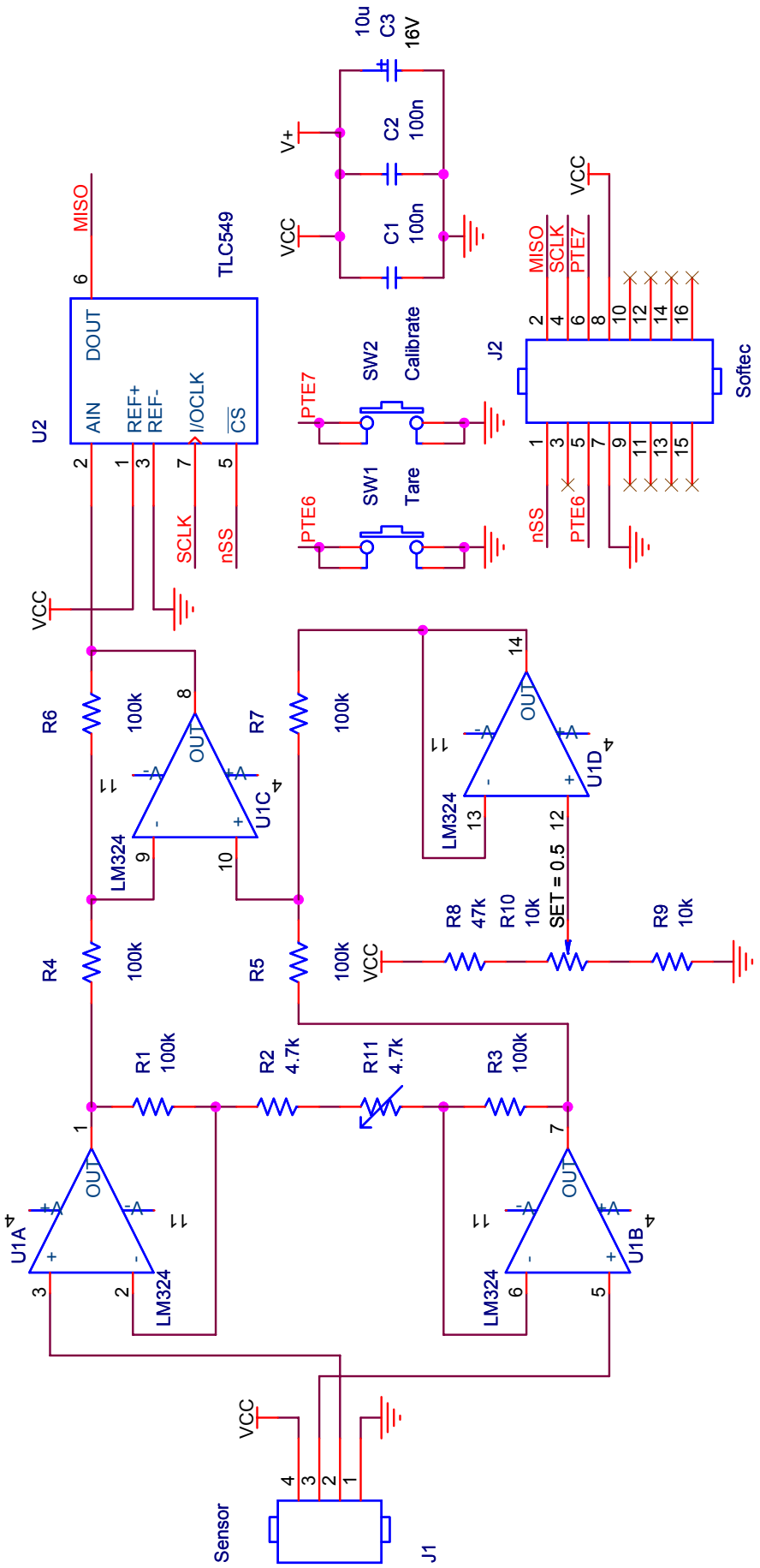


Figure 27. Instrumentation amplifier and analogue-to-digital converter for an electronic weight scale.

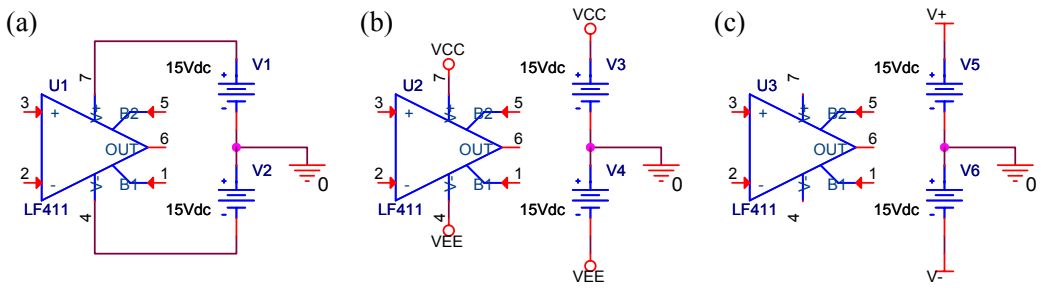


Figure 28. Three ways of connecting power pins to the supply rails.

The shape of power symbols doesn't matter, just their names. Automatic connection by name is a special property of power symbols and pins.
Now draw and complete the circuit yourself following these guidelines.

- The four op-amps are in a single package, LM324, called a *quad* op-amp. This is why they have the letters A–D at the end of their refdes. Capture automatically uses successive op-amps in a multiple package until it runs out and needs a further package. The inputs and output of each op-amp have distinct pins but the power pins are the same for all four.
- *Connect a further power symbol* named V– to ground. Do not do anything to the op-amps themselves. This symbol automatically connects the negative supply of all the op-amps to ground. (The op-amps are used in a *single supply* configuration, where their negative supply pin is connected to ground rather than a negative voltage.)
- The power pins of the ADC are not shown at all (REF+ and REF– are reference voltages rather than power.) Find the names of the pins by opening the Property Editor and making the Pins sheet active. *Add power symbols with these names* to the supplies to provide the correct connections. Do not edit the ADC itself in any way.
- Many other connections are also made by name rather than drawing lines, using a *net alias*. All wires with the same name are connected together.
  1. Draw a short wire on the appropriate pins.
  2. Choose Place > Net Alias... from the menu bar or use the button on the toolbar.
  3. Enter the name for the Alias and click OK.
  4. Click on the wire(s) that you wish to name.
- The variable resistor R11 is a 'virtual component' (you will not find one in stores). *Replace this by a real (variable) component.*
- The pushbuttons are in a local Capture library called EDP2LIB. Download this from the moodle page and copy it to your project folder for this design. Four pins are needed on the symbol, although only two seem necessary, because the physical pushbutton has four pins and the schematic must match this.
- Note the orientation of the 8×2 header carefully. Pin 1 is top left when viewed from the top of the board but the part is mirrored in some libraries.

Follow the same steps as before, summarised in Appendix B on page 48. The components are available so that you can insert the correct footprints.

☛ **Milestone**: Ask a member of staff to check your schematic drawing before proceeding.

8.2 Layout

Here are some tips to help you product a good layout for the PCB.

- Aim to keep the noisy, digital SPI away from the sensitive analogue inputs.
- The four op-amps within the LM324 are identical so you might wish to swap them around to improve the layout – I assigned the four randomly.
- Make the power and ground tracks wider as usual.
- The three capacitors in parallel are for decoupling noise and must be positioned carefully when you lay out the PCB. One of the 100 nF capacitors should be as close as possible to the power pins of the op-amp and the other should be close to those of the ADC. The 10 µF electrolytic capacitor is best placed near the source of power (J2).
- Mark pin 1 of the 8×2 header clearly on the top of the board to show which way the cable should be plugged in. The ribbon cable has a red stripe to identify pin 1.

Most of the design should work as before but you may encounter a puzzling new feature of PCB Editor: the nets for VCC and ground do not appear in the ratsnest. The reason is that separate planes in the PCB are often used for power and ground, in which case there is no point in showing the connections – they are made directly to the planes. PCB Editor therefore hides power nets by default. This isn't useful for our single and double-sided boards so make the nets visible as follows.

1. Choose Edit > Net Properties... to bring up the Constraint Manager, then Net and General Properties.
2. Find column headed No Rat. The entry is probably On in the rows for VCC and GND. Change these entries to (Clear), which should empty the cells.
3. Quit from the Constraint Manager and the nets should appear in the ratsnest. Seek expert advice if they remain invisible.

☛ **Milestone**: Ask a member of staff to assess your finished design.

Congratulations! Read Mitzner's book [1] if you would like to learn more about PCB Editor.

References

[1] Kraig Mitzner, *Complete PCB Design using OrCAD Capture and PCB Editor*, Newnes (Elsevier), 2009, ISBN 9780750689717, about £40. Read this book if you wish to learn more about PCB Designer. Highly recommended. Mitzner covers many features that are not explained in these notes and explains the background theory, which I barely touch. The only disadvantage is that Mitzner concentrates on practice for commercial boards, reasonably enough, but we have to follow a slightly different process for boards made in the university.

[2] Clive Maxfield, *Bebop to the Boolean Boogie: An unconventional guide to electronics*, 3rd edition, Newnes, 2009, ISBN 9781856175074. You might not guess from its title but this includes a wide-ranging description of modern components and construction including PCBs. An entertaining read.

[3] David L Jones, *PCB Design Tutorial*, www.alternatezone.com. This is a good, practical guide to the design and manufacture of PCBs but not specific to OrCAD. The comments on CAD software are a little out of date but it is full of real-world advice.

A How to correct a layout if you spot an error in the circuit

It would be highly irritating if you had to repeat the whole layout after making a change to a circuit. The good news is that it is surprisingly easy to make corrections and that you already know the steps.

1. Save your board in its current state and quit from PCB Editor.
2. Re-open Capture and make the corrections to your circuit. Always run a DRC before proceeding.
3. Repeat the instructions in section 4.5 on page 15 for creating a netlist and sending it to PCB Editor with these small changes.
    - For Input Board File, choose the board that you just saved in PCB Editor – the most recent version of your layout.
    - Use a distinct name for the Output Board File to create a new board.
4. The new board opens in PCB Editor with the minimum number of changes to accommodate the revisions to your circuit. You will have to place any extra components and re-route any tracks that were disturbed.

The jargon for this process is that Capture sends an *Engineering Change Order* (ECO) to PCB Editor.

B Summary: PCB design flow

This checklist is adapted from a handout by Mr I. Young. *Save your work frequently!*

1. Make a new directory for each design. Create an allegro directory within it.
2. Start Capture, create a new project in the new directory and draw the circuit.
   - ❏ Select an Analog or Mixed A/D project if you wish to simulate the circuit. Alternatively, try the PC Board Wizard, which gives you the choice of simulation or not and offers appropriate libraries.
   - ❏ Use libraries in the pspice directory if you wish to simulate your design. If not, you may prefer libraries in the library directory, one level higher. (For example, you could take passive components from library/discrete rather than library/pspice/analog.) These cause fewer warnings from the netlister.
   - ❏ A helpful, local library of symbols is available in Q:/TDP3_ORCAD/Projects.olb.
   - ❏ Use wires to join components, symbols and junctions – don't just push them together.
   - ❏ Provide power connections for all integrated circuits. If power pins are hidden you must place power symbols with matching names on the supply rails.
   - ❏ Include a battery or a connector for a power supply.
   - ❏ Check the circuit carefully before starting the layout: It is much easier to correct mistakes now. If you spot an error in the circuit later, refer to appendix A.
3. Prepare the schematic for PCB Editor.
   - ❏ Get the real components first so that you can match them to footprints.
   - ❏ Edit components with incorrectly numbered pins, such as the electrolytic capacitor in the analog library.
   - ❏ Mark all unconnected pins with the No Connect symbol.
   - ❏ Add the No Connect property NC to packages with pins that are not shown on the symbol in Capture (for example, pin 8 of single op-amps in DIP8 packages).
   - ❏ Add footprints from our local library, prefix GU-. The symbols are in the directory Q/allegro/pcb_lib/symbols. In most cases you should use the DIPSOCK footprints rather than dip for integrated circuits to prevent tracks running to the top pads.
   - ❏ Run a Design Rules Check. Check the Session Log even if no warning dialogue box is shown and correct any errors. Print the final schematic to guide the layout.
4. Create an empty board in PCB Editor using the New Board Wizard.
   - ❏ Set up the search paths if necessary. Add Q:/allegro/pcb_lib/symbols to psmpath and /padstacks to padpath.
   - ❏ Use 25 mil design rules so that your board will be easy to etch and solder.
   - ❏ Make the size of board generous; you can reduce it later.

- ❑ Choose GU-VIA80 for the default via.

5. Netlist the design in Capture. Check all warnings in the the Session Log carefully even if PCB Editor appears to be launched successfully.
6. Place the components on the board in PCB Editor. Pin the Find and Options panels open to control the operation of the tools.
   - ❑ Take time to arrange and orient the components to simplify the ratsnest as far as possible. **This step is critical to get a well-routed board.**
   - ❑ Add mounting holes if required. Do not place them too close to the edge.
   - ❑ Use Setup > Constraints > Physical... to increase the width of tracks for the power supplies and other tracks that carry a heavy current.
   - ❑ Fix the list of vias so that only GU-VIA80 is shown and increase the spacing around vias.
   - ❑ Update the Design Rules Check and correct any errors.
7. Route the board.
   - ❑ Manual routing is best for a simple design (which includes most of ours).
   - ❑ If you must use the autorouter, try a single-sided board first. Use Display > Status... to check that the completion rate is 100%.
   - ❑ If only a few tracks are not routed automatically, complete them by hand and place vias where they are easy to solder. Use wires on top instead of a double-sided board.
   - ❑ If you *must* use a double-sided board, review the results of the autorouter carefully. Move any vias and tracks to pads on the top that cannot be soldered easily.
   - ❑ Gloss the design in PCB Editor or PCB Router.
8. Add text on the etch layer(s) to identify the board and connectors. Mirror text on the bottom.
9. Write photomasks as pdf files at actual size. Follow the instructions carefully and remember to select a filmmask in the Options control panel so that guide holes appear in the pads.
10. Take your board (`.brd`) and pdf files to Mr I. Young in the SPEED group (room 512A). He will check the layout and print the photomasks.
11. Take the photomasks to the electronics workshop (room 712A), where staff will etch and drill your PCB. Finished boards are left in pigeonholes in the electronics stores, just outside the workshop and data library.

Mr Young is always happy to assist students with PCB design. Please ask him if you need a footprint for a component that is not in the library or if you encounter problems that are not solved by this handout.

This handout is available on moodle under General Information > Laboratories, which you can enter as a guest. A further handout describes more advanced techniques in PCB Editor, which you may wish to explore. For example, it explains how to add a copper 'pour' to a PCB as a ground plane and how to create footprints (package symbols).