Electronic Design Project 2
Cadence OrCAD PCB Designer
Notes for demonstrators

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Objectives

After completing these laboratories, you should be able to:

- capture, simulate and lay out a simple, one-transistor amplifier on a one-sided printed circuit board (PCB) with manual routing
- lay out an instrumentation amplifier based on three op-amps, comparing one-sided and double-sided boards with automatic routing
- lay out a mixed-signal system, comparable with the final project in this course, with precautions to prevent interference between the analog and digital sections.

Preamble

You must bring a bound, A4 notebook to every laboratory for recording your results. It needn't be a new book for this course or anything fancy but *you will get no marks if you don't have a book with you*. Please don't use the same book for another course this year. You must also have university (Novell) printer credits so that you can print the circuits, layouts and the results of your simulations. These should be attached firmly into your laboratory book for future reference.

The first part of these laboratories, which is a 'pencil and paper' analysis of a one-transistor amplifier, must be written up in your laboratory book as you do it. The remaining parts do not need much of a record to be kept but you will find it useful to make a note of tricks and tips for using OrCAD. This will be valuable when you have to design your own circuits in Team Design Project 3 next year and in subsequent projects.

These laboratories form part of your professional development because it is expected that every electronic engineer should be able to design, populate and test a printed circuit board (PCB). You are therefore required to complete all tasks to be awarded credit. Most of the marks are awarded simply for completion but extra marks will be awarded for good layouts.

Note for direct entrants: I've tried to make connections with material covered last year, which you may find utterly unhelpful! Please ask me if you are missing any background knowledge.

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1 Introduction

This series of exercises introduces you to schematic capture, simulation and PCB layout using the Cadence OrCAD design suite. This comprises three main applications:

- **Capture** for the schematic capture of circuits, which enables a circuit to be rapidly drawn on the screen. It offers great flexibility compared with a traditional pencil and paper drawing, as design changes can be incorporated and errors corrected quickly and easily. (On the other hand, it is much faster to develop the outline of a circuit using pencil and paper.) A *netlist*, which describes the components and their interconnections, is the link to PSpice and PCB Editor.

- **PSpice** to simulate a captured circuit and confirm that it performs as specified. Plots were produced by a separate application called Probe in the past and I'll stick to this name, although it has long been integrated into PSpice.

- **PCB Editor (Allegro)** for the layout of printed circuit boards. This includes an automatic router (SPECCTRA) that works out the arrangement of tracks needed to connect your components on the PCB. The output is a set of files that can be sent to a manufacturer or the electronics workshop in the Rankine Building.

The first two should be familiar from last year but the third is new. These programs are accessed via networked Windows PCs in the department, with up to 40 users at any one time. Unfortunately the licensing arrangements do not permit access from outwith the Rankine Building. A demonstration version is available; please ask.

We are using PCB Designer for the first time this year because our previous application, Layout, is being discontinued. OrCAD PCB Designer is the most basic version of Cadence's Allegro suite for PCB design and much of the documentation refers to 'Allegro' rather than 'PCB Editor'. Allegro is widely used in industry and is similar to the Cadence software for laying out integrated circuits (ICs), which you will experience in Digital Circuit Design 3. That's the good news: Allegro is far more powerful than we need for laying out our simple circuits and the vast number of features can seem bewildering. It is also new to your instructors and this course will be a learning experience for all of us!

Fixup. I have encountered numerous problems with the software, mainly due to incompatibilities between the libraries supplied for Capture and those for PCB Editor. These are marked as *Fixups*. I expect that we will find smoother ways around these difficulties in the future but you are the guinea-pigs. I'd also be grateful for suggestions for improving these instructions.

There is extensive online help for all these programs although I have to admit that it could be better organised. Please try this before asking a demonstrator for help – it is part of the learning process. Most 'professional' software is so complicated that even experts make regular use of the help files.

Three types of information are needed for each component and are stored in libraries.

- **Electrical symbols** are used to draw the circuit in Capture.
- **Electrical models** allow you to simulate the circuit in PSpice.
- **Footprints** show the size and shapes of the pads (where the pins are soldered to the board) and the outline of the package. They are used to lay out the circuit in PCB Editor.

The first two should again be familiar from last year. Remember that each type of component is kept in a different library file and you must select the files needed for a particular design. The third piece of information is new. You might wonder why yet another library is needed. The reason is that components with the same electrical behaviour come in different packages. For example, an integrated circuit might come in two versions:

- a traditional, plastic dual-in-line package (PDIP) with pins $0.1''$ apart
- a smaller, surface-mount device (SMD) with pins only 0.5 mm apart, if it has pins at all

The opposite is also true: resistors of a particular shape come in a wide range of values. Further information is needed to describe the characteristics of the printed circuit board on which the components are mounted.

Each circuit design is regarded as a *project* and a project manager groups all the files together in a subdirectory. These files should be stored in your work space on the University's central system, accessed via the network as the H drive. Do not store files in any other place on the network or on a computer – they will be erased.

The Cadence system provides many facilities which are not needed for these introductory designs. Please do not attempt to use commands which are not described in these instructions;

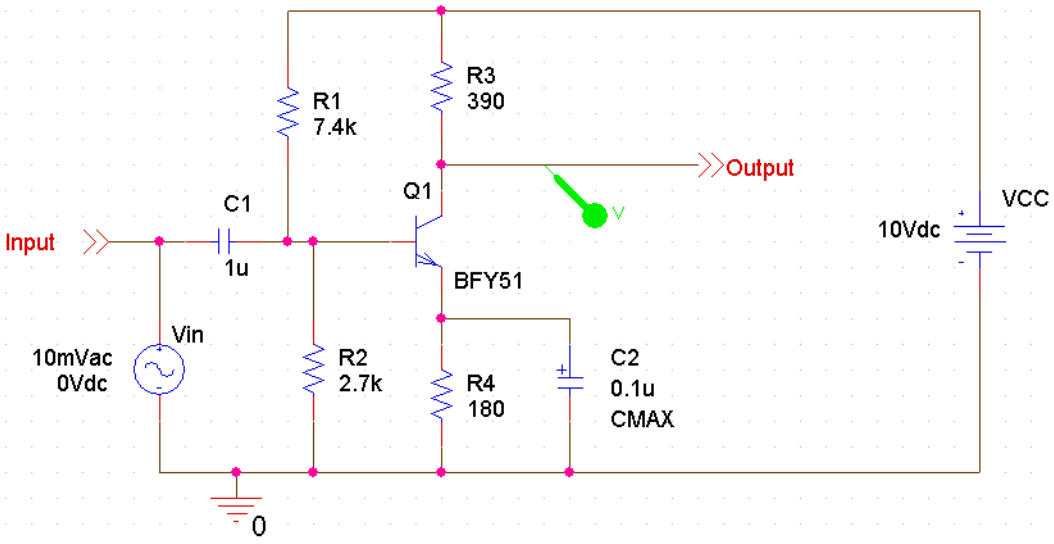

Figure 1. A simple, one-transistor amplifier that can be simulated using Spice.

you will waste a lot of time and may lose large portions of your work. Please ask for help when you encounter problems – you are likely to make matters worse if you try to fix things yourself.

You should know this by now, but a reminder is never a bad idea: **Save your work frequently and take regular backups of important circuits.**

2 One-transistor amplifier: simple analysis

Figure 1 shows the circuit of a simple amplifier with one transistor. It is intended to amplify audio signals, say from 20 Hz – 20 kHz. I have used international standard symbols for the components, such as the zigzag line for a resistor rather than the anonymous rectangle preferred by the IET.

An engineer always makes a rough design using pencil and paper before simulating it. You will not learn how to design this particular circuit until the Analogue Electronics 2 course later in year, so we shall 'reverse engineer' it instead. The calculations are simple and should be done in your laboratory book. You should be pleasantly surprised to find that you don't need to know much about transistors to analyse this. In fact you did most of it in Electronic Engineering 1Y. Make sure that you recognise the emitter, base and collector.

We first find the bias point, operating point or quiescent point. This means the conditions when no signal is applied and the circuit is 'resting'. There is no input and you can therefore ignore the 10 mVac source.

1. Resistors R_1 and R_2 form a simple potential divider if we ignore the other components attached to them. (We should go back and check this assumption when the currents are known.) Calculate the voltage on the base of the transistor Q_1.

   Hint for demonstrators. 2.7 V ❦

2. The base–emitter junction of a transistor is a forward-biassed diode (hence the arrow on its symbol) and therefore has a voltage of $V_{be} \approx 0.7\,\text{V}$ across it. Calculate the voltage on the emitter.

   Hint for demonstrators. 2.0 V ❦

3. We now know the voltage across the resistor R_4. Calculate the current through it.

   Hint for demonstrators. 11.1 mA (the aim was 10 mA) ❦

4. The current into the base of a transistor is much smaller than the other two currents, so the current flowing into the collector is nearly equal to that flowing out of the emitter. Calculate the voltage dropped across R_3 and hence the voltage on the collector.

   Hint for demonstrators. 4.3 V across R_3 so $V_c = 5.7\,\text{V}$ (the aim was 6 V) ❦

This has shown why the four resistors are needed but not the capacitors. What is the expression for the impedance of a capacitor (remember that it is complex), and how does its magnitude depend on frequency? The function of the capacitors in this circuit is to allow high frequencies to pass – the signals that we wish to amplify – but to block the steady voltages that set the bias point.

- We have seen that the base of the transistor is kept at a particular voltage by the potential divider, which sets the bias point. The capacitor C_1 on the input isolates this voltage from the previous stage of the system but lets the signal through.
- Look at the circuit through which the input signal flows. It passes 'through' the capacitor C_1, through the base–emitter junction of the transistor, through R_4 and C_2 in parallel, and back to the ground connection of the input. This shows that R_4 is in series with the input and will reduce its magnitude. We really want all the voltage to be applied across the base–emitter junction, where it will be amplified by the transistor. However, we can't simply get rid of R_4 because it is needed to set the bias point – it determines the current through the transistor, as you saw above. The solution is to put the bypass capacitor C_2 across the resistor.

The bias has zero frequency so it all flows through the resistor. The signal has a 'high' frequency so most of it flows through the capacitor, which should have a much smaller impedance than the resistor. Ideally the impedance of C_2 should obey $|Z_C(f)| \ll R_4$ for all frequencies in the signal. Is this true for the values in figure 1?

Hint for demonstrators. No! At the lowest frequency of 10 Hz, $X_C = 1/2\pi fC = 160\,\text{k}\Omega$, which is much larger than $R_4 = 180\,\Omega$. The capacitor should be a thousand times larger. This will be shown by the simulation. ❦

Finally, we would like to estimate the voltage gain of the circuit. This needs some background on transistors that you have not yet covered so I'll just quote the result. The gain is given by

$$\frac{V_{out}}{V_{in}} = -g_m R_3 \tag{1}$$

where g_m is called the *transconductance* of the transistor, defined by $\partial I_c/\partial V_{be}$. Its value is given by

$$g_m = \frac{I_c}{V_T} \tag{2}$$

where I_c is the collector current at the bias point, which you have calculated already, and V_T is called the *thermal voltage*. This is in turn given by $V_T = k_B T/e$ where k_B is Boltzmann's constant (remember this from physics courses?), T is the absolute temperature and e is the magnitude of the electronic charge. Don't worry about the formula because the value of V_T is close to 25 mV at room temperature, which isn't too hard to remember. Now you can calculate the transconductance and voltage gain. What is the gain in decibels (dB)? – you should remember the definition.

Hint for demonstrators. Transconductance $g_m = 11\,\text{mA}/25\,\text{mV} = 0.44\,\text{S}$, giving a gain of $-0.44 \times 390 = -170$.

The gain in decibels is defined as

$$20\log_{10}\left|\frac{\text{output voltage}}{\text{input voltage}}\right| = 45\,\text{dB}. \tag{3}$$

❦

☛ **Milestone:** Show your results to a member of staff and be prepared to explain them.

An interesting feature is that we haven't used any details of the transistor at all! This makes it easy to design circuits based on bipolar junction transistors, to give them their full name.

Now we'll capture the circuit in OrCAD, simulate it and see how good these estimates are.

3 Schematic capture and simulation

Always create a fresh directory for every new project in OrCAD. You get all manner of strange errors if you do not do this, from which it seems impossible to recover. In any case it helps to keep your work organised.

Select Start > Programs > OrCAD 16.0 > OrCAD Capture (the version number may be higher if OrCAD has been upgraded). I use '>' throughout this document to show the levels of a hierarchical menu. There will be a short delay while the software is loaded and the licence server is accessed. Wait until the red splash screen disappears. The screen will then show the OrCAD Capture main window with a menu bar and a tool bar. A sub-window shows the session log, which may be minimised.

3.1 Create a project

I'll repeat this: Your first action must *always* be to create a new directory to hold all the files for a new project. Next, create an OrCAD project.

1. Select File > New > Project from the menu bar.
2. In the New Project dialog box:

- Select an Analog or Mixed A/D project. This choice is essential or you will not be able to simulate the circuit.
- Give the project a meaningful name.
- Click on the Browse key, select your H drive and navigate to a suitable location. Click the Create Directory button if you haven't already made a new directory for the design and enter a suitable name. Click OK.
- Select this new directory and click OK. The path and directory now show in the location box (if you can see them – they are usually too long). Click on OK in the New Project dialog box.
- Click Next.

3. Select the Create a blank project button in the small dialog box that appears and click OK.

4. Your project will now be created. The Project Manager window (headed name.opj) shows the files associated with your design and the resources that will be used, such as library files. Check that the File tab is selected if the view looks unfamiliar.

5. Open the window SCHEMATIC1: PAGE1 for your design. There is a Title box in the lower right-hand corner. Double-click on the placeholders, which are in angle brackets <>, and replace them with a descriptive title and so on.

3.2 Draw the circuit

Lay out the circuit in figure 1 on page 4. The method is exactly the same as last year, but here are a few tips in case you have forgotten. The names of the components are listed in table 1 on page 12. The capacitor C_2 is an *electrolytic* type, which must be installed with the correct polarity or it will explode. Its parameter CMAX is the maximum working voltage, which is not needed for simulation. I've renamed some of the components to make their functions clearer.

- All circuits must have a ground node called 0 (zero) for simulation. You will get confusing messages about unconnected nodes if you forget this. Get it from the ground button on the right.

- PSpice is unhelpful about notation. Usage like 10^6 doesn't work but it won't tell you! (It will just stop at the caret and take the value as 10.) Use 1e6 or 1Meg instead – not 1M because a single m or M means milli, not mega.

- Libraries must be chosen from the pspice folder, otherwise the components will not have PSpice models and you will not be able to simulate them.

- Simple components like resistors are in the analog library, sources such as VDC are in source and the param block is in special. Use Search if you can't guess where a component is located. You will probably need to do this for the transistor.

- Always join components with wires, not by placing them so close that their pins overlap. This can cause strange errors.

- Wires and components sometimes become joined incorrectly if you move them about. Use Place > Junction or the junction tool from the buttons on the right to eliminate spurious connections.
- Place voltage probes on the points on the circuit where you want to plot the values. This is easier than selecting them from the list of variables in Probe.
- I like to use off-page connectors to label nodes such as input and output, where the voltages will be plotted. There is a menu and button for these. The names appear in Probe, which makes it much easier to identify the traces.

3.3 Simulate the circuit

Set up a Simulation Profile to make an AC Sweep of the circuit from 10 Hz to 100 kHz. Remember that the sweep should be logarithmic in decades, not linear. About 10 points per decade should be adequate. Run the simulation and plot the results. Plot the voltage gain in decibels (dB) rather than the output voltage itself. You should remember how to do this from the *RC* filter last year but here is a reminder.

1. Delete all the traces in the plot window.
2. Choose Trace > Add Trace from the menu bar. The dialog box shows variables on the left and functions on the right.
3. Choose the DB function from the right, and inset the output voltage divided by the input voltage using the variables from the left. The final expression should look like DB(V(Output)/V(Input)) if you used the same names as me.

Hint for demonstrators. If the PSpice menu and toolbar are missing, the student has probably forgotten to choose 'Analog or Mixed A/D' when the project was created. Copy and paste the circuit into a new project with the correct type.

Many students will have forgotten what is meant by voltage gain: output voltage divided by input voltage. I have explained how to use the decibel function in probe but there are more advanced approaches to request this type of plot directly from the menus in Capture, using PSpice > Markers > Plot Window Templates... and choosing Bode Plot - dB or Voltage Gain. The input must be 1 Vac for this.

My results are in figure 2. The gain never reaches its target value. The wide plateau around 1 kHz is where the gain is limited by R_4 because the bypass capacitor is too small. ❦

- Does the gain match the estimated value? Is it reasonably constant with frequency across the audio range?
- You should also check that the bias point agrees with the pencil-and-paper calculations. Go back to Capture and click the V button to get the voltages on all nodes. Check the current through the transistor too.

I found that the gain did not behave as expected (so now I have given you the answer to the first question!) and suspect that the capacitor C_2 across the emitter resistor R_4 is too small. Check

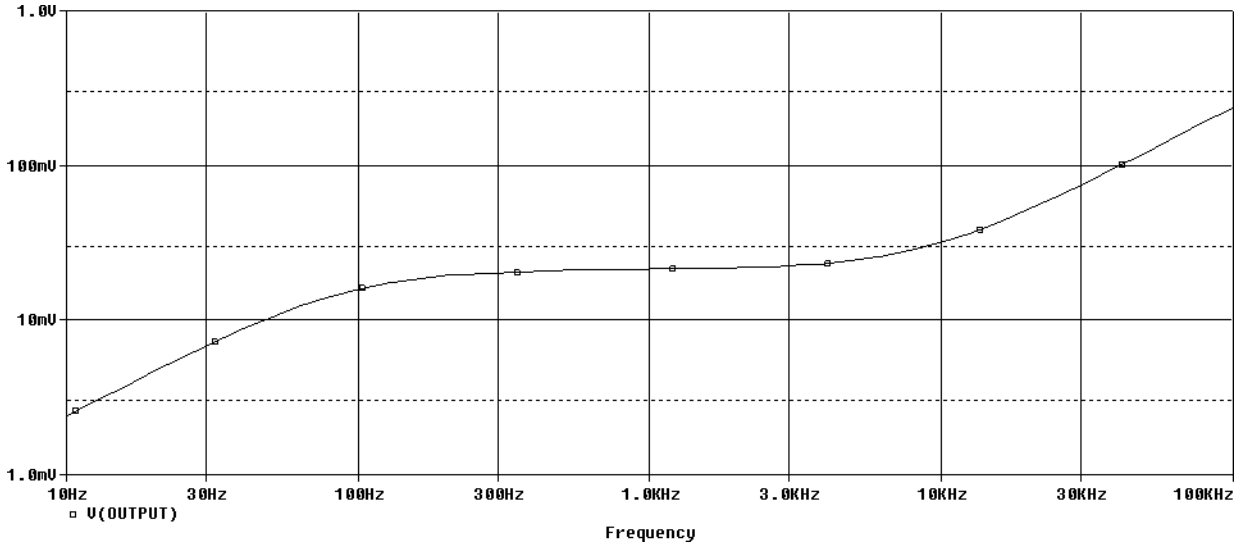

Figure 2. Gain as a function of frequency.

this by simulating the circuit for a set of values of C_2. This requires a *parameter*. You should remember how to do this from Electronic Engineering 1X and 1Y but it is clumsy so here is a reminder.

1. First place a param block from the special library.
2. Open its spreadsheet by double clicking or with the Edit Properties... contextual menu item.
3. Choose Add row... (or column, depending on the orientation of your spreadsheet) to create the parameter. Give it a name, such as Cap2, and a default value (use its previous, fixed value). Click OK to get rid of the dialog box.
4. The parameter does not appear on the schematic by default so you must select the newly added row/column in the spreadsheet, click the Display button, select Name and Value and finally click OK.
5. Change the value of C_2 from a fixed value to the parameter. Remember that the parameter must be enclosed in curly brackets {} in the Value field.
6. Create a new simulation profile with the same frequency sweep plus a parametric sweep on Cap2 from 0.1 µF – 1000 µF. Use a logarithmic sweep with one value per decade. Run the simulation and print your results in colour. The printout looks better if you make the lines thicker. (If you print in black and white, set the number of trace colours to zero so that the curves show up.)

Does a larger value of C_2 improve the performance? What value would you recommend?

☛ **Milestone:** Show your results to a member of staff and be prepared to explain them.

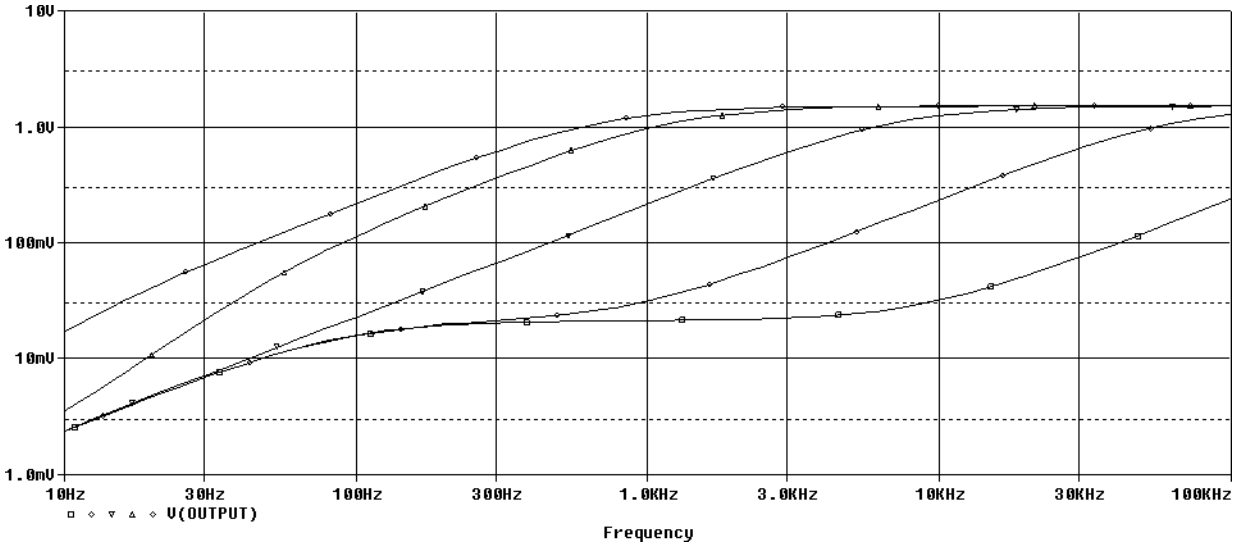

Figure 3. Gain as a function of frequency for different bypass capacitors.

Hint for demonstrators. My results are in figure 3. Increasing the bypass capacitor improves the gain until it is limited at low frequency by C_1 instead. There isn't much difference between the results for 100 µF and 1000 µF so I would use 100 µF. ❦

4 Preparation for PCB layout

Once the design of the circuit has been finalised, it should be laid out on the printed circuit board (PCB). This takes a few steps before you leave Capture. The overall *design flow* for making a PCB is shown in figure 4 on the next page and there is a summary in section 9.

4.1 Edit the circuit

First, the 'virtual components' in the schematic must be replaced by real components. Here this means the voltage sources and param block. There is no way that you can build a real circuit with a param block for instance! (Well, you could use a pair of sockets and unplug the component to change it.) The real circuit has connectors for input, output and power, which must be placed instead. This is shown in figure 5. The types of connector are HEADER 2 and the like. They are in the connector library, which is in the directory one level above pspice. The connectors are oriented so that pin 1 is connected to ground in both cases. It is shown by a square marker on the PCB. I have changed the names to make them more descriptive than the defaults, such as HEADER 2; do not edit the references J1 and J2. Add text to label the pins of each connector and put your name on the circuit, or you won't be able to identify it when it comes out of the printer.

Hint for demonstrators. Some students change the Reference (J1 or J2) of the connectors to Input or Output instead of changing the Value (HEADER 2 or HEADER 3). This causes trouble with the netlister later on. ❦

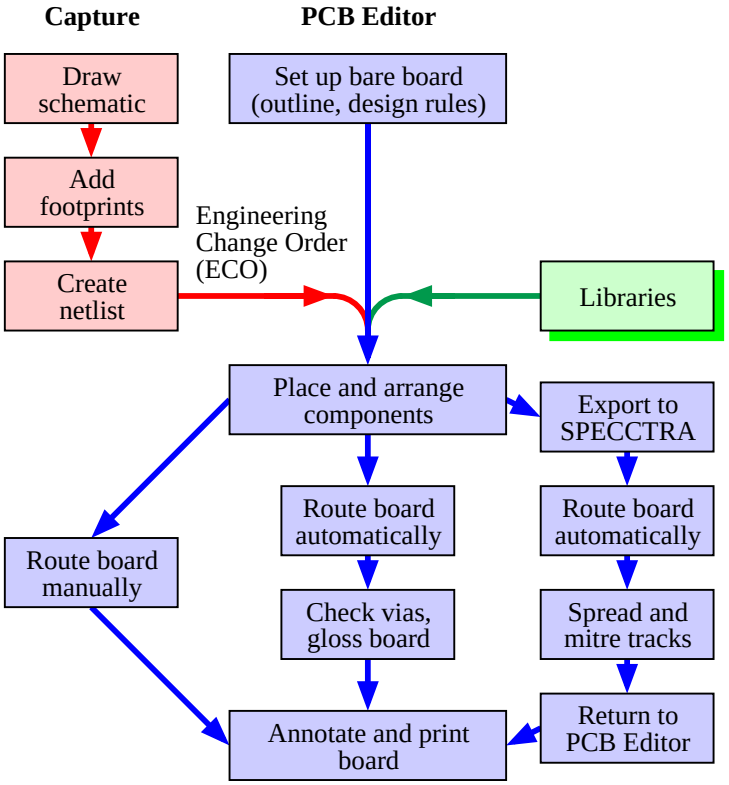

Figure 4. Design flow for making a PCB with Capture and PCB Editor. The three paths for PCB Editor depend on whether the tracks are drawn manually (as we shall do for our first design), automatically within PCB Editor, or by running the automatic router (SPECCTRA) as a separate application.

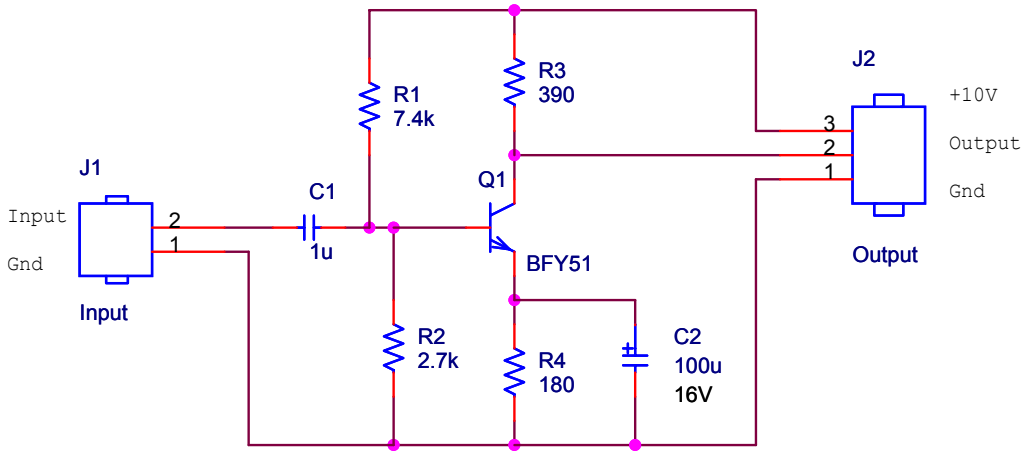

Figure 5. The simple, one-transistor amplifier with only real components, ready for layout.

Table 1. Footprints of components for the one transistor amplifier.

Part	Name	Footprint
Resistor	R	RC400
Capacitor	C	RC500
C, polarised	C_elect	RC200_RADIAL
Connector	HEADER 2	MOLEX2
Connector	HEADER 3	MOLEX3
Transistor	BFY51	TO5 (letter 'oh' not number zero)

Fixup. There is a stupid incompatibility between the electrolytic capacitor C_elect in the analog library and the footprints. The pins of the footprints are numbered 1, 2 but those of the capacitor are p, n. This means that the software cannot match the capacitor to its footprint. Edit the electrolytic capacitor and change the numbers of its pins to resolve this. You will need to edit parts in future so it is useful to learn the procedure.

1. Select the electrolytic capacitor and choose Edit > Part from the menu bar. A window will open with an enlarged view of the capacitor.
2. The negative pin is shown as a red line on the right. Select it and and choose Edit > Properties.... This brings up the Pin Properties dialogue box.
3. Change the Number to 2 and click OK. Don't worry about the name.
4. The positive pin is shown as a circle. Select this and edit its Number to 1.
5. Choose File > Close (or click the close box as usual). You have the choice of updating this part alone, or all 'part instances' – that means all C_elect components in your design. Of course there is only one so it doesn't matter whether you choose Update Current or Update All in this case.

Print the drawing sheet and stick it into your laboratory book. The circuit takes up only a small part of the page, so it is a good idea to choose File > Print Area > Set and mark out a rectangle that includes only the part of the page that you wish to print.

☛ **Milestone:** Have your drawing checked before you go any further.

4.2 Add footprints

We must next associate *footprints* with the components so that the PCB can be laid out. These are the physical outlines of the components including the positions of the pins. The pspice library contains footprints already but unfortunately they are mostly wrong. We must therefore enter the correct footprints now. The footprints for this circuit are listed in table 1. Please type carefully and don't muddle the letter O with the numeral 0.

1. Drag the cursor in Capture so that all the components are enclosed in a rectangle. Do not include the title box.

2. Choose Edit > Properties... from the menu bar, which brings up the Properties spreadsheet.

3. Type each name into the PCB Footprint field of the Properties spreadsheet in Capture. All the resistors have same footprint so use copy and paste for speed.

A problem with footprints...

PCB Editor comes with a small library of footprints but they are intended for commercial production and are unsuitable for boards made in this department. Many components are missing too. Mr I. Young of the SPEED group in this department has therefore designed a more suitable set of footprints. There is a catalogue at the end of this handout, which you should be able to match with the components kept in stores.

4.3 Design rules check

The next step is a Design Rules Check, to ensure that there are no errors.

1. Click on the Project Manager window and highlight your design (with extension .dsn).

2. Select Tools > Design Rules Check... from the menu bar.

3. Choose options (probably the default):

   - report identical part references
   - check unconnected nets

4. Click OK, and look at the report in the Session log window. There is no positive message that all rules have been passed successfully, just an absence of complaints. The final line is usually Check bus width mismatch; I don't know why it starts with Check, which is misleading, rather than Checking like the others.

5. Return to your drawing and correct any errors. These may be shown by green circles (a strange choice of colour for an error!). Repeat the Design Rules Check until it runs silently.

6. You may wish to run the Design Rules Check and select Action > Delete existing DRC markers to get rid of the green circles. They do not vanish by themselves.

4.4 Make a bare board in PCB Editor

The simplest way of creating a PCB is first to set up an empty PCB, then to add your components and connections to the board. This follows the design flow shown in figure 4 on page 11.

First create a directory allegro within your directory for the current project. PCB Editor likes to keep its files in a directory with this name. Then choose Start > Programs > OrCAD 16.0 > OrCAD PCB Editor, which opens the OrCAD PCB Designer application (Cadence seem muddled about the name). I'll leave the details of the interface until later because we need only two dialogue boxes for this step.

Set up the search paths for footprints

I mentioned above that we use a local library for footprints rather than those supplied with Allegro. We must therefore tell PCB Editor to look in the local library first. You should only have to do this once (and maybe not at all, depending on how the software and PCs are configured).

1. Choose Setup > User Preferences... from the menu bar, which brings up the User Preferences Editor.

2. Choose Design_paths in the list of Categories.

3. We first need to change psmpath, which is where PCB Editor looks for library symbols. Click on the Value button (which shows only '...'). This brings up a box entitled psmpath Items.

4. Click the New (Insert) button (the leftmost one), which adds an empty item to the list with another '...' button. Click this button, which brings up the usual Windows Select Directory box.

5. Navigate to the Elecapps drive (Q), find the allegro directory, then pcb_lib and finally symbols. Click OK to select this directory.

6. Next we must tell PCB Editor to look in our local directory before the default libraries, denoted by $psmpath. Click on $psmpath followed by the Move Down arrow. The psmpath Items box should now look like figure 6 on the next page except that your directories are different (my computer is not on the same network). Click OK.

7. Follow the same procedure for padpath, which uses the padstacks directory in pcb_lib. This is the information for the *padstacks*, the copper islands used for mounting components, including holes for pin-through-hole components.

8. Click OK to dismiss the User Preferences Editor.

You should never have to do this again!

Define the board

Choose File > New... from the menu. In the first dialogue box, set the Drawing Type to Board (wizard). Click Browse..., navigate to your new allegro directory and give the board a name such as bare.brd. Click Open then OK to bring up the new board wizard. This takes you through several screens to define the parameters of the PCB. Some of these are obvious, such as the size of the board, while others set up the *design rules* – the width of tracks on the PCB, how much space must be left between them, and so on.

1. The first screen is purely descriptive. Read it, then click Next >.

2. This asks for a board template. We don't have one so select No (probably the default) and click Next >.

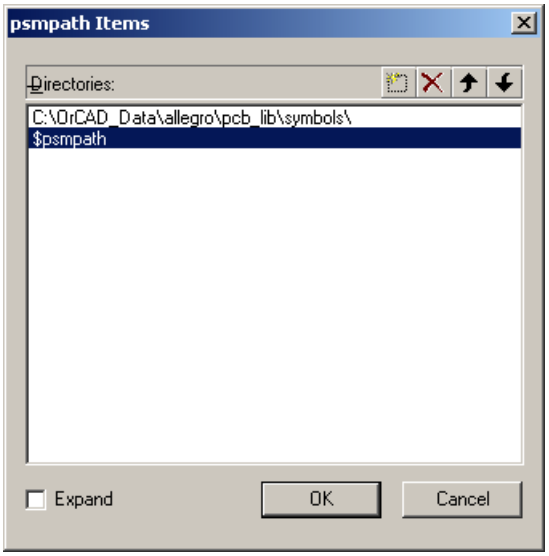

Figure 6. Completed dialogue box for setting up psmpath. Your directory path will be different.

3. You are next asked for a 'tech' file. This is short for a *technology* file, which specifies the design rules – number of layers, widths and separation of tracks and so on. We won't use one for this design so select No and click Next >.

4. This asks for a board symbol. We don't have one so select No again and click Next >.

5. We now reach the screens for the parameters that must be set up. The units should be Mils. These are not millimeters but the American term for thousandths of an inch; 1 mm $\approx$ 40 mils. All dimensions are given in these units so get used to them.

   Leave the drawing size at A. This is an American size but you aren't allowed European A4 if the units are mils. Leave the origin at the centre.

6. Set the grid spacing to be 25 mils.

   The Etch layer count is the number of copper layers on the board – the number of layers of tracks for signals and power. Leave this at 2, although we shall use only one layer in the first design.

   Don't worry about the artwork films – we don't use them.

7. Leave the names of the layers as Top and Bottom and their types as Routing Layer.

8. Enter 30 for the Minimum Line width (in mils). This value will propagate into the other boxes. It means 0.03″ or about 0.76 mm, which is very wide for a track nowadays but makes the board easy to lay out.

   For the Default via padstack, click on the button with ... and choose Via80. This first design is far too simple to need vias, which carry a signal from one layer of the PCB to another, but they may be required later.

9. Rectangular board (it's curious that a circular board is the default).

10. Enter a width of 3000 and height of 2000 mils. This defines the board outline as $3'' \times 2''$. There is no corner cutoff.

    Specify the Route keepin distance as 100. A *keepin* means that objects must be kept inside the specified region. In this case it means that tracks cannot go any closer than 100 mils to the edge of the board. It gives a border around the PCB to aid handling and manufacture. (We'll encounter keepouts as well later.)

    Set the Package keepin distance to 250. Components must be placed within this keepin and therefore cannot be closer than 250 mils to the edge of the board. The gap between the two keepins allows you to run tracks around the outside of all the components, which is often helpful on a more complicated board.

11. Click Finish – that's it.

This has set up the design rules and made an empty board which you can see in the main window of PCB Editor, shown in figure 8 on page 19. There are three rectangles for the board outline, route keepin and package keepin. Choose File > Save and close PCB Editor.

Hint for demonstrators. If students can't find Via80, it means that PCB Editor can't find our local library. Check that the paths have been set up correctly.

The next step is to return to Capture and send the circuit to PCB Editor so that it can be added to the bare board.

4.5 Create a netlist

The information about your design is sent from Capture to PCB Editor in the form of a *netlist*, which contains a description of the circuit and its components. (There are actually three files but you don't need to look at them.)

1. Highlight your design in the Project Manager window of Capture.
2. Select Tools > Create Netlist... from the menu bar, which brings up a dialogue box as in figure 7 on the next page. Make sure that the PCB Editor tab is active.
3. Check that the PCB Footprint box contains PCB Footprint.
4. Check that the box underneath for Create PCB Editor Netlist is selected.
5. Under Options, the Netlist Files Directory should be shown as allegro. Select Create or Update PCB Editor Board (Netrev).
6. For Input Board File, choose the bare board that you have just set up. Click on the '...' button to navigate.
7. The Output Board File should show something sensible automatically; edit it if not. It should use the new allegro directory.
8. Under Board Launching Option, select Open Board in OrCAD PCB Editor. This is required because our licence doesn't cover the full version of Allegro.

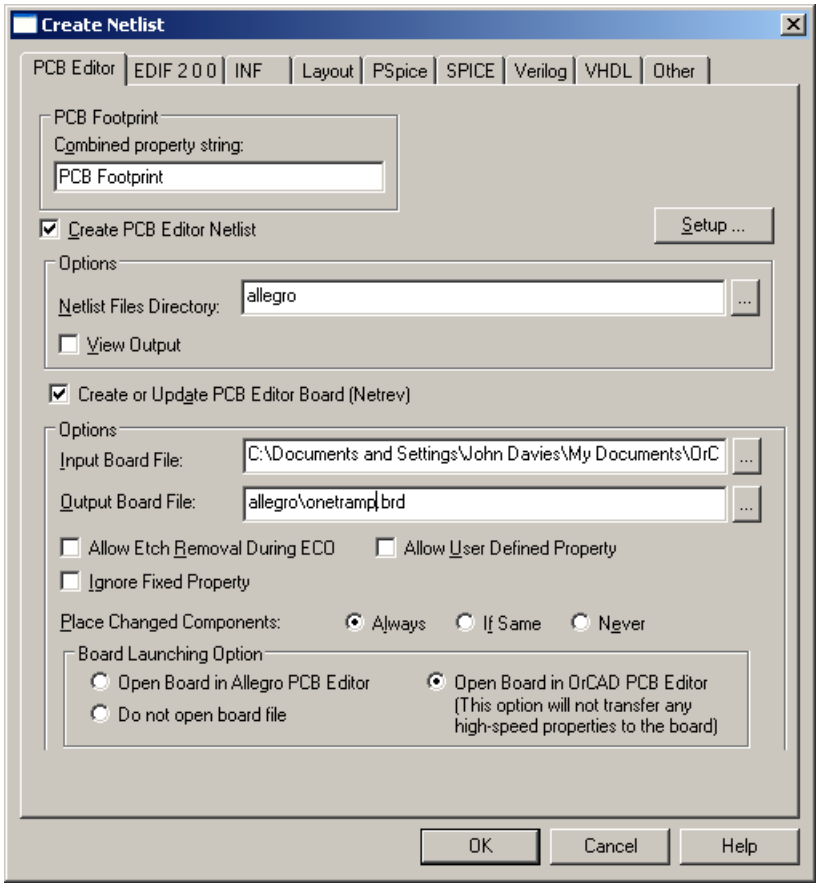

Figure 7. Completed dialogue box for netlisting the design and sending it to PCB Editor. Your file names will be different.

9. The entries in the dialogue box should now resemble figure 7 except that your pathnames are different. Click OK to dismiss this dialog box and start the netlister.

You will be warned that your design will be saved by Capture, then a Progress box will appear to show the various processes needed: Netlisting the design followed by Updating OrCAD PCB Editor Board. PCB Editor will then be launched with your new board.

- You will probably see a Warning box, which tells you that Netrev succeeded with warnings. Check the Session Log if this happens. Messages about RVMAX and CMAX can be ignored; these are maximum voltage ratings of the components and are not important for this circuit. Pay attention to any others and seek advice.
- OrCAD PCB Editor will also give you a warning that Database was last saved by a higher tier tool, which you can ignore.
- Consult a demonstrator if you get an error and the process fails.

You should now see your empty board outline on the screen of PCB Editor again; the components are invisible at this stage. Close Capture and allow it to save all the files.

Hint for demonstrators. If PCB Editor complains that no product licences are available, the student has probably forgotten to select Open Board in OrCAD PCB Editor. A different message appears if we run out of licences, which I hope will not happen.

If the Netlist Files Directory does not show as allegro automatically, and nothing appears to happen when you run the netlister, there is a problem with the permissions. Netlisting must be performed once on each computer by a user with administrator privileges before it will work for anybody else. Don't ask me why…

PCB Editor is almost always launched even if there was a fatal error during netlisting, which misleads students into thinking that the process was successful. It is vital to check the session log.

5 OrCAD PCB Editor

OrCAD PCB Editor is the basic version of the Allegro PCB Editor from Cadence. Despite being 'basic' it is vastly more powerful than is needed for the simple designs that we shall lay out in this course. Its interface will probably feel unfamiliar because the application was originally developed for unix and has been ported to Windows with minimal changes. Some distinctive features will become obvious almost immediately.

- The main window, which shows your design, has no scroll bars.
- There is always one design open; you cannot open more than one, nor close the current design without opening a new one or exiting the application.
- There is no 'null' tool, such as the pointer shown by most drawing applications when no other tool is selected. If you are not sure which tool is active, right-click in a region of empty space and choose Done from the contextual menu to deselect the current tool.

5.1 The screen

PCB Editor needs a big screen – the elderly laptop that I have used while writing these instructions is not large enough to show all the toolbars! These are the main elements of the application, shown in figure 8 on the next page.

- **Menu bar** along the top as usual.
- **Toolbars** in two rows under the menu bar and a further column down the left-hand side. Their arrangement depends on the size of the screen. Hover the pointer over a button to reveal its function.
- **Control panels** on the right-hand side with tabs for Visibility, Options and Find. Each panel pops out when you move the pointer over its tab. This can be irritating and there is a pin to lock each panel open.
- **Command console window** at the bottom left of the screen. This prints a running log of your actions and is useful to show when Allegro is waiting for input from you. It also displays the output from commands such as Design Rules Check.

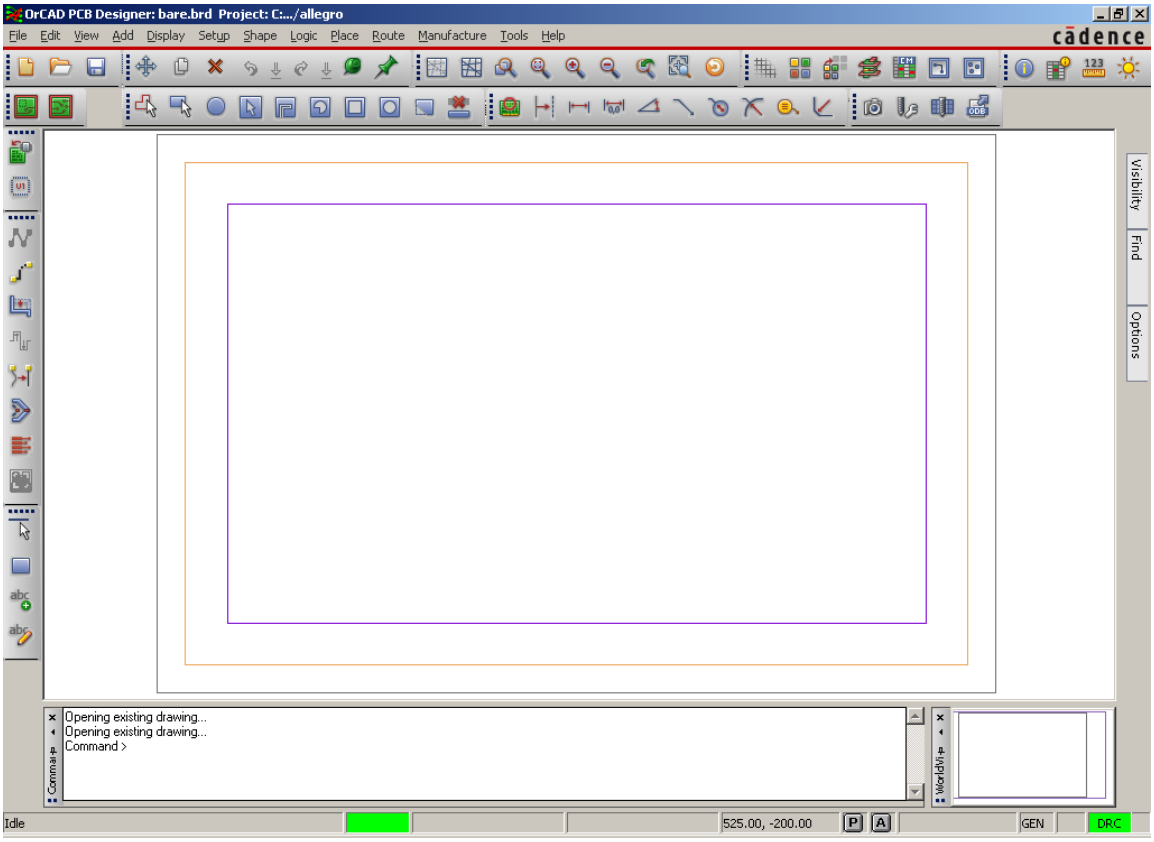

Figure 8. Screenshot of OrCAD PCB Editor with an empty board. The rectangles show the board outline (outer), route keepin and package keepin (inner). I have changed the background of the windows to white for a clearer printout.

- **Worldview window** shows how the relation between the board outline and the view in the main design window. It is useful for moving the design window around the board as we shall soon see.
- **Status bar** at the bottom of the screen. It shows the coordinates of the pointer (crosshairs) and the P button is useful for typing coordinates instead of clicking with the mouse if your hand is unsteady.

  At the right is a coloured block called DRC, which stands for Design Rules Check (as you remember from Capture, of course). It is currently yellow because the design has not been checked. Usually it should be green to show that automatic checking is turned on.

There is a lot of jargon associated with Allegro. It often refers to your design as the *database*, because that's what it is from the point of view of the computer. The various elements of the design are classified into *classes* and *subclasses*. Here are some common elements.

- The **Etch** class includes the regions of copper that act as pads for the components and the tracks that carry the signals between them. Our designs have two subclasses of etch, **Top** and **Bottom**. They are coloured green and yellow respectively.

- The **Board Geometry** class includes the **Outline**, which we have already seen. There are also **Silkscreen_Bottom** and **Silkscreen_Top**, which are used for text to annotate the board.

- We have also seen the **Package Keepin** class, used to prevent components being placed too close to the edge of the board.

The active class and subclass can be chosen in the Options control panel but PCB Editor usually selects the appropriate classes automatically when you make a tool active.

The screen always shows the board viewed from the top. The bottom layer is seen through the board as if it were transparent.

5.2 Moving around the design

There are two ways to *pan* or *roam* the design – move it horizontally or vertically so that you can see the region of interest.

- Use the arrow keys on the keyboard.

- Hold down the middle button of the mouse and drag. A confusing feature of this is that *it drags the window over the design*. This means that the design moves in the *opposite* direction to your drag. It is the reverse of the hand 'grabber' in applications such as Acrobat, which drag the design under the window.

  But I have only a two-button mouse! Many two-button mice have scroll wheels, which act as the middle button when pressed. If yours really has only two buttons, hold down the shift key while pressing the right button.

You will also need to *zoom* into the design to concentrate on small details or out to review the complete layout. Again there are two methods.

- Use the commands under the View menu. There are corresponding buttons and shortcuts. Zoom Fit fills the window with your complete design and is useful if you lose sight of it.

- The scroll wheel of the mouse zooms in and out, centred on the current position of the pointer.

The WorldView window can also be used to zoom and pan. If you drag a rectangle here, that becomes the area shown in the main window.

There's a lot more to say about the interface but it would be better to place the components and populate the PCB next.

5.3 Place the components

Choose Place > Manually... from the menu bar to start placing the components. This brings up the Placement dialogue box shown in figure 9 on the following page. The Placement List tab should be active and the list should show Components by refdes with the components in your design listed below.

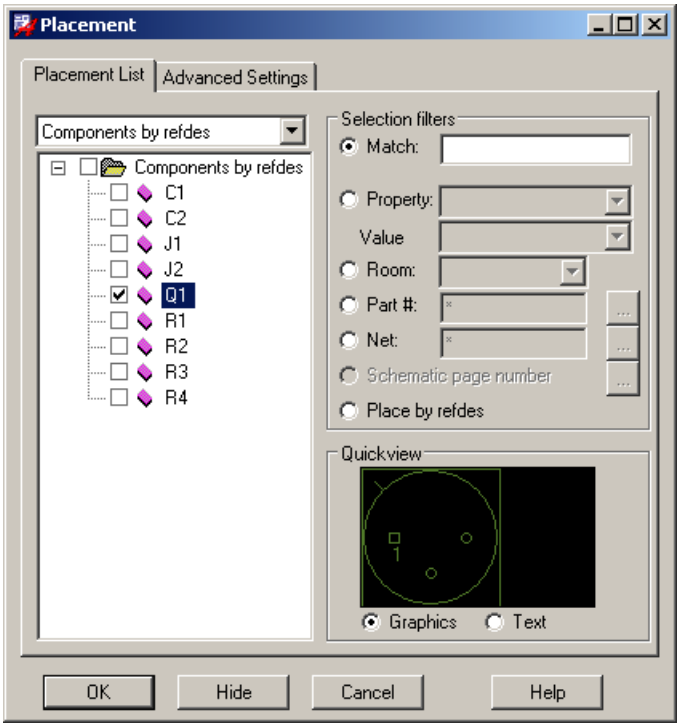

Figure 9. The Placement dialogue box, showing the components for the one-transistor amplifier. Transistor Q1 is ready to be placed on the board.

Jargon: *refdes* is an abbreviation for *reference designator*, the label for each component on the schematic drawing. For example, the transistor probably has refdes Q1.

Allegro can place components automatically but it is straightforward to place them manually for this simple design. See figure 11 on page 24 for guidance on the desired layout.

1. Start by placing the transistor. Click the box next to Q1, which shows its outline in the Quickview box.

2. Move the cursor out of the Placement box on to your design. The outline of the transistor is attached to the cursor. Left-click to place it centrally on your board. The outline will be filled in and a small P for 'placed' appears in the Placement box next to the refdes. If you hover the cursor over the outline of the transistor a popup message Component Instance "Q1" is shown.

3. We'll place the connectors for input and output next. Select the boxes for both J1 and J2. Move the mouse onto the design and a two-pin header for J1 appears on the cursor. Click somewhere near the left-hand side to place it. Don't worry about its orientation for now.

4. The outline of J2 now appears automatically; place this on the right-hand side.

5. Next place the four resistors. Put them in the same positions relative to the transistor that they have on your schematic drawing. This will make the circuit easier to wire! Refer to your printout to identify each resistor.

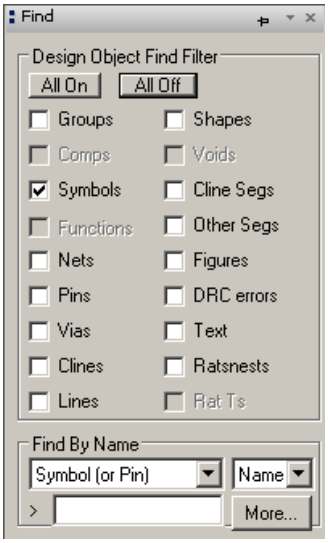

Figure 10. The Find control panel set up so that only symbols can be selected.

Keep all components inside the inner purple rectangle, which shows the Package Keepin. It will turn green if you try to place any part of a component outside it.

6. Place the two capacitors in the same way. This completes the placement so dismiss the dialogue box.

The components are joined by a set of cyan lines to show their logical connections. This is called the *ratsnest*. These 'virtual' lines are turned into copper tracks when you *route* the board. The lines of the ratsnest simply take the shortest path between components and therefore cross other lines. Real tracks cannot do this. It is therefore vital to adjust the orientation and position of the placed components to improve the layout, reduce the number of crossings in the ratsnest and make routing easier.

Hint for demonstrators. If no outline appears when a component is selected in the Placement dialogue box, the search path for symbols or padstacks is probably wrong.

If components are missing, there was probably an error during netlisting. Go back and check the session log in Capture.

Before doing this, experiment by moving the mouse over the design without clicking. You will see different elements of each component highlight as the mouse passes over – outline, pins, text, lines of the ratsnest. How can we be sure to move a complete component, not just a part of it? (Moving a pin by itself would be a seriously bad idea, for instance.)

This is where the Find control panel is useful. Bring the panel up by moving the mouse over its tab, click the All Off button, then select Symbols as in figure 10. Move the mouse away so that the panel closes itself. You will now find that only symbols for components are highlighted when you move the mouse around the design. The ratsnest will not be selected, for instance. This makes it much easier to move and rotate components.

- Select a component, right-click and choose Move.

- To rotate a selected component, right-click, choose Spin and move the mouse around to get the desired orientation.
- Both of these actions can also be chosen from the Edit menu and there is a Move button too.
- Do *not* use the Mirror command, which is different from the commands in Capture: Here is means that the component should be placed on the bottom of the PCB rather than the top. Our designs are not that ambitious.

Move and rotate the components to give as few crossings in the ratsnest as possible. Copper tracks must not cross each other! This design is easy because there are no crossings at all if you follow the schematic drawing, which makes routing trivial.

Hint for demonstrators. If some components have red outlines rather than the usual colour, and their refdes is in mirrored text, they have been mirrored and placed on the bottom of the board instead of the top. Select them and mirror them back to the top.

When you have placed and arranged all the components, update the design rules check by choosing Tools > Update DRC from the menu bar. The DRC block near the bottom right of the window turns green and the Command window shows No DRC errors detected if everything is correct. If you have placed a component outside the keepin, for example, the message would be DRC done; 1 errors detected. The error is shown by a tiny red 'butterfly' marker on the design. Move the component inside the keepin and the marker disappears.

Note. There are errors with some footprints at present because we have only recently converted the library to Allegro and it needs more work to clean it up. Ignore these.

Save your design. Unusually, Allegro asks you if you wish to overwrite the existing file. You may wish to save successive versions under different names in case you need to go back and repeat a step. Allegro does not save backups automatically.

5.4 Route the board

The electrical connections depicted by the ratsnest must now be converted to copper tracks on the PCB. The layers of copper are called *etch* in Allegro because of the usual manufacturing process. The tracks will be drawn on the bottom of the board, with the components on the top (where they go by default). The wires from the components pass through the holes in the pads and are soldered to the tracks on the bottom of the board.

Jargon: *cline* is short for *connecting line*, a segment of a copper track. A plain line may show the edge of the board or the outline of a component and is not a conductor.

Keep the layout of tracks as straightforward as possible. It is a good idea to imagine soldering the board yourself! Do not make your life difficult by running tracks close to pads, for instance. You should aim for something like the layout shown in figure 11 on the next page but there is no need to follow this precisely.

1. Pin the Options control panel open, which makes it easier to see what is going to happen.

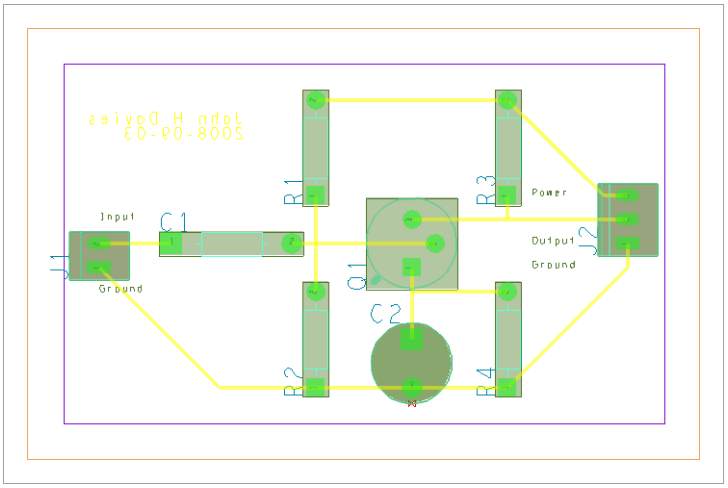

Figure 11. Screenshot of the routed board for the simple, one-transistor amplifier. The tracks are yellow, which shows that they are on the bottom of the board. Your screen may not match this image exactly because it depends on which classes are active at the time.

2. Choose Route > Connect from the menu.

3. The Options control panel changes to reflect the current activity and it now shows the layers available for routing. We want all the tracks to go on the bottom of the board so change the Act (active) layer to Bottom, which will be painted yellow. You can also change the Alt (alternative) layer to Top, which is painted green, but we will need only one layer for this simple circuit. You will see that Line lock is set to 45 (degrees), which determines the allowed change in direction of a track.

   Take a look at the Find control panel too. This automatically changes so that you can select the relevant objects for routing.

4. Left-click on a pin to start routing a segment – the region of a track that runs from one pin to another. A segment of the ratsnest highlights to show that it is available for routing.

5. Move the mouse towards the pin at the other end of the highlighted ratsnest. A thick yellow line is drawn to show the copper track.

6. Click at intermediate points to fix corners. These will automatically turn through 45°, which is good practice. It is a bad idea to draw 90° corners because they are prone to breakage during etching.

7. Click on the destination pin to complete the track.

8. Repeat to route all segments of the ratsnest. Select a pin, right-click, choose Add Connect and draw the track.

Run a design rules check to detect any problems with routing and save your board.

Hint for demonstrators. Some students put the tracks on the top instead of the bottom, in which case they appear green on the screen. Set the Find control panel for Nets, draw a rectangle around the board to select all the nets, right-click and change their layer to Bottom.

Another error is to draw tracks that don't match the ratsnest. Some students lay out the components incorrectly but draw the tracks to match figure 11. This causes a profusion of DRC errors.

A few students manage to draw tracks that bear no relation to the ratsnest at all and aren't even connected to pins. The underlying problem is usually that Pins are not active in the Find control panel.

Oops! – I made a mistake

There are several ways of undoing an error.

- Right-click the mouse and choose Oops. This undoes the most recent partial action, such as the last segment of a track.
- Choose Cancel, which undoes the last complete action.
- If you have made a complete mess, go to the menu File > Recent Designs and reload your design (there is no Revert to Saved command). This abandons all changes since you last saved the file, which I hope was not too long ago. . . .

My tracks don't look very good: How can I improve them?

There are many ways of adjusting the tracks. First make sure that you are not still using the Connect tool by right-clicking and choosing Done if this appears on the contextual menu. Small adjustments to routed tracks can be made with the Route > Slide tool. Select the tool, click on a segment and slide it around. Allegro moves other tracks out of the way if necessary, which can be startling.

For larger changes, you might wish to remove part of a track or the complete track and redraw it.

- Move the mouse over a segment, which should highlight. If it does not, open the Find control panel and choose All On.
- You can delete the etch at three levels:
  - Delete removes the segment – a single straight line of track between corners or pins.
  - Connect Line > Delete removes the complete track (cline) between the two nearest pins or junctions.
  - Net > Ripup etch unroutes the complete net.
- Use Route > Connect to redraw the track.

Aaarghh! – I've just spotted an error in the circuit

If you spot an error in the circuit, rather than the layout, follow the instructions in section 10 on page 46. You can correct the schematic drawing in Capture and send only the changes to PCB Editor, which will make the minimal number of alterations to your board. It is *not* necessary to repeat the whole layout. This is one of the advantages of computer-aided design.

5.5 Add text

Next add some *silkscreen* text. This is printed on a commercial board using ink or paint rather than copper. It is used for component identifiers and other text needed to make to board easy to fabricate and use. In particular, all connectors (headers) must have the function of each pin identified as on the schematic. Your name would be useful too. There is no need to add labels for each component because these are shown automatically. (We cannot produce silkscreen in the department and use the copper layers if necessary.)

1. Start by putting your name on the board, which is always a good idea if you want to claim it. Choose Add > Text from the menu.

2. Open the Options control panel. You are probably getting the hang of the interface by now: choose a command, select options, then do it. Pin the Options panel open if your screen is large enough.

   - For a PCB that is made in the department, it is best to put text such as your name on the bottom layer of copper because this is part of every board. The Active Class should therefore be Etch and the Subclass should be Bottom.
   - Text on the bottom of the board should be mirrored so that it reads correctly from below, so select the Mirror box.
   - Text block is a confusing way of specifying the size of text. A larger number for the block produces larger text. Something like 3 is about right for your name.

3. Click in the design where you would like the text and type. Hit Return (Enter) to get a new line. Right-click and choose Done when you have finished or click to begin a new block of text elsewhere.

4. Now add some text on top of the board to identify the connectors. Again choose Add > Text but this time set the active class and subclass to Board Geometry and Silkscreen_Top. Turn off the mirroring and reduce the size to 2.

   Add text for Input and Ground on the input connector and Power, Output and Ground on the output connector. (There seems to be no way of transferring this information from Capture.)

Congratulations! – you have finished your first PCB. Don't forget to save it.

5.6 Print the design

The simplest way of printing the design is to 'plot' it (the usage goes back to the days of pen plotters). Select File > Plot Setup... from the menu and choose the following settings.

- Usually the Plot scaling should be unity so that the size of the printout matches that of the PCB. Our board is so simple that it is better to enlarge the drawing so enter 2 instead.
- Change the Default line weight to 10, otherwise the outlines are thin and indistinct.
- Set the Plot method to Color and close the dialogue box.

Open the Options control panel and set the Active Class and Subclass to Etch and Bottom. This will emphasize the most important features.

Now print your layout with File > Plot.... I suggest that you use the PDF printer first to save printer credits. Adjust the Print quality if necessary (probably not). The result should resemble figure 11 on page 24. Print it on paper using the colour printer, whose price has been reduced for this class. Stick the output in your laboratory record book.

If only a black-and-white printer is available, you have two options – neither satisfactory.

- Print the colour plot in black and white. The yellow tracks will probably be invisible.
- Change the Plot method to Black and white. The problem with this is that all colours are printed as black, which means that the components obscure the tracks.

None of these plots is useful for manufacturing the PCB. In the next design I'll show you how to get printouts that can be used to make your PCB in the department.

If the board is being produced commercially, you should next select Manufacture > Artwork. This produces files for the etch layers that can be sent to the manufacturer. The files are often called *Gerbers* after a major company and their RS274X format is widely used. Another file for drill holes is also needed. None of these steps are required for one-off PCBs made in the department. We produce the masks directly with the Plot command and the holes are drilled by hand.

☛ **Milestone:** Ask a member of staff to assess your finished design.

6 Instrumentation amplifier – single-sided board

The second design is another classic circuit, shown in figure 12. This is an *instrumentation amplifier* based on three op-amps. You will again study its operation in Analogue Electronics 2. Its main characteristics are as follows.

- High input impedance on both inputs because each is connected directly to the non-inverting input of an op-amp.
- The third op-amp acts as a subtracter to pick out the difference between its inputs (it can provide gain as well, but I have chosen not to do this).
- The gain for *differential* signals (the difference $V_+ - V_-$) can be adjusted with the single resistor R_2.
- The gain for *common-mode* signals (where $V_+ = V_-$) is very low.

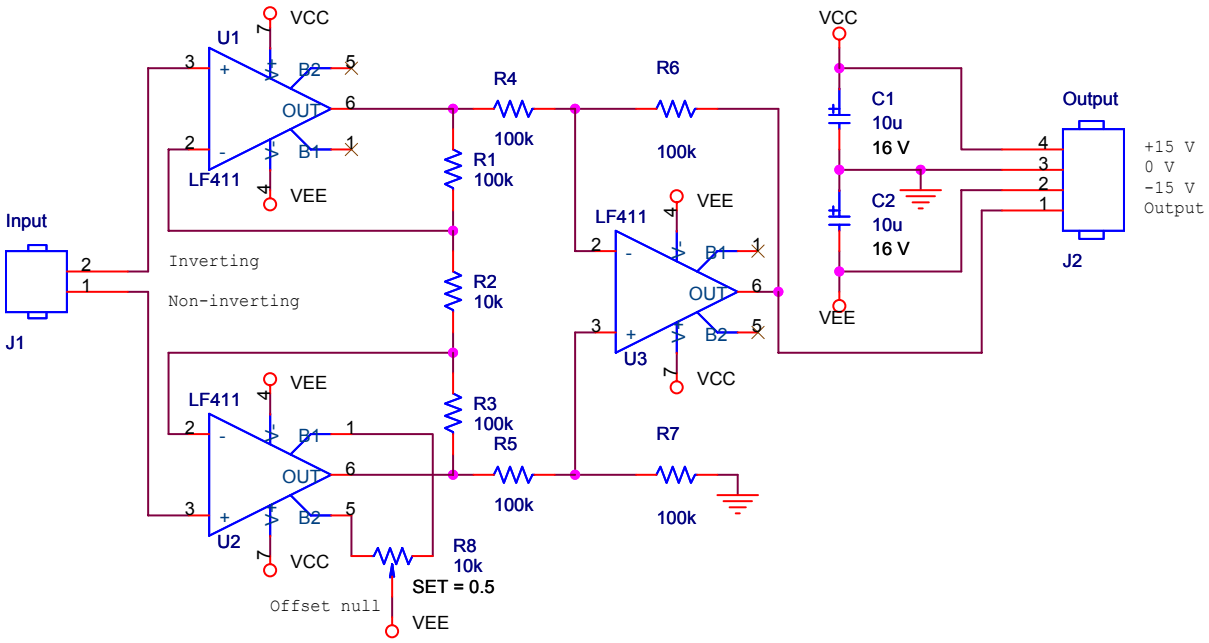

Figure 12. Instrumentation amplifier based on three op-amps.

The circuit is used to amplify a small difference in voltage between its two inputs while rejecting a large background or noise voltage that affects the two inputs equally. This is often needed with sensors, so remember this in Team Design Project 3. It may also be helpful later this year.

In practice it is unlikely that the circuit would be build using three separate packages with single op-amps as in this design. Complete instrumentation amplifiers are available in 8-pin packages. Even if these were unsuitable, you can get quad packages of four op-amps. However, it is probably easier to lay out this design than the quad package. We shall not simulate this circuit, just lay out the PCB. The LF411 is a widely used op-amp.

6.1 Schematic capture

Creating a directory for this design, as always, and start a new project in Capture. Place the components on the schematic but do not connect them yet. The only unfamiliar component should be the potentiometer, which is called POT – search for it.

Power supply rails are normally hidden to simplify the drawing. All power symbols with the same name are connected together.

1. Select Place > Power or click the power button on the right and select VCC_CIRCLE from the CAPSYM library. Use this for both +15 V and −15 V supplies. Mirror it vertically as necessary.

2. Select each power symbol in turn, right click to get the pop-up menu and select Edit Properties.... Change the name to VCC for positive and VEE for negative supplies respectively. This is a standard usage (but there are many others). Check the orientation of the op-amps carefully! I have mirrored some of them vertically to make the circuit clearer but this means that the power connections are reversed as well.

Table 2. Footprints for instrumentation amplifier.

Part	Name	Footprint
10µF capacitor	C_elect	RC100_RADIAL
Op-Amp	LF411	DIP8
Potentiometer	POT	VRES16
4-pin Header	HEADER 4	MOLEX4

3. Select GND from CAPSYM for the ground (earth) symbols. There are several to choose from but you must use the same one throughout your drawing.

You can now wire the components and add text to identify the pins in the two connectors.

An extra step is needed to mark the unconnected pins on two of the amplifiers. These pins are intended to be unconnected because they are for offset adjustment and it is only necessary to do this on one op-amp. Show that they are deliberately unconnected by choosing Place > No Connect from the menu bar or selecting the appropriate button on the right, then clicking on the pins. A small cross will appear as in figure 12 on the preceding page. PCB Editor expects every pin to be connected or explicitly marked as not connected.

Finally, run a Design Rules Check and correct any errors.

6.2 Set up a bare board in PCB Editor

Remember to make an allegro directory first. Set up the board as before (section 4.4 on page 13) but with these changes.

- Set the Minimum Line width to 20 mils and allow this value to propagate automatically into the other parameters. This is still wide by commercial standards but gives the narrowest tracks that can be produced in the department without extra care.
- Make the board $3.5'' \times 2.5''$, which gives you plenty of room despite the larger number of components. These dimensions are in inches, which you must convert to mils.

Save the board and quit from PCB Editor.

6.3 Identify and enter the footprints

You must next enter the footprints. I'm not giving you a table this time: You must work out which to use. There is a catalogue of our local library at the end of this handout and the components themselves are available in the laboratory so that you can match them up.

Hint for demonstrators. Table 2 shows suitable choices for the new components.

Fixup. There are again incompatibilities between Capture and PCB Editor that we must fix before making the netlist. First, the pins of the electrolytic capacitors are wrongly numbered. See section 4.1 on page 10 for the fix.

Fixup. The next problem is that only 7 pins are defined on the electrical symbols for the op-amps but the package has 8 pins. You might expect that the software would assume that undefined pins are not connected but it does not: It must be told this formally. This should have been done by Cadence in their libraries but we have to do it ourselves at present. Here's how.

1. Select one of the op-amps and choose Edit > Part, which brings up the Part Editor.
2. Choose Options > Part Properties. . . , which brings up the list of User Properties.
3. Click the New. . . button. Give the new property the name NC, which stands for No Connect, and the value 8, which is the number of the unconnected pin. (Use a list separated by commas, such as 7,8, if more pins are not connected.)
4. Click OK to get rid of the dialog boxes and close the Part Editor. Choose Update All so that this change is applied to all LF411 parts in your design.

Print your schematic when it has been completed correctly and survived the DRC.

☛ **Milestone:** Have your drawing checked before you go any further.

6.4 Import into PCB Editor and place the components

You can now create a netlist and send the design to PCB Editor as before. Check the Session Log: You can ignore any warnings (I got 6) about RVMAX and CMAX but check with a demonstrator if you get any others.

We'll place the components using a different technique this time. Choose Place > Quickplace. . . from the menu bar. The defaults should be suitable (Place all components, Around package keepin, Top). Click Place then OK. Your components are now arranged at the top of the board, ready for you to move them into position. Place the components to resemble the schematic drawing and adjust them to make the ratsnest simple with as few crossings as possible. *This is really important.* It is easy to route the tracks on a well-placed board; conversely, a poorly-placed board will need long, convoluted tracks or may even be unroutable.

Hint for demonstrators. Some students will complain that Quickplace has not placed their components. The usual problem is that the screen has been zoomed to fit the board but the components are above the board and therefore out of sight! ❦

Run a Design Rules Check when the components have all been placed and save your board.

6.5 Preparation for routing

It is usual to make power tracks wider than signal tracks as they have to carry more current. Our tracks are already so wide that it's barely necessary but we'll do it for future reference.

1. Choose Setup > Constraints > Physical. . . from the menu bar. This brings up the Constraint Manager and a Tip of the Day if you are unlucky (sigh).
2. The left-hand part of the window shows the various properties that can be edited. Click on All Layers under Net. See figure 13 on the next page for guidance.

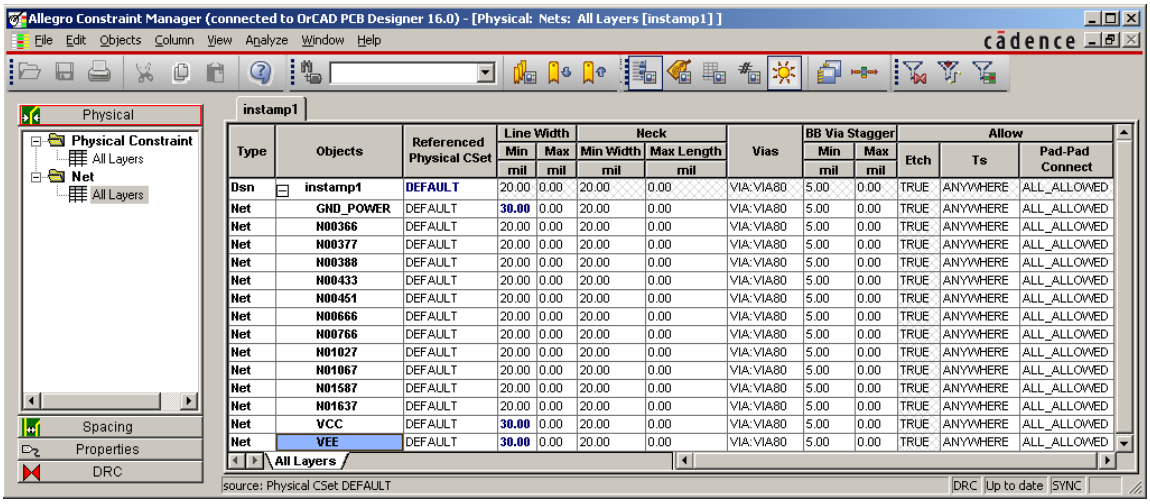

Figure 13. Constraint manager after changing the widths of the three power nets.

3. The main part of the window now shows a list of the nets in your design. Most of them have random-looking numbers, such as N00451, but a few are named. These are the nets that carry power, to which we assigned names in Capture: VCC, VEE and GND or something similar, depending on the symbol that you chose.

4. Change the minimum width for these three nets from 20 to 30 mil.

5. Choose File > Close to return to PCB Editor.

6.6 Autorouting a single-sided board

In this more complicated design we are going to use the autorouter to do the routing. You will do this twice: first as a single-sided board as in the one-transistor amplifier, and later as a double-sided board. It should be possible to route all tracks on the single-sided board if you have laid it out well but the double-sided board may have a simpler layout with a smaller total length of track. The Allegro autorouter is called SPECCTRA. Save your board before autorouting in case anything catastrophic goes wrong.

There are two ways of routing the board automatically, both shown in figure 4 on page 11: Everything can be done from within PCB Editor or you can run SPECCTRA as a separate application. The first is more convenient when it works but the second offers finer control.

Autorouting from within PCB Editor

Choose Route > Route Automatic... from the menu bar. This brings up the Automatic Router dialogue box. Unfortunately it often causes a fatal error message that SPECCTRA quit unexpectedly, in which case you will have to use the other method.

If it does work, select Use smart router for the Strategy. For a single-sided board deselect the box next to the TOP Routing Subclass. You might wish to experiment with the Routing Direction for the bottom layer. Click Route and wait for the results to come back. Click on the

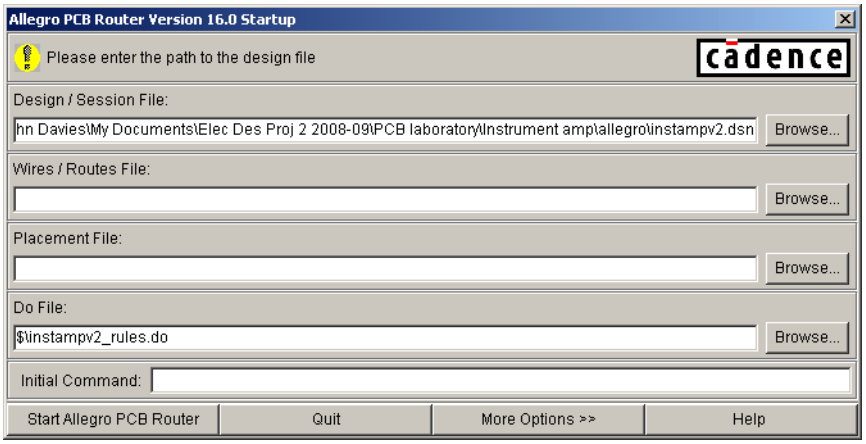

Figure 14. Startup dialogue box for importing a design into SPECCTRA.

Results button to find a report on the routing and check the Completion percentage to ensure that all nets were routed successfully. Save your board.

After all tracks have been successfully routed, choose Route > Gloss... from the menu bar. *Glossing* means to tidy up the design. This includes spreading tracks apart where possible and replacing 90° corners by 45° bends (mitring). Accept the defaults and gloss your design.

Warning. I have found that the gloss command occasionally unroutes some of the tracks, which revert to lines of ratsnest. Use View > Refresh to redraw the display and check carefully. Abandon the glossing if it has damaged your routing.

Finally, use Tools > Quick Reports > Etch Length by Layer Report to find the lengths of the tracks and add them up. In general, a better design has shorter tracks.

Autorouting with SPECCTRA

Use the manual equivalent of the automatic flow described in the previous paragraph if automatic routing does not work from PCB Editor. It's a bit clumsier but gives better control over the process and makes it easier to experiment with different settings.

Note. At some point you will probably get a Licensing Error warning from SPECCTRA. Click Ignore Feature for This Session if it appears.

1. Choose File > Export > Router from the menu bar of PCB Editor. It will ask you for a name for the Auto-Router Design file and you can probably accept the suggestion. Click Run. You may be warned about overwriting the file, which isn't a problem. A message Translation Completed should appear, after which you can close the box.

2. Start SPECCTRA for OrCAD from the Windows Start menu. You will be presented with the fairly complicated dialogue box shown in figure 14. Use the Browse... buttons to open the following two files.

    - For the Design / Session File (the first), choose the file that you just exported from PCB Editor.

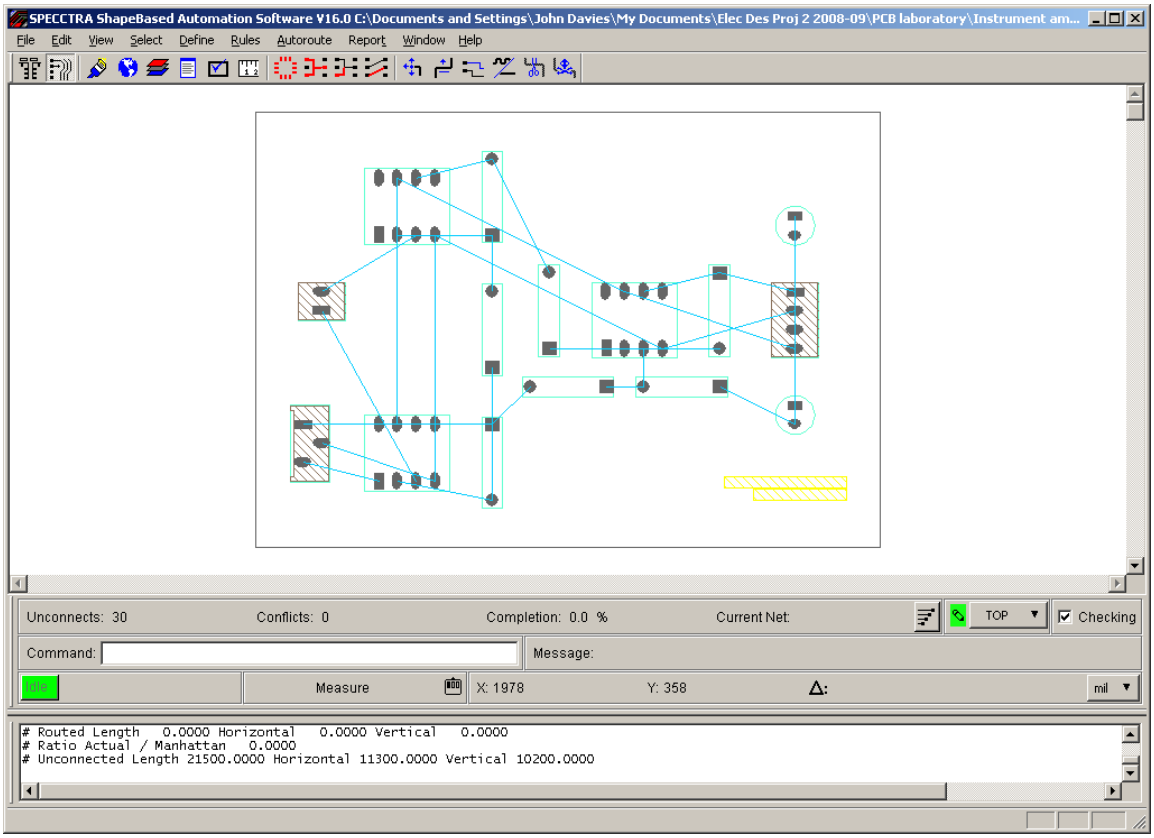

Figure 15. Screenshot of SPECCTRA, ready to route the instrumentation amplifier. I have changed the background of the window to white for a clearer printout.

- For the Do File (the last), choose the file that ends in _rules. The first part of the name should match your board file.

Click Start Allegro PCB Router to dismiss the box. SPECCTRA will now start and you should now see your components joined by the ratsnest within the outline of the route keepin as in figure 15. Some of the components have shaded footprints, which I'll explain later.

3. We must now tell SPECCTRA to route only the bottom layer. Choose View > Layers... from the menu bar. Turn routing off for the top layer by clicking on the drop-down menu next to TOP as shown in figure 16 on the next page and selecting the ⊘ symbol. You might like to experiment with the setting of the BOTTOM layer. The directions are hints to the router but in practice tracks will be drawn in both directions. Click Close when you have finished.

4. Choose Autoroute > Route.... Leave Smart selected and click OK. The autorouter will work away and you will see Message: Smart_route finished, completion rate: 100.00% if all is well. The tracks should be in colour, yellow for the bottom, if they are routed successfully. Sometimes they are drawn white, which should indicate a design rules error, even when they appear to be correct – I don't know why.

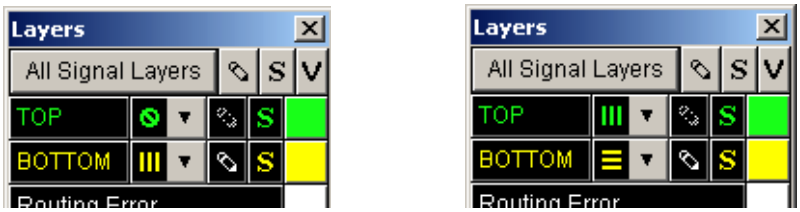

Figure 16. Settings in the Layers box for single-sided routing on the bottom layer and double-sided routing on both layers.

See the suggestions below if the autorouter is unable to route your board.

5. It is a good idea to use two more commands to improve the layout for assembly. First choose Autoroute > Post Route > Spread Wires... and accept the defaults. This spreads the tracks out a bit and keeps them further away from the solder pads.

6. You'll have noticed that the autorouted board has 90° bends in the tracks, which I told you to avoid when you routed the board by hand. We'll now sort this out. Run Autoroute > Post Route > [Un]Miter Corners... and accept the defaults. The corners will be rounded off and tracks run diagonally where possible.

7. To see the details of the finished layout, choose Report > Route Status. This will show a lot more than you want to know! Look near the bottom to find the Routed length and Unconnected length (which should be zero). Record these figures in your notebook.

8. Choose File > Quit... and agree to Save and Quit. This writes a *session* file that describes the routed tracks.

9. Return to PCB Editor and choose File > Import > Router.... Locate the Session File whose name matches your board and click Run. You should see a message Translation Completed. Close the box.

10. The window now shows your design with tracks instead of the ratsnest. Save it under a different name to preserve the unrouted board for later.

Hint for demonstrators. My layout is shown in figure 17. ❦

Help! – My board won't route

Here are some suggestions for helping the autorouter.

1. If the routing has almost worked (only one or two unrouted segments), try changing the hints given to the router. For the one-sided board there is only the suggested direction of tracks in figure 16. It is best to unroute the board and begin afresh. Choose Edit > Delete Wires > All Wires from the menu bar of SPECCTRA or reload the previous version of your board in PCB Editor.

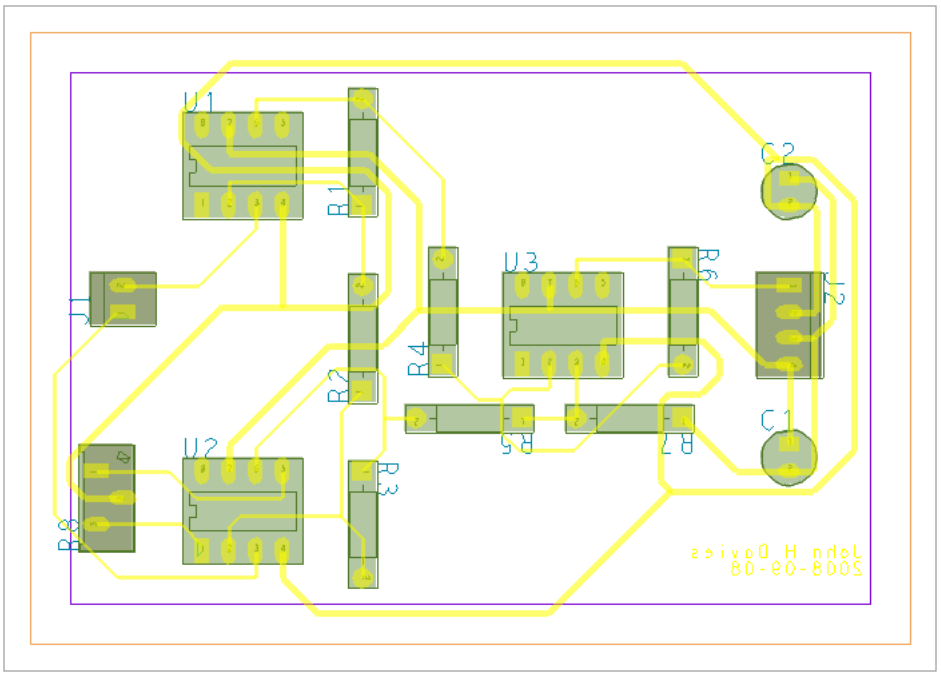

Figure 17. My one-sided layout after autorouting. The total routed length was 29.3″.

2. If you are far from success, look at the layout to see where the problems lie. Often there is one particular track that prevents successful routing. Can you see how to rearrange the components to get around the problem?

   Quit from SPECCTRA *without* saving or reload the previous version of your board in PCB Editor. Rearrange or reorientate components to make the ratsnest simpler and ease the problem before trying the autorouter again.

If none of this works, get advice from a demonstrator.

6.7 Final touches

Add text on the top silkscreen layer to identify all pins on the connectors and put your name on the bottom etch layer as before. Run a final design rule check and save your routed board.

6.8 Print the board and photomasks

First make a coloured print of the board as before.

The rest of this section explains how to get a black-and-white print that can be used as a photomask to manufacture your board in this department. I'm afraid that this is complicated because Allegro is not intended for such a primitive process. The problem is that we need small holes in the middle of the pads to act as markers for the drill. We have been promised this feature for the next release of OrCAD but it's not there yet. Here is the fixup for now. The idea is to change the colours of the layers and the order in which they are drawn on the screen to give the desired image. Save your design first in case something goes wrong.

1. Start by opening the Color Dialog box with Display > Color/Visibility... from the menu bar.

2. Click the button to turn Global Visibility Off, agree to the confirmation and click Apply (this is needed after every change to see the effect). The design vanishes from the main window.

3. Click Display in the list on the left. We want to change the Background colour of the window. Click a suitable colour in the Color swatches near the bottom of the window (dark grey is fine), then click the swatch next to Background. This will turn to the new colour. Click Apply to update the main window.

4. Now we need make the desired features visible again and paint them black. Start by selecting Board Geometry from the list. This brings up a set of Subclasses to the right. Select the checkbox next to Outline to turn it on. Change its colour to black by clicking in the black swatch in the Color region, then the swatch next to Outline. Finally, click Apply and the board outline should become visible in the main window.

5. This must be repeated for all the features that we wish to print. For the bottom of a PCB these are Stack-Up > Conductor > Bottom > Pin, Via and Etch. Activate them, make them black and click Apply. Your tracks will appear.

6. Now for the holes! Find Stack-Up > Non-Conductor > Pastemask_Bottom. This time click the checkbox in the All column and change the colour to white.

7. Click Apply – nothing happens! The pastemasks do not appear because white has a lower priority than other colours. Close the Color Dialog.

8. Open the colour priority control by choosing Display > Color Priority... from the menu. Scroll down until you find a white swatch. Click the swatch (not the check box), scroll back up to the top and click on the topmost colour swatch. It will turn white to show that white now has the highest priority and the other colours move down. White holes should appear in the middle of all the pads. Hooray!

   Sometimes this doesn't work because there is more than one white swatch, so you may have to repeat the process to bring all the white swatches up to the top.

9. Finally, choose File > Plot... as usual and you should get a beautiful picture with the board outline, etch and drill holes. Figure 18 on the next page shows my printout for the single-sided board.

10. These steps can be repeated for the top of a double-sided board.

After all this, quit from PCB Editor *without saving* (or reload your design) to avoid messing up the colours next time you use it.

☛ **Milestone:** Ask a member of staff to assess your design.

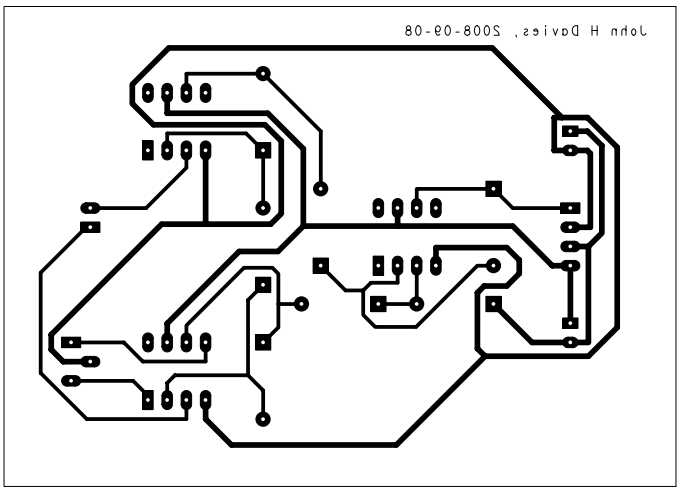

Figure 18. Printout at actual size for manufacturing a single-sided board (bottom layer) with holes in the pads to guide the drill.

7 Instrumentation amplifier – double-sided board

We will now route the board using both sides. Many simple, commercial boards are of this type, although four-layer boards are common for more demanding circuits and further layers are required for really complicated designs. Having said all that, *use a single side for your designs wherever possible*. There are many possible problems with double-sided PCBs, most of which arise from badly placed vias.

In a commercially produced board the copper plating extends through the holes, joining the pads on the two sides of the board. A plated-through hole that is used purely to move a track from one side of the board to the other is called a *free via*. Figure 19 shows the construction of a double-sided PCB. Unfortunately we cannot produce plated-through holes in the department, which is why you had to insert wires for vias and solder them top and bottom for the novelty lights in Electronic Engineering 1X.

It is also possible to use wires of components as vias. This works well for some components, such as resistors and capacitors. However, it does not work for others such as Molex connectors because it is impossible to solder the top of the board – the pad is hidden under the base of the connector. It works fine for an integrated circuit if it is soldered directly to the board but it is safer to put ICs in sockets and these hide the pads too. *Vias must therefore be placed with great care.*

To show these problems, figure 20 on the following page shows the two-sided layout of the instrumentation amplifier as it might come from the autorouter.

- There are five free vias on the board, far too many for a board that could be routed successfully with only one layer. The worst via is under U3, which is unacceptable for a home-made via (there would be no problem on a commercial board with plated-through holes). Another is very close to the trimmer (R8) and it would be difficult to solder this without damaging the trimmer. You would have to solder the via first and keep it neat.

- There are several more vias on pins of resistors – R3 has two, for instance. These shouldn't be a problem.

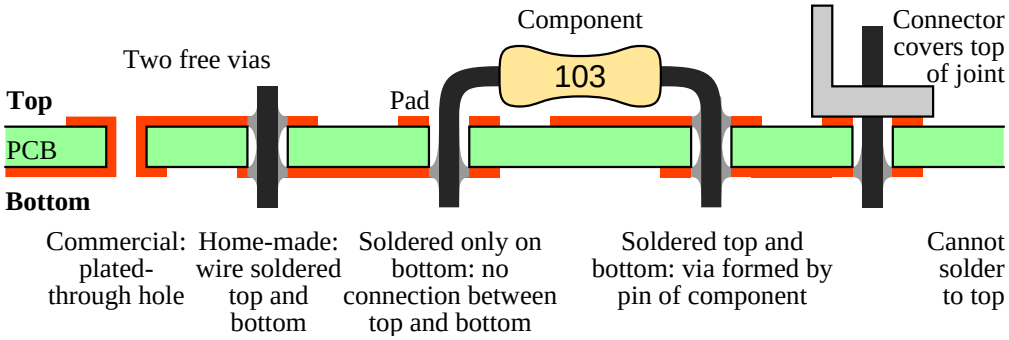

Figure 19. Cross-section of a double-sided printed circuit board showing free vias formed by a plated-through hole and a wire through a non-plated hole soldered top and bottom. A via can also be formed using a pin-through-hole component but not at a connector because it covers the top pad.

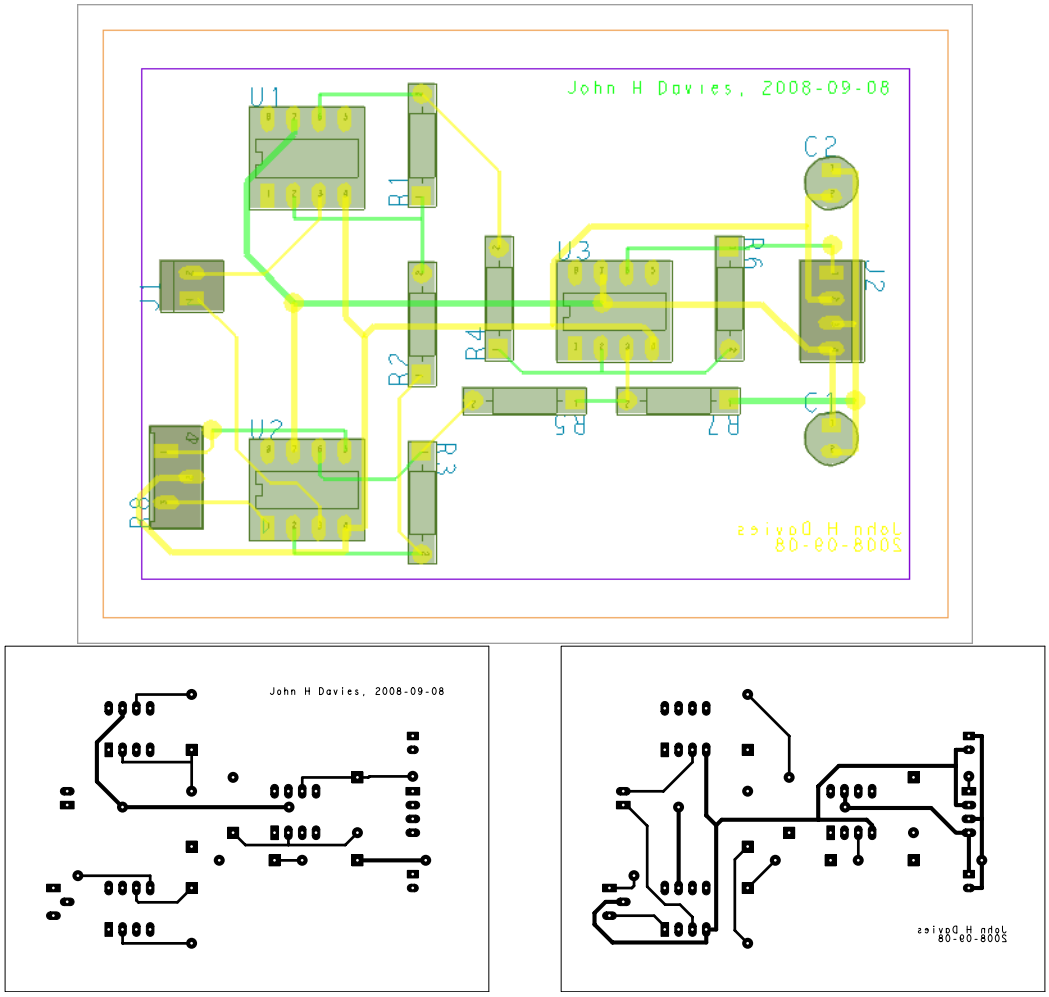

Figure 20. Screenshot of a bad double-sided layout with several badly-placed vias that might be produced by the autorouter. I've also shown the top and bottom photomasks.

- The pins of the integrated circuits are connected to tracks on both the top and bottom. This is no problem if the IC is soldered directly to the board but won't work if it is in a socket.

- The Molex connectors (J1 and J2) and the trimmer (R8) have tracks only to the bottom of their pins. This is why the via is needed near R8. There are no tracks to the top because the symbols for these components have *route keepouts* on the top, which forbid the router from running tracks there. The footprints have diagonal shading in SPECCTRA to show this, visible in figure 15 on page 33.

Now try routing your board using both sides.

1. Re-open the unrouted version of your board for the instrumentation amplifier.

2. Remember the Default via padstack when you used the new board wizard? We specified VIA80. Unfortunately there seems to be a bug with this because another type of via called simply VIA appears in the design and is used wrongly by default. The problem is that VIA is much too small to be soldered by hand so we must get rid of it.

   Fixup. Choose Setup > Constraints > Physical... from the menu bar. Select Physical Constraint Set > All Layers to bring up the spreadsheet shown in figure 13 on page 31. The column headed Vias for the DEFAULT row probably has VIA:VIA80. Highlight this cell and choose Edit > Change.... Remove VIA from the Via list on the right and click OK. The cell will change to VIA80, which is what we want. Close the Constraint Manager and save your board.

3. Run the autorouter from within PCB Editor or export the board to the router and start SPECCTRA as before. This time you should allow routing on both layers, which is the default. You might like to experiment with the directions on the two layers. Note the routed length and the number of vias; a good design may have none at all, which is a bonus. Remember to gloss or space and mitre the tracks.

4. Import the tracks into PCB Editor if you used SPECCTRA . Save the routed board under a new name.

You may get vias in inconvenient places, like that under U3 in figure 20 on the previous page. These must be moved. If you are lucky you may be able to use the Slide command on the via but it is often better to rip up the complete track and re-route it by hand. You will probably have to move other tracks to create space for the via.

- Select the cline or net with the offending via, right-click and choose Delete or Ripup etch from the contextual menu.

- Select one of the pins, right-click and choose Add connect. Check in the Options control panel that the correct layer is active.

- Draw out the segments of the track as usual.

- When you reach the point where a via is needed, right-click and choose Add Via. A via is inserted and routing switches to the alternative layer.

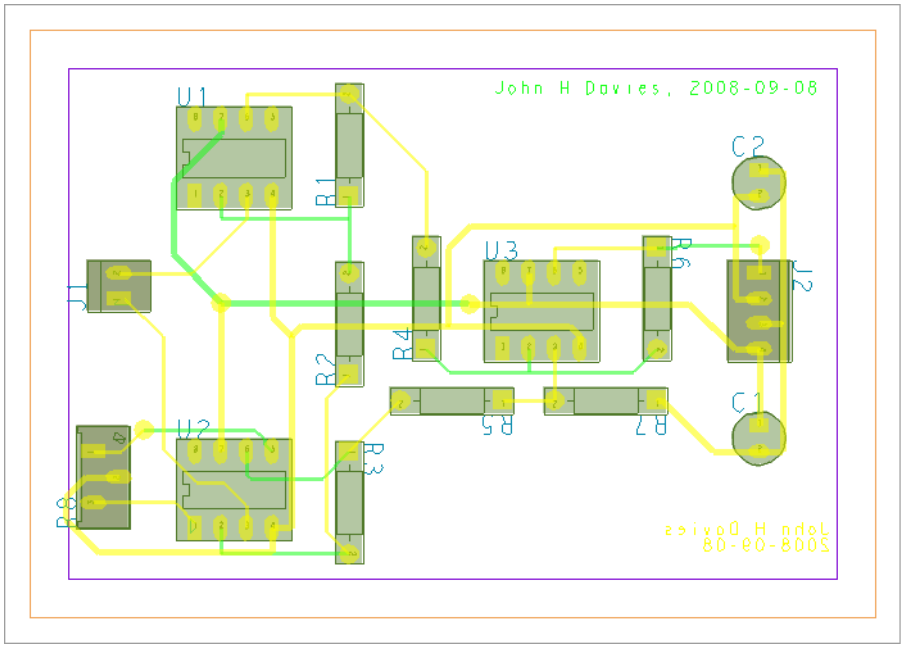

Figure 21. Double-sided layout after moving the badly-placed vias and other improvements.

- Continue routing to complete the track.

I made several changes to my board to get the final version in figure 21.

- I moved the via from under U3 to a clear region of PCB.
- I also moved the via away from R8.
- I eliminated the via near C1 by rerouting the tracks slightly.
- I moved several tracks from the top to the bottom, which will make the board easier to solder by hand.
- It would have been better to edit the board further so that all tracks leave the ICs on the bottom of the board. This would require extensive rerouting and more vias to be inserted.

When you have finished editing your board, add text on the top etch layer to identify both layers. It would be embarrassing if the top of your board was processed with the bottom of somebody else's. Finally, print the finished board in colour. For production you would need to produce separate masks for the top and bottom layers, following the instructions in section 6.8 on page 35. My masks before I tidied the layout are shown in figure 20 on page 38.

☛ **Milestone:** Ask a member of staff to assess your finished design.

8 A mixed-signal system

The final design is a *mixed-signal* system. This means that it includes both analogue and digital components like the final project in this course. In fact this design is one approach to the project

in 2007–08, which was an electronic weight scale. We used the MC9S08GB60 on a SofTec demonstration board and the display module from Embedded Processors 2. The project was to design and build the electronics required between the sensor and the microcontroller.

Figure 22 on the next page shows the circuit. These are its principal features.

- An *instrumentation amplifier* (again), which amplifies the small signal from the weight sensor. It includes adjustments for the gain and offset voltage.
- The output of the instrumentation amplifier enters an *analogue-to-digital converter* (ADC, part TLC549), which converts the analogue voltage to a digital value.
- The digital value is transferred to a GB60 microcontroller on a Softec board through a *serial peripheral interface* (SPI). Its signals are called MISO, MOSI (not used here), SCLK and $\overline{\text{CS}}$; the last is active low so I called it nSS on the diagram.
- Two pushbuttons are included on the board to *Tare* (set to zero) and *Calibrate* the system. They should be connected to general-purpose input/output (GPIO) pins of the microcontroller.

There is a 4-way Molex connector for the weight sensor and a 8×2 header (just two rows of pins) for a ribbon cable to the SofTec board.

I've used several new aspects of standard practice on this schematic drawing.

- The four opamps are in a single package, LM324. This is why they have the letters A–D at the end of their refdes. Capture automatically uses successive op-amps in a package until it runs out and needs a further package. You can see that the inputs and output of each op-amp have distinct pins but the power pins are the same for all four op-amps.
- Many connections are made by name rather than drawing lines. You have seen some of these before, such as VCC and GND. Others are made by adding a *net alias* to wires.

  1. Draw a short wire on the appropriate pins.
  2. Choose Place > Net Alias... from the menu bar or use the button.
  3. Enter the name for the Alias and click OK.
  4. Click on the wire(s) that you wish to name.

  This practice is particularly common in digital circuits.
- Although the power pins of the opamp are shown (they are often hidden completely), I have not connected them to power and ground explicitly. Instead they should be connected by name. I've added an extra power symbol called V+ for the positive supply.

  You must add a further symbol to connect V– to ground. The shape of the symbol doesn't matter, just its name. (The op-amps are used in a *single supply* configuration, where their negative supply pin is connected to ground rather than a negative voltage.)
- The power pins of the ADC aren't shown at all, but of course it must have them. (Although the REF+ and REF– pins are connected to VCC and ground, these are actually reference voltages rather than power.) Find the names of the power pins by opening the

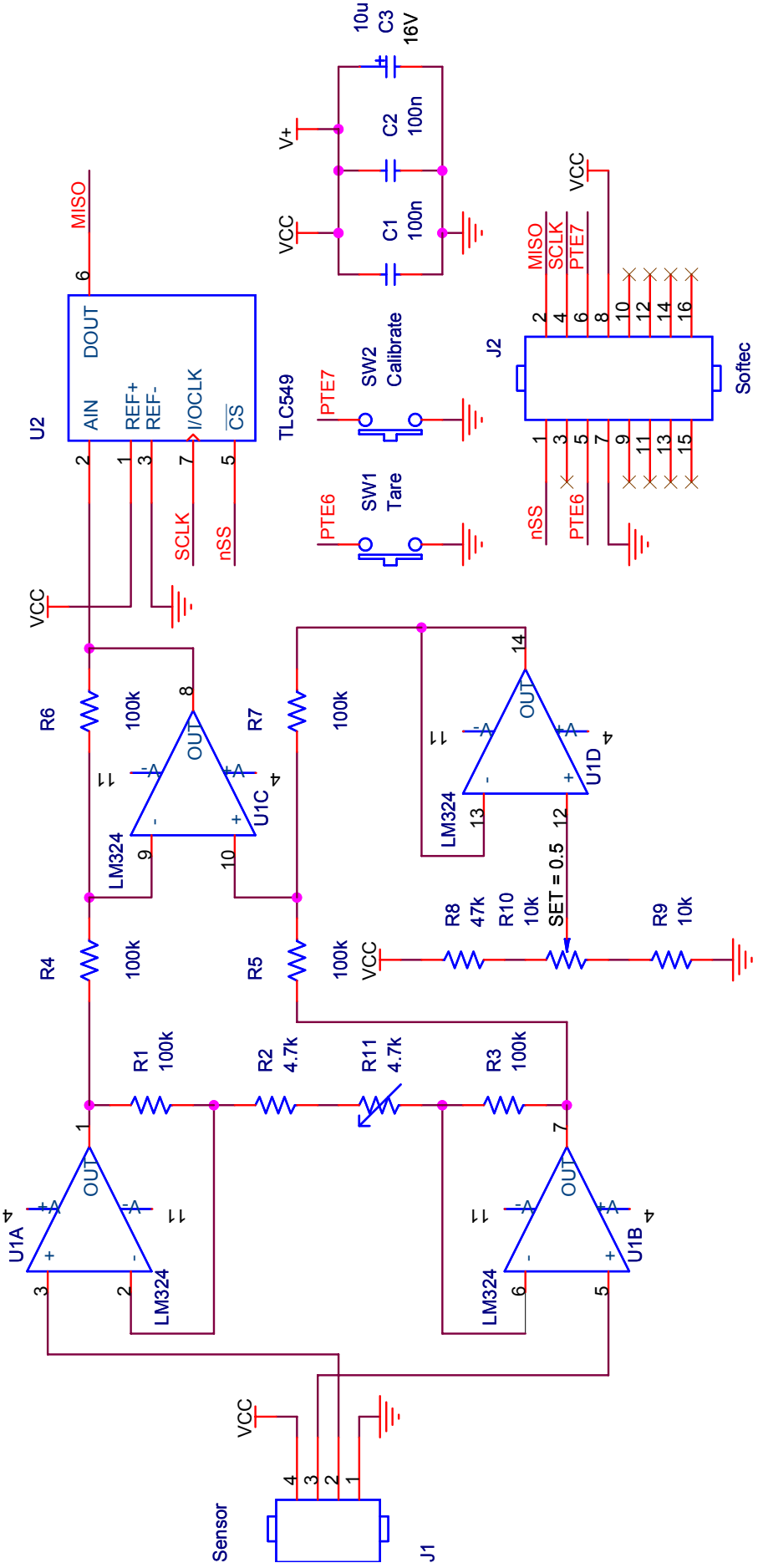

Figure 22. Instrumentation amplifier and analogue-to-digital converter for an electronic weight scale.

Property Editor with Edit > Properties. . . . Make the Pins sheet active instead of the usual Parts. This shows the numbers and names of the pins (and more). Make sure that the names are defined elsewhere to provide the correct connections.

- Why three capacitors in parallel? These are for decoupling noise away from sensitive components and must be positioned carefully when you lay out the board. One of the 100 nF capacitors should be as close as possible to the power pins of the op-amp and the other should be as close as possible to those of the ADC. The 10 µF capacitor is electrolytic and its placement is less critical.
- The variable resistor R11 is a 'virtual component' and must be replaced by a real component in your schematic. How is this done?
- The pushbuttons are in a local Capture library called projects, which is in the tdp3_orcad folder on the Elecapps networked drive.
- Note the orientation of the 8×2 header carefully. Pin 1 is top left when viewed from the top of the board but the part is mirrored in some libraries.

Hint for demonstrators.

1. A power or ground symbol called V– must be added to the ground net. (There is a convenient space below V+!)
2. The power pins of the ADC are called VCC and GND so they are automatically connected without further effort.
3. The variable resistor must be replaced by a potentiometer, whose wiper is connected to one end (it doesn't matter which).
4. Check the orientation of J2 despite the warning in the instructions.

☛ **Milestone:** Ask a member of staff to check your schematic drawing before proceeding. Here are a few more points to help you lay out the PCB.

- The footprints for the pushbutton have four pins but the capture symbol has only two pins. You must therefore create a NC property with the value 3,4 to mark these pins as unconnected, as for the op-amp on page 30.
- I've provided the front pages of the data sheets for the LM324 and TLC549 so that you can see the pinouts and general features.
- Aim to keep the noisy, digital SPI away from the sensitive analogue inputs.
- The four op-amps within the LM324 are identical so you might wish to swap them around to get a better layout – I assigned the four randomly.
- Make the power and ground tracks wider as usual.

- Select footprints using the components available in the laboratory, as before.
- Mark pin 1 of the 8×2 header clearly on the top of the board to show which way the cable should be plugged in. The ribbon cable has a red stripe to identify pin 1 of the connector.

Hint for demonstrators. The symbol for the pushbutton should be redrawn so that pairs of pins are connected together, rather than marking two as not connected. ❦

Most of the design should work as before but you may encounter a puzzling new 'feature' of PCB Editor: the nets for VCC and ground do not appear in the ratsnest. The reason is that separate planes in the PCB are often used for power and ground, in which case there is no point in showing the connections – they are made directly to the planes. PCB Editor therefore hides the nets by default. This isn't useful for our single and double-sided boards so make the nets visible again as follows.

1. Choose Edit > Net Properties... to bring up the Constraint Manager, then Net and General Properties.
2. There is a column headed No Rat and the entry is probably On in the rows for VCC and GND. Change these entries to (Clear), which should empty the cells.
3. Quit from the Constraint Manager and the nets should reappear in the ratsnest. Seek expert advice if they are still invisible.

Hint for demonstrators. This doesn't always happen – I think that it depends which alias 'wins' for the nets. If this method doesn't reveal the nets there are further suggestions in section B.6. ❦

☛ **Milestone:** Ask a member of staff to assess your finished design.

9 Summary: PCB design flow

This list is adapted from a handout by Mr I. Young. *Save your work frequently!*

1. Draw the circuit in Capture.
    - Make a new directory for each design.
    - Check the circuit carefully.
    - Make sure that all power connections are included. If you are using integrated circuit with hidden power pins you must place correctly named power symbols on the power supply lines to ensure the IC power pins are appropriately connected.
    - Add footprints from our local library.
    - Edit components with incorrectly numbered pins, such as electrolytic capacitors.
    - Mark all unconnected pins and add the No Connect property to packages with unused pins.
    - Run a Design Rules Check and correct any errors.
2. Set up a bare board in PCB Editor using the New Board Wizard.
    - First make an allegro directory.
    - Use 20 mil design rules so that your board will be easy to etch and solder.
    - Make the size of board generous; you can reduce it later.
3. Netlist the design in Capture. Check any warnings.
4. Place the components on the board in PCB Editor.
    - Arrange and orient the components to simplify the ratsnest as far as possible. *This step is critical to get a well-routed board.*
    - Add mounting holes if required (not explained in these notes).
    - Use wider tracks for the power supplies and fix the list of vias.
    - Run a Design Rules Check and correct any errors.
5. Route the board.
    - Manual routing is best for a simple design (which includes most of ours).
    - If you must use the autorouter, try a single-sided board first. Check that the completion rate is 100%.
    - If only a few tracks are not routed automatically, do them by hand and put vias in convenient places. Use wires on top instead of requesting a double-sided board.
    - If you must use a double-sided board, review the results of the autorouter carefully and move any vias and tracks on the top that cannot be soldered easily.
    - Gloss the design in PCB Editor or SPECCTRA.
6. Add text to identify the board and connectors.
7. Write photomasks as pdf files at actual size. We will print the masks on tracing film.

10 How to correct a layout if you spot an error in the circuit

It sometimes happens that you spot an error in a circuit after you have done most of the layout. It would be highly irritating if you had to do the whole layout again. The good news is that you do not have to start from scratch. It is surprisingly easy to make corrections and you already know the steps.

1. Save your board and quit from PCB Editor.
2. Re-open Capture and make the corrections to your circuit. Always run a DRC before proceeding.
3. Repeat the instructions in section 4.5 on page 16 for creating a netlist and sending it to PCB Editor. Just make these small changes.
   - For Input Board File, choose the board that you just saved in PCB Editor – the most recent version of your layout.
   - Use a distinct name for the Output Board File to create a new board.
4. The new board will open in PCB Editor with the minimum number of changes to accommodate the revisions to your circuit. You will have to place any extra components and re-route any tracks that were disturbed.

The jargon for this process is that Capture sends an *Engineering Change Order* (ECO) to PCB Editor.

A Where to learn more

The online help for Cadence OrCAD PCB Designer is poorly organised. There is no way of searching more than one file at a time for text, which makes it very difficult to solve problems until you know most of the answer already! The help documents are no more than online versions of the manuals, which are supplied as pdf files – over 100 of them. Unfortunately their names are cryptic so it isn't even easy to work out which to read, and the interdocument links have been set up in a way that works only on unix. Here is a guide to the most helpful documents with their filenames (all have the extension .pdf). The documentation is not entirely consistent with our version of PCB Editor.

- The *OrCAD Flow Tutorial* (flowtut) takes you through the complete process of capture, simulation and PCB design and covers several techniques that I have not described in these notes.
- *OrCAD Capture User's Guide* (cap_ug) has a particularly relevant chapter on *Using Capture with PCB Editor*, which includes issues such as assigning the No Connect property.
- *PSpice User's Guide* (pspug) describes simulation and analysis.
- The *Allegro PCB Editor User Guide* (algromast) is the most helpful set of documents for this piece of software but is so long that it is split into 12 further documents, of which these are most relevant:

  1. *Getting Started with Physical Design* (algrostart). This is the most useful document for learning how to use Allegro, much better than the tutorial.
  2. *Defining and Developing Libraries* (algrolibdev). Mostly devices, symbols and padstacks but also technology files.
  3. *Transferring Logic Design Data* (algrologic). Despite the name, this means importing from Capture or a similar application and includes analogue components.
  4. *Preparing the Layout* (algrolay). This includes the cross-section of the board, keepins and keepouts, padstacks and etch shapes – fills or pours.
  5. *Creating Design Rules* (algrodesrls). I've barely looked at this.
  6. *Placing the Elements* (algroplace). Most of this is rather advanced too.
  7. *Routing the Design* (algroroute). This describes different strategies for routing, both manual and automatic, and covers fanouts, which I have not mentioned.
  8. *Completing the Design* (algrodescmp). Another one that I have barely opened.
  9. *Preparing Manufacturing Data* (algroman). Covers the final steps needed to send a board for commercial manufacture – silkscreens, artwork (Gerbers) and drill files.

  You might also need the *Allegro Constraint Manager User Guide* (cmug). The *Allegro PCB Editor Tutorial* (algrotutorial) concentrates on the user interface and doesn't tell you how to do much.

- Routing from PCB Editor, both manual and automatic, is explained in the *Autorouting with Allegro PCB Editor Tutorial* (aleg_spec_tut). The *Allegro PCB Router Tutorial*

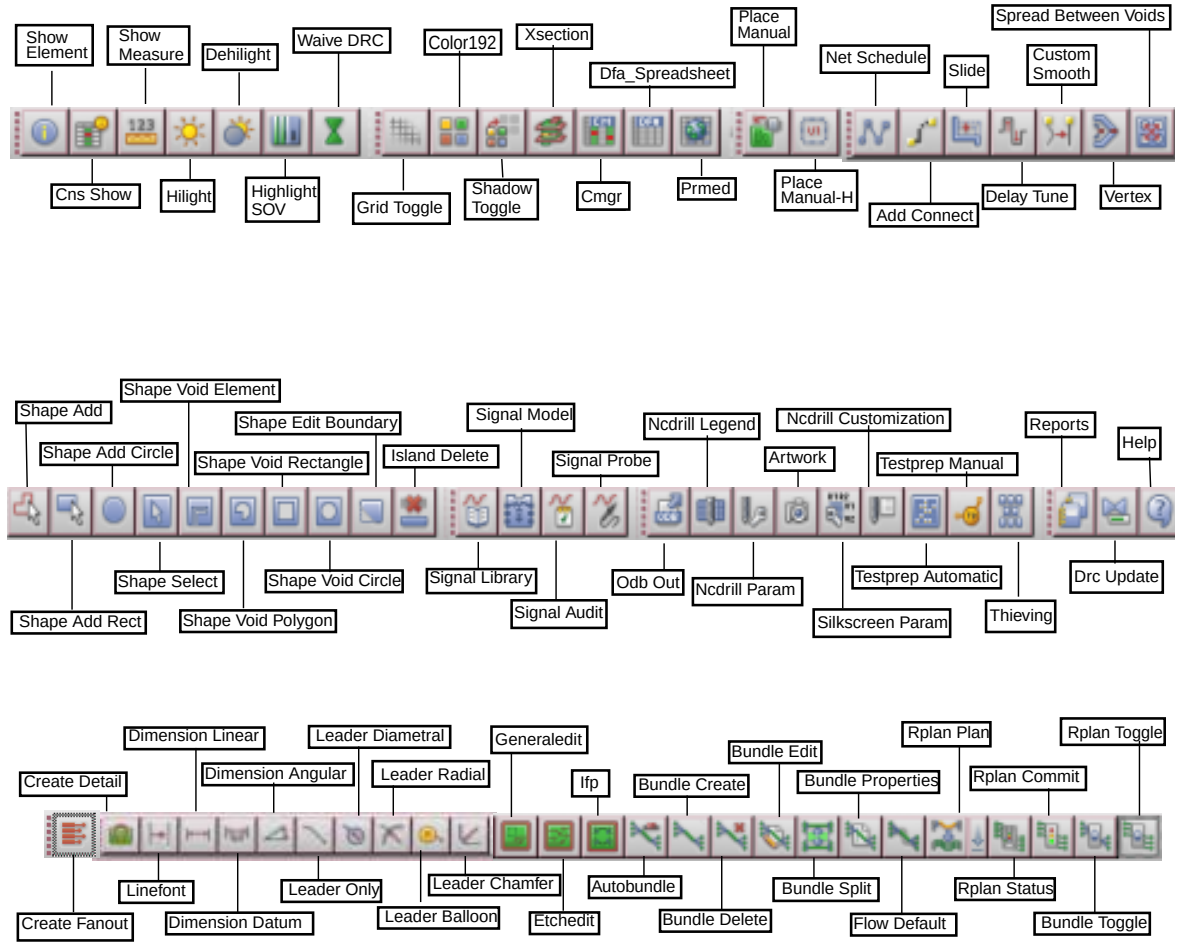

Figure 23. Toolbars in Allegro, taken from the *Allegro PCB and Package Physical Layout Command Reference*. Not all of the buttons are available in OrCAD PCB Editor and many provide functions that I have not described.

(sptut) explains routing within SPECCTRA itself, for which the complete reference is *Allegro PCB Router User Guide* (spug).

- If you know precisely which PCB Editor command is involved, there is a file for commands starting with each letter. They are called *A Commands* (acoms) to *Z Commands* (zcoms). The names of the commands are not always obvious, in which case the *Allegro PCB and Package Physical Layout Command Reference* (cmdrefmast) is the place to start. The new board wizard is under L (layout wizard), for instance, which confuses me repeatedly. Figure 23 for the toolbars is taken from this manual.

B Power-user tips and random jottings

This is a disorganised collection of techniques that I have found useful but seemed too complicated for the body of this handout (which is already far too long).

B.1 Modes of operation

I didn't dwell on this in the instructions because we would all rather try out the software than read a lengthy 'theory of operation' but here is a little more. The main point is that the tools in PCB Editor can be used in two different ways (see page 23 of *Getting Started with Physical Design* for further details).

- **Menu-driven editing mode or verb–noun use model**. In this mode you first choose a command, either from the menu bar or by clicking a button, then the design element on which the tool should operate.

- **Pre-selection mode or noun–verb use model**. In this mode you first choose the object followed by the command, which is usually selected from the contextual menu by right-clicking.

The verb–noun approach is a little more cumbersome but it is much easier to see what is happening, particularly if you keep the control panels open. For example, if you choose Add Connect, the Find panel automatically selects Pins, Vias and so on – the items to which a connection can be added. The Options displays the etch layers available and options for the tracks, such as width and angle of bends. If the Move command is selected instead, different options are offered and other classes are activated in Find.

The noun–verb model is often more convenient when you know what you are doing and want to perform a set of operations on an object. However, there is a huge number of possible operations and they don't all fit into a contextual menu. PCB Editor therefore has two *Application Modes*, which can be selected from the menu bar with Setup > Application Mode or with a button. These are the modes.

- **General Edit** (GEN). This is the most useful mode and is intended for arranging components and adding connections.

- **Etch Edit** (EE). This is mainly for editing tracks that have already been routed.

The current mode is shown near the right-hand end of the status bar below the windows.

The particular set of commands in the contextual menu depends on exactly what is selected. You may therefore need to adjust the Find control panel before you are able to select the desired element – a pin for Add Connect, for instance.

Fancier versions of Allegro have a third mode for Flow Planning and there is an empty space on the button bar for it but it is not available to us. A Placement mode is due to be added soon.

Use Setup > Application Mode > None to exit from the current application mode and return to a menu-driven editing mode (there is no button). No contextual menu is available and the Find control panel is deactivated until a tool or application mode is chosen again. If PCB Editor appears 'dead' there is probably no application mode selected.

If that isn't enough, there are further shortcuts described on pages 34–35 of *Getting Started with Physical Design*. These are the actions that take place by default when you click and drag on an object, often while holding a modifier key down, and are the quickest ways of performing the most common actions. For example, in general editing mode:

- dragging a symbol, text or via moves it
- control-dragging a symbol, text or via duplicates it
- shift-dragging a symbol rotates (spins) it
- dragging a cline segment slides it

Similarly, in etch editing mode:

- dragging a cline segment slides it
- double-clicking a pin or via adds a connection (and this can be shortened further to a single click with the contextual menu Customize > Enable Single Click Execution)

That should be enough for now!

B.2 Design rules, particularly width of tracks.

The suggested design rules do not permit a track to run between the pads of of an integrated circuit, $0.1''$ apart. This keeps the board easy to solder but makes it more difficult to route. If you wish to allow tracks between the pads, reduce the Minimum line to pad spacing to 12 mils in the New Board Wizard. For an existing design use Setup > Constraints > Spacing... to bring up the Constraint Manager, select Spacing Constraint Set > All Layers and change the appropriate entries from 20 to 12. You will need to solder the board carefully!

It can be helpful to change the width of a track along its length, particularly if the tracks are narrow, because our etching process tends to attack long, isolated tracks; keep them at least 20 mil wide. You can change the width during manual routing with the Options control panel or contextual menu.

B.3 Editing padstacks to include guide holes for drilling

Here's how to fix the padstacks so that they can be plotted with a guide hole for drilling. The trick is to use the solderpaste layer for the guide hole. (I'm grateful to redwire and other members of the Cadence forum for help with this. The procedure should become obsolete with version 16.2.) See *Library Padstacks* in *Defining and Developing Libraries*, *Layout Padstacks, Vias, and Etch Shapes* in *Preparing the Layout*, and *Padstack Designer* in *P Commands* for full details.

1. Right-click on a pin and choose Modify Design Padstack > All Instances. Alternatively, choose Tools > Padstack > Modify Design Padstack... from the menu bar and select a padstack either by clicking or from the Options control panel. The Padstack Designer starts.

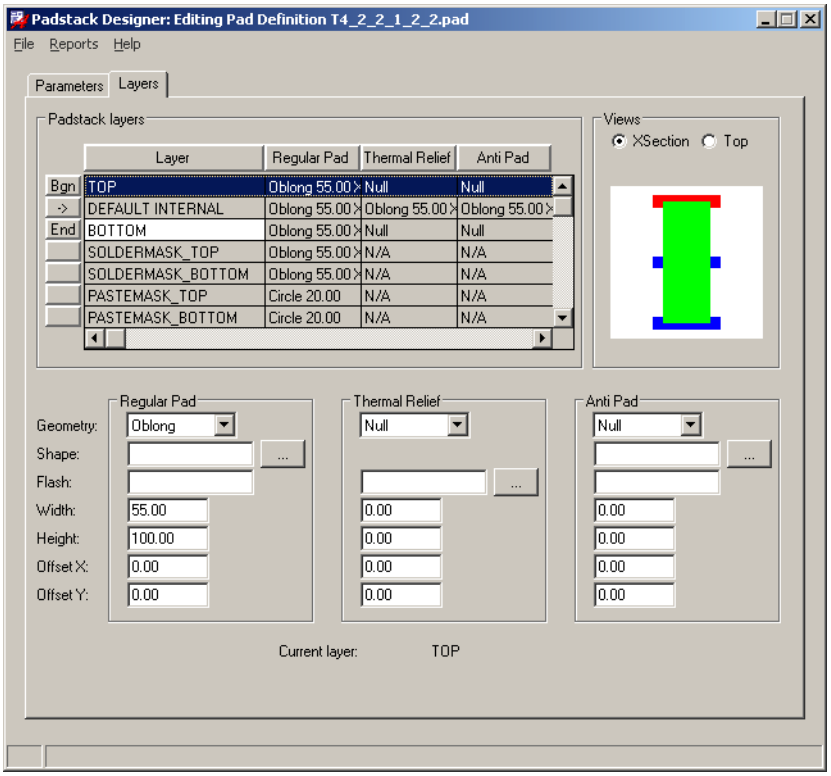

Figure 24. Padstack editor settings with a pastemask to act as a dummy hole.

2. You will probably see the Parameters tab first. There's probably no need to touch this unless you want to adjust the diameter of the hole.

3. The Layers tab needs the work. See figure 24. I'm not sure what the Thermal Relief and Anti Pad should be, but these settings avoid complaints.

    - The TOP and BOTTOM layers should have the dimensions of the copper under Regular Pad. It is best to set the Thermal Relief and Anti Pad to null.
    - The DEFAULT INTERNAL layer has the same dimensions in all three categories.
    - SOLDERMASK_TOP and SOLDERMASK_BOTTOM have the same size Regular Pad as the others.
    - I have edited the PASTEMASK_TOP and PASTEMASK_BOTTOM to have a circular Regular Pad with diameter 20 mil. This will become the guide hole in the final plot.

There are further commands to replace padstacks and to purge unused padstacks from a design.

B.4 Pours or fills

It is easy to fill the unused areas of an etch layer with conductor to provide screening. This is called a *dynamic etch shape* in Allegro and the procedures are described in *Preparing for Layout*, although it doesn't seem entirely consistent with OrCAD PCB Editor. A dynamic

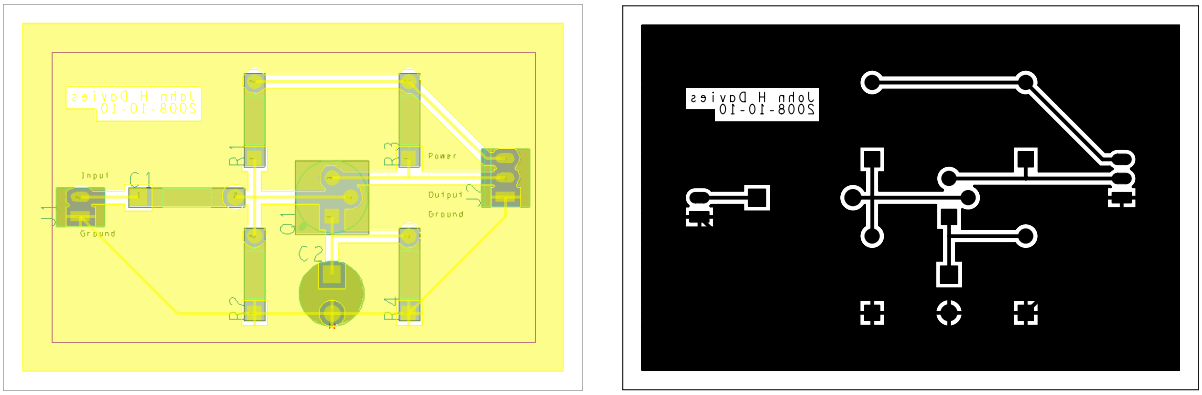

Figure 25. Screenshot and photomask for the one-transistor amplifier with a solid dynamic shape attached to the ground net. Pins are connected to the shape through thermal-relief pads and I haven't bothered to show drill holes.

shape is automatically redrawn in response to changes in other elements, unlike a static shape whose outline is fixed. In this case the filled area will reflow around tracks if they are moved.

I have used the one-transistor amplifier as an example, starting with the finished design at the end of section 5. Figure 25 shows the PCB with a solid fill attached to the ground net (I'll make it cross-hatched later).

1. Choose Shape > Global Dynamic Params... from the menu bar to set up the parameters first. There are several tabs.

   - Shape fill – increase the Line width and Spacing from 5 to 20 mils, consistent with our coarse design rules. The Border width becomes 20 automatically. I used the default Hori_Vert fill style.
   - Void controls – set the artwork format if necessary.
   - Clearances – increased to 20 mils.

2. Select Shape > Rectangular from the menu bar and check the settings in the Options panel. The shape should be in the Bottom Etch layer, Dynamic Copper, connected to GND; select the net with the '...' button.

3. Draw a large rectangle to include the whole board. It will automatically be trimmed to the route keepin and PCB Editor creates spaces (voids) around the pins, tracks and text.

That's it! A screenshot of the filled board is shown in figure 25 and I plotted the photomask in the usual way (but forgot about the drill holes). An empty area called an *antipad* is left around pins of nets that are not connected to the fill. You might have expected that grounded pins would be surrounded immediately by fill but instead each pin has a *thermal relief* around it. This is an empty region crossed by a few lines of etch to provide electrical contact.

The reason for the thermal reliefs is that copper conducts heat as well as electricity. A pin surrounded by a large area of etch will therefore tend to cool more quickly after it has been soldered than one that has only a pad and a track. All pins must cool at about the same rate to give consistent joints if the board is soldered automatically so thermal reliefs are used whenever

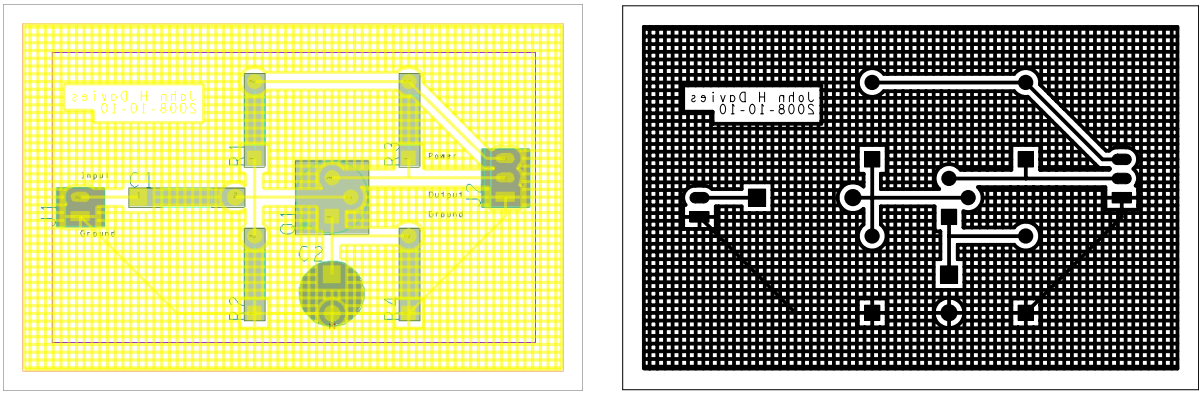

Figure 26. Screenshot and photomask for the one-transistor amplifier with a hatched shape attached to the ground net. The tracks for the ground net are now visible.

pins are connected to planes of etch rather than tracks. It isn't such an issue when boards are soldered by hand; in fact the usual problem is overheating of small pads.

As far as I can tell, dynamic shapes always have solid fill in our version of PCB Editor. You can change the fill to cross-hatched or another pattern but the shape then loses its dynamic property. This should therefore be left to the final step.

1. choose Shape > Select Shape or Void from the menu bar and select the shape.

2. Right-click and choose Parameters... from the contextual menu. Change the Fill style on the Shape fill tab. Other parameters are inherited from the global dynamic parameters that you set up earlier.

Figure 26 shows a screenshot and photomask for a hori_vert fill. The shape is now static and will *not* be redrawn if you make changes such as moving a track.

B.5 Alternative design flow

If you don't like the idea of the new board wizard, you can follow a more conventional but clumsier flow to start the board. It gives a little more control.

1. Send the netlist from Capture to PCB Editor *without* first setting up a bare board. Leave the Input Board File empty in the Create Netlist dialogue box, figure 7 on page 17.

2. In PCB Editor, use Setup > Outlines > Board Outline to define the outline of the board and the route and package keepins, which are made identical. The same dialogue box can be used to change these outlines later. You might wish to draw a different route keepin with Setup > Areas > Route Keepin.

   I have not tried placing the components first and subsequently drawing the board outline and keepins around them. You would obviously have to keep DRC off.

3. Import a technology file with File > Import > Techfile when we set one up! Until then you will have to work through the steps below.

4. Use Setup > Cross-section to define the number, names and types of layers. The default is two layers, which is fine.

5. Set up the grids with Setup > Grids. I suggest 100 mil for the non-etch layers and 25 mil for the etch.

6. Define the widths of tracks with Setup > Constraints > Physical and the separations with Setup > Constraints > Spacing. While you are doing this, edit the vias in the Physical pane as described on page 39.

7. You might wish to tweak some of the parameters in Setup > Design Parameters > Display, such as the display of drill holes and the ratsnest. Their visibility is treated differently from other elements of the design. (At present you can display the drill holes on the screen but not plot them.)

B.6 Disappearing ground and power nets

PCB Editor likes to hide the nets for power and ground signals when it draws the ratsnest, which is unhelpful for us. Unfortunately it has several ways of doing this, which require different techniques for making them visible again. You might hope that Display > Show Rats > All would do what it says, but it does not! Here is the simplest method, given in the main text but repeated here for convenience.

1. Choose Edit > Net Properties... to bring up the Constraint Manager, then Net and General Properties.

2. There is a column headed No Rat and the entry is probably On in the rows for VCC and GND. Change these entries to (Clear).

3. Quit from the Constraint Manager and the nets should reappear in the ratsnest.

If that doesn't work, or the apparently unconnected pins are shown with a Boxed X (like a checkbox), here is the next method.

1. Choose Edit > Net Properties... to bring up the Constraint Manager, then Net and General Properties.

2. Delete any entries in the column headed Voltage. These are constant (DC) voltages and therefore indicate a power supply.

3. Quit from the Constraint Manager and the nets should reappear in the ratsnest.

If that doesn't work either, here's my final method.

1. Select the missing nets. That sounds tricky but is not. Set the Find control panel for Nets, hover the mouse over one of the unconnected pins and its net is selected (and named on screen).

2. Right-click and choose Property Edit. Two boxes appear: Edit Property and Show Properties.

3. The list on the right-hand side of the Edit Property box should show Ratsnest_Schedule and its value is probably POWER_AND_GROUND. Click the Delete check box to get rid of this property. If there is a Voltage property, delete that too.

4. Click Apply and the net should reappear. Click OK to get rid of the Property Editor.

B.7 Copying the names of pins from Capture to PCB Editor

In section 4.1 on page 10 I ask students to label the pins of the connectors on the schematic drawing, as in figure 5 on page 11. Later, in section 5.5 on page 26, I ask them to write the same text to label the pins on the PCB, as in figure 11 on page 24. This is a stupid procedure because the two sets of labels might be inconsistent. It would be far more reliable if the names were copied automatically from Capture to PCB Editor. This can be done but is not as straightforward as it might be. These instructions are based on advice from Joewi, redwire, tltoth and oldmouldy in threads 10494 and 10835 on the Cadence PCB Design Forum.

1. In Capture, select the components whose pins are to be named. Open the Property Editor and choose the Pins sheet.

2. Click New Row... (or New Column...) to create a new property and give it an appropriate name, such as SSNAME (for silkscreen name).

3. Enter names for each pin into the row for SSNAME. Make the property visible with Display... so that it shows on the schematic.

4. Two steps are needed in the Setup dialog box (figure 7 on page 17) for netlisting the design and sending it to PCB Editor. First, the easy one: Activate the checkbox for Allow User Defined Property.

5. Click on the Setup... button across from Create PCB Editor Netlist. The dialog box shows the Configuration File, called allegro.cfg. We need to Edit... this.

   - Add the line SSNAME=YES to the section for [pinprops] at the end of the file, which tells the netlister to include this property in the netlist.
   - Save the edited configuration file in a different location, such as the allegro directory for the current project, or give it a different name in the default location. The point is not to overwrite the supplied file (even if you have permission).
   - Still in the Setup dialog box, use the '...' button to select the edited configuration file.

6. Run the netlister, wait for PCB Editor to open the board and place the components as usual. SSNAME is not yet visible.

7. Choose Display > Property... from the menu bar and select the Graphics tab. Scroll down the list of Available Properties and click on our added property, whose name has probably changed to Ssname. SSNAME will appear under Selected Properties. You will probably want to increase the Text block from its default of 1, which is tiny. There is a drop-down list for Subclass but it contains only the single entry PROPERTIES, which is part of the Manufacturing class. Click Create and the SSNAME text will appear on the drawing. It can be moved and rotated in the usual way.

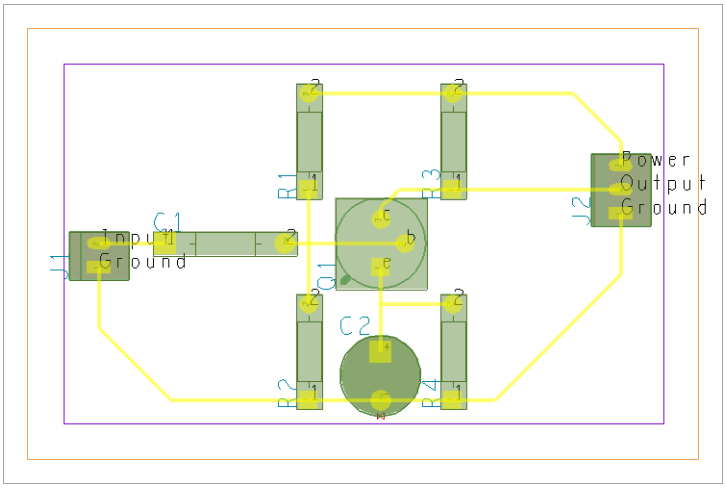

Figure 27. Board for one-transistor amplifier with the names of all pins transferred from Capture.

Whew! A slightly simpler alternative is to use Name, which is a standard property of a pin. Follow exactly the same procedure except that you do not need to define the new property. Curiously, you must still select Allow User Defined Property even though it was not defined by the user. The snag is that the name is now shown for *every* pin, which can clutter the board – see figure 27.

B.8 Miscellaneous PCB Editor tips

- There seems to be no Unroute Board command within PCB Editor, which would be helpful if you made a complete mess of routing. One method is to reload the design, assuming that you saved it first. Alternatively, try this.

  1. Open the Find control panel and select Nets only.
  2. Drag across the design to select all the nets.
  3. All the nets are now highlighted in the main window. Right-click and choose Ripup etch.

- I haven't described how to produce Gerber files and the like, which require the Manufacture menu of PCB Editor. This will depend on the demands of the company involved. See *Preparing Manufacturing Data*.

- It should be possible to set up colour files that make it simpler to produce photomasks. I haven't yet got this to work reliably. The colorview commands are described in *C Commands*.

- I haven't explained how to add mechanical features such as mounting holes, which ought to be remedied. These can be placed by selecting Place > Manually. . . and choosing Mechanical symbols from the drop-down list. Click the Advanced Settings tab and choose Library because these symbols are not in the database imported from Capture. See the section on *Adding mounting holes* in *OrCAD Flow Tutorial*.

- Our local allegro library doesn't yet include mechanical symbols. There is another problem with the electrical symbols too: the values have vanished. The padstacks have proliferated into a mess too. The main references for this job are *Defining and Developing Libraries* and *Preparing the Layout*. Issues with importing from Capture are covered in *Preparing your design for use with PCB Editor* in the *Capture User's Guide*. The conversion of libraries from Layout is described under the orcad in command in *O Commands*.

- It would be convenient if the schematic circuit could be drawn once with both 'virtual components' such as sources for simulation and sockets for the real PCB. Unfortunately this cannot be done without editing the components in the pspice library because some have pins numbered 0, which allegro rejects. Many of the libraries are full of bugs. Some components have pins 'numbered' with letters (such as the electrolytic capacitor) and some aren't numbered at all. Avoid the libraries in oldlibs, which seems obvious but students find them attractive.

- I find it helpful to adjust the grids produced by the new board wizard, which are the same for everything. Choose Setup > Grids... from the menu bar and change the Spacing figures for Non-Etch (essentially the components) to 100. Leave the remaining spacings at 25.

- Lines in the ratsnest are 'jogged' by default. I prefer to join the components with straight lines instead. Choose Setup > Design Parameters... from the menu to bring up the Design Parameter Editor. Select the Display tab and adjust the Ratsnest geometry to Straight.

- There are two types of 'design' file that both use the extension .dsn, but whose contents are entirely different.

  - Capture has a design file to hold its database (Windows calls it a Data Source Name)
  - PCB Editor uses a design file to export the board to the autorouter.

  Don't let them get mixed up! This is one of the reasons for setting up a separate allegro subdirectory.

- In section 5.3 on page 20 I advised students to place their components on the board roughly in position using the Placement dialogue box, then rearrange and reorient them later. I think this is the simplest approach but you can also rotate and mirror components using the contextual menu while the Placement dialogue box is open. Curiously the command for rotation becomes Rotate rather than Spin.

- There is a high chance of error if you copy names of footprints from a document and type them manually: It is better practice to select them from a library. This is a bit clumsy in PCB Editor. (Perhaps there is a better way that I have yet to discover because this worked much better in Layout. A listing of the directory might be easier.)

  1. Choose Place > Manually... from the menu bar.
  2. Click the Advanced Settings tab and choose to Display definitions from Library.

3. Return to the Placement List and select Package symbols from the drop-down list. You will now see a list of all packages in the libraries.
4. Scroll down to find the outline that you want, RC400 for example. Click in the check box next to the component and a graphic appears in the Quickview window. This helps you to confirm that it is the correct outline, although there is no scale.
5. Select the Text radio button and the name of the component appears. You can copy this and paste it into the Properties Editor in Capture.
6. Dismiss the Placement box with Cancel when you have finished and quit from PCB Editor without saving any changes.

B.9 SPECCTRA tips

- Tracks can be edited in SPECCTRA instead of PCB Editor. This is handy for moving badly-placed vias (I found it easier than PCB Editor). Right-click in the window, which brings up the INTERACTIVE ROUTING MENU. Move mode is probably the most useful. You can then select tracks or vias and move them. This is best done before the finishing touches of spreading and mitring. In fact you can do most of the placement in SPECCTRA as well as the routing but I didn't want to describe yet another interface.

- If you export a fully or partly routed board from PCB Editor to SPECCTRA, the imported tracks are protected against changes in SPECCTRA. Choose Edit > [Un]protect > Wires by Net... (or Wires by Layer List...) to remove the protection. You can then unroute these tracks and reroute the board.