A basic introduction to

Cadence OrCAD PCB Designer

Version 16.3

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Preamble

This document introduces the basic features of OrCAD PCB Designer. It is aimed primarily at novices with limited experience of construction who have never designed a PCB before. For this reason I concentrate on pin-through-hole devices (although surface-mount devices are no more difficult) on single and double-sided boards. I strongly recommend Mitzner's book [1] instead if you are an experienced designer, interested in more advanced PCBs for commercial production.

Other readers may be experienced users of OrCAD Layout who are obliged to switch to PCB Editor; I hope that they don't feel that their intelligence is insulted! I've highlighted some of the most significant differences between Layout and PCB Editor. (I think that PCB Designer refers to the complete suite while PCB Editor is the specific application for editing PCBs but it's not entirely clear.)

I adapted this document from an introductory class and have removed several features that are unlikely to be of interest to most readers. For example, we have developed a local library of footprints for PCBs constructed by students. The pads are enlarged to allow easy soldering and the symbols contain features to discourage common design errors, such as tracks to inaccessible pads underneath connectors. However, I've retained the instructions to produce photomasks directly with the Plot command, rather than with Gerber files. This is helpful if you make PCBs in-house by traditional processes, which is often the case for student projects.

Differences between versions 16.0, 16.2 and 16.3

Version 16.3 of OrCAD was released in late 2009, following 16.2 in late 2008. The *What's New* document exceeds 90 pages but most of the changes aren't relevant to an introductory tutorial. Here are the most important new features in version 16.2.

- The appearance of Capture has been updated to match PCB Editor. Buttons are now larger and their purpose is sometimes clearer. A bar of tabs can be used to switch between windows.
- Cross-probing between Capture and PCB Editor has been improved.
- The Plot command can leave drill holes open, which may be helpful for PCBs drilled by hand.
- The software is installed in the same way, regardless of whether you have a licence or not. Applications simply run in demonstration mode if they cannot find a licence. The demo version is a great improvement on previous editions but the installer has a peculiarity: you are forced to specify a licence server even if you wish to use only the demo mode. A bogus server such as 5280@localhost should get around this problem.

This tutorial is affected less by changes from 16.2 to 16.3.

- A board can now be 'flipped' (viewed from underneath rather than from the top) and rotated in 3D but this is of limited value for the simple designs described here.
- Jumpers have been added to assist the design of single-sided boards.

- The autorouter is now called Allegro (or OrCAD) PCB Router rather than SPECCTRA.

Board files written by version 16.3 of PCB Editor cannot be read by version 16.2, nor can those written by 16.2 be read by version 16.0. (This contradicts the statement in *Getting Started with Physical Design* that 'Allegro PCB Editor databases are backward-compatible with their major version number (the number to the left of the dot)'.) Use the menu item File > Export > Save design to 16.2... (or 16.01...) to write a file compatible with an earlier version. (The jargon is to *downrev* the design.) I have not yet updated this document for version 16.5.

Prospectus

This document falls into two major parts.

- The main body is a tutorial that guides you through the layout of two simple PCBs. First is a one-transistor amplifier, which is really straightforward but allows you to concentrate on the interface of the applications. The second design is an instrumentation amplifier, which is laid out on single and double-sided PCBs using the autorouter. I also show how to produce manufacturing data for this design.
- The appendices contain a collection of techniques that you might find useful. Links to these are given in the tutorials.

PCB Editor has so many features, even in its OrCAD version, that I cover only a small fraction of them.

1 Introduction

The Cadence OrCAD PCB Designer suite comprises three main applications.

- **Capture** is used to draw the circuit on the screen (schematic capture). A *netlist*, which describes the components and their interconnections, is the link to PSpice and PCB Editor.
- **PSpice** simulates a captured circuit. I do not describe PSpice in this tutorial.
- **PCB Editor (Allegro)** is the application for laying out a printed circuit board. It includes an automatic router that works out the arrangement of tracks needed to connect the components on the PCB. The output from PCB Editor is a plot or a set of files that can be sent to a manufacturer.

The overall *design flow* for making a PCB is shown in figure 1 on the following page with a summary in section 7 on page 46.

PCB Editor replaces the earlier application, Layout, which is now discontinued. OrCAD PCB Designer is the most basic version of Cadence's Allegro suite for PCB design and much of the documentation refers to 'Allegro' rather than 'PCB Editor'.

Fixup. The libraries for Capture and PCB Editor have some incompatibilities that must be corrected by *Fixups*. I hope to find smoother ways around these difficulties in the future. ❦

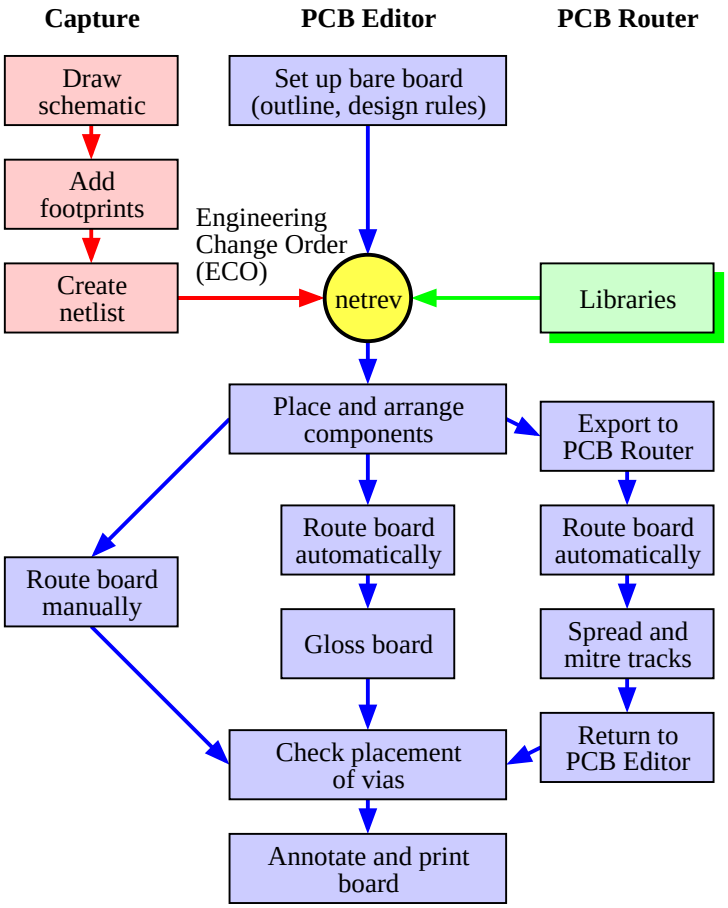


Figure 1. Design flow for making a PCB with Capture and PCB Editor. The three paths for PCB Editor depend on whether the tracks are drawn manually (as in the first design), automatically within PCB Editor, or by running the autorouter as a separate application.

1.1 Libraries, files, directories and design rules

Three types of information are needed for each component, corresponding to the three main applications listed above.

- **Electrical symbols** are used to draw the circuit in Capture.
- **Electrical models** allow you to simulate the circuit in PSpice.
- **Footprints** or **package symbols** show the physical size and shapes of the pads (where the pins are soldered to the board) and the outline of the package. They are used to lay out the circuit in PCB Editor.

These are stored in different sets of libraries and you must select the files needed for a particular design. Footprints are needed as well as electrical symbols because components with the same electrical behaviour come in different packages. For example, an integrated circuit might come in two versions:

- a traditional, plastic dual-in-line package (PDIP) with pins 0.1″ apart

- a smaller, surface-mount device (SMD) with pins only 0.5 mm apart, if it has pins at all

The opposite is also true: resistors of a particular shape come in a wide range of values.

Further information is needed to describe the characteristics of the printed circuit board on which the components are mounted. The details are important for high-speed designs but we need to know only the number of layers of copper, called *etch* in PCB Designer. This tutorial covers only single-sided boards, which have components on top and copper on the bottom, and double-sided boards, which have copper on both surfaces but usually components only on the top. Fancier boards often have two internal planes of copper used for power and ground; complex designs need further layers.

Design rules are required to lay out the circuit on the PCB. The full details are complex but the basic rules specify the minimum width of tracks and the gap between them. Manufacturers often express these numbers in the format 10/8, meaning minimum widths of 10 for tracks and 8 for gaps (although the numbers are usually the same). The units are almost always *mils*, which mean thousands of an inch; see section 2.5 on page 10. I use 25/25 rules in this tutorial, which are extremely coarse but produce boards that are easy for inexperienced students to solder.

Further design rules control a diverse range of features, such as the spacing between tracks and pads, whether vias are permitted and the impedance of tracks (they act like transmission lines at high frequency). These rules are adjusted with the *Constraint Manager*, which we'll encounter in section 4.4 on page 29.

Fixup. Older versions of OrCAD prefer designs to be stored in OrCAD_Data rather than My Documents and may reject filenames that contain spaces. If you get inexplicable errors about unexpected arguments or incomplete file names, try copying the design to OrCAD_Data and removing spaces from the names of all directories and files. ❦

1.2 Help!

All programs provide extensive online help. Appendix A on page 47 explains how to use the Cadence Help system and guides you around the major documents supplied with PCB Designer. Many commands in PCB Editor have names that are not obviously related to the corresponding item on the menus so I have pointed these out.

2 One-transistor amplifier: Schematic capture

The first design is a one-transistor amplifier. It has only a few components and will be laid out on a huge board to make the routing straightforward: The challenge is to learn the software. The initial step is to draw the circuit in Capture.

Capture treats each circuit design as a *project* and a project manager shows the logical relation between the files required. *It is essential to create a new directory for each project.* Strange errors can occur if you have more than one project in a directory, from which it seems impossible to recover. It also keeps your work organised. OrCAD creates a subdirectory for PSpice files and an allegro subdirectory for PCB files. You should know this by now but a reminder is never a bad idea: **Save your work frequently and take regular backups of important circuits.**

Note. I have wasted hours trying to reconstruct projects where students have not obeyed the rule of one project per directory! I don't know why they find it so difficult. ❦

Select Start > Programs > OrCAD 16.2 > OrCAD Capture. I use '>' throughout this document to show the levels of a hierarchical menu. There will be a short delay while the software is loaded and the licence server is accessed. Alternatively, you will be asked if you wish to use Demo mode if no licence can be found. The screen then shows the OrCAD Capture main window with a menu bar and various toolbars. A sub-window at the bottom shows the session log; its title may be hard to find if the window has been docked. Version 16.3 offers different ways of controlling the windows; right-click in a title bar.

2.1 Create a project

The first step in OrCAD is always to create a project.

1. Create a new directory in Windows to hold all files for the project.
2. Select File > New > Project from the menu bar of Capture.
3. In the New Project dialog box:
   - Select an Analog or Mixed A/D project if you wish to simulate the circuit. You could use the PC Board Wizard or Schematic options if you don't want to simulate the circuit, in which case the steps differ slightly from my description.
   - Click on the Browse key and navigate to the new directory that you created for this design. Click OK.
   - Give the project a meaningful name.
   - The path and directory now show in the location box (if you can see them – they are usually too long). Click OK in the New Project dialog box.
   - Click Next.
4. Select the Create a blank project button in the small dialog box that appears and click OK.
5. Your project will now be created. The Project Manager window at the top left shows the files associated with your design and the resources used, such as library files. Its title is the full pathname of your project, which is usually far too long to fit. Make the File tab active if necessary.
6. Expand the Design Resources folder in the project, then the design (called *./project-name*.dsn, where *project-name* is the name of your project), then the SCHEMATIC1 folder and finally double-click PAGE1 to open the schematic page for your design. Locate the Title box in the lower right-hand corner, double-click on the placeholders, which are in angle brackets <>, and replace them with a descriptive title and so on.

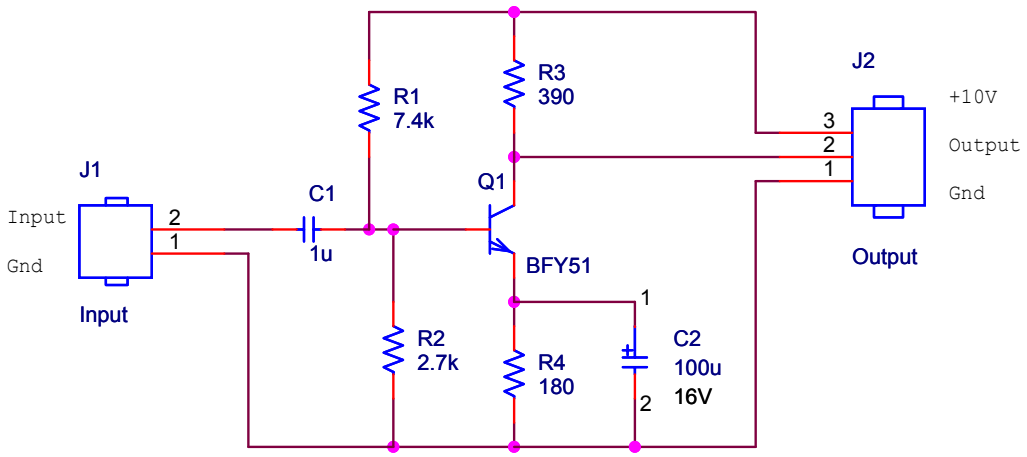


Figure 2. Schematic drawing of a simple, one-transistor amplifier. The pin numbers on the electrolytic capacitor are not normally visible but are shown to illustrate a fixup later.

2.2 Draw the circuit

Draw the circuit shown in figure 2. The names of the components are listed in table 1 on the following page; I've renamed some of them to make their functions clearer. I assume that you are familiar with Capture but here are a few tips to help.

Jargon: The label that identifies each component on the schematic drawing is called its *reference* or *refdes*, short for *reference designator*. For example, the transistor has refdes Q1. Each refdes must be unique: No other component can be called Q1. ❦

- I used libraries from the pspice folder so that the circuit could be simulated although I do not describe that here. Basic components like resistors are in the analog library. The connectors are in the connector library, which is in the directory one level above the pspice directory (OrCAD16.3/tools/capture/library/). Use Search if you can't guess where a component is located. You may need to do this for the transistor.

  If you have no intention of simulating the circuit you might prefer to use components from the discrete library instead of pspice/analog. This avoids a problem with the numbering of pins that will arise shortly.

- The capacitor C_2 is an *electrolytic* type, which must be installed with the correct polarity or it will explode. One of its plates on the schematic is therefore labelled with a + sign and must be connected to a positive voltage. (Its pin numbers are also shown because of a fixup later.) The parameter CMAX is the maximum working voltage of the capacitor, which is not needed for simulation but important when you pick out the real component. I set it to 16 V, which is a common value.

- Always join components with wires, not by placing them so close that their pins overlap. This can cause strange errors.

Table 1. Components, names in Capture and footprints for the one-transistor amplifier. These are taken from the library supplied with PCB Designer. The names are not case-sensitive.

Part	Capture name	Footprint name
Resistors	R	res400
Capacitor, non-polarised	C	cap600
Capacitor, electrolytic	C_elect	cap196
Connector, input	HEADER 2	jumper2
Connector, output and power	HEADER 3	jumper3
Transistor	BFY51	to5 (letter 'oh' not number zero)

- Wires and components sometimes become joined incorrectly if you move them about. Use Place > Junction or the junction tool from the toolbar on the right to eliminate spurious connections.
- Include connectors for all wires that leave the PCB. This includes inputs, outputs and the power supplies. It is a good idea to change the 'values' of connectors to make them more descriptive than the defaults, for example Input rather than HEADER 2. Do not edit the reference, such as J1.
- Add text to label the pins of each connector.

Print the drawing sheet: You will need this soon to guide the layout of your PCB. This circuit takes up only a small part of the page so it is a good idea to choose File > Print Area > Set and mark out a rectangle that includes only the part of the page that you wish to print. *Check the circuit carefully* – it is much easier to correct mistakes at this stage.

Note. The Place Part dialog box is a pop-out panel in version 16.3 and its appearance has been modified considerably from the traditional version. The functionality is unchanged. Click on the 'pin' icon in the title bar to fix it if you prefer.

Some students change the Reference (J1 or J2) of the connectors to Input or Output instead of changing the Value (HEADER 2 or HEADER 3). This upsets the netlister later. ❦

2.3 Preparation for PCB layout

The procedure to this point should be familiar if you have used Capture with PSpice. A few extra steps are needed to prepare the schematic for a PCB.

Fixup. The electrolytic capacitor C_elect in the pspice/analog library is incompatible with its footprint. The pins of the footprint are numbered 1, 2 but those of the capacitor are p, n. This means that the software cannot match the capacitor to its footprint. Edit the electrolytic capacitor and change the numbers of its pins to resolve this.

1. Select the electrolytic capacitor and choose Edit > Part from the menu bar. A window opens with an enlarged view of the capacitor.

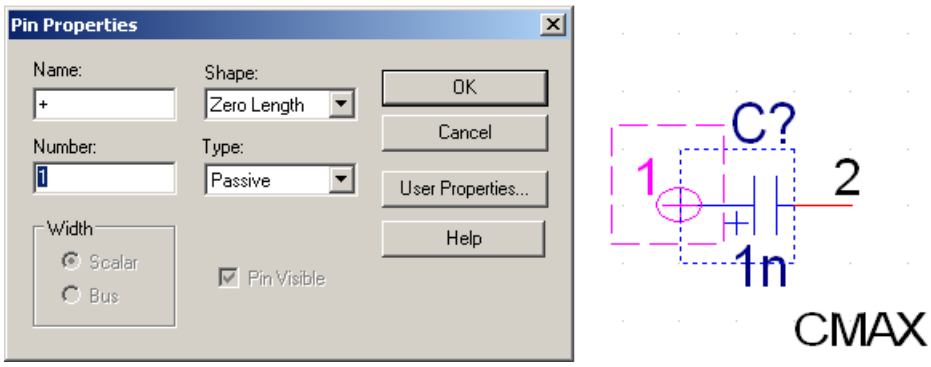


Figure 3. Edit Part window and Pin Properties dialogue box for correcting the numbering of the pins of the electrolytic capacitor.

2. The positive pin is shown as a circle on the left. Select it and and choose Edit > Properties.... This brings up the Pin Properties dialogue box, shown in figure 3.

3. Change the Number to 1 and click OK. Don't worry about the name of the pin.

4. The negative pin is shown as a red line on the right. Change its Number to 2.

5. Choose File > Close. You have the choice of updating this part alone, or all 'part instances' – that means all C_elect components in your design. There is only one so it doesn't matter whether you choose Update Current or Update All in this case.

I made the pin numbers visible for the electrolytic capacitor in figure 2 on page 7 as a reminder of this fixup. You need not do this. ❦

This problem can be avoided by using components from the discrete library instead, which is in the directory one level above the pspice directory. However, these components are not associated with pspice models and therefore cannot be used for simulation.

The main task in preparing the design for layout is to associate a *footprint* with each component. The footprint shows the physical outline of the components including the copper *pads* to which the pins are soldered. Most pads are either circular or oval except for pin 1, which has square corners to identify it. The components in many Capture libraries have footprints already but unfortunately they are mostly wrong. We must therefore enter the correct footprints, which are listed in table 1 on the previous page for this circuit. Don't muddle the letter 'o' with the numeral '0'. The whole business of assigning footprints is unnecessary if you have a database of components in Capture CIS.

1. Drag the cursor over your schematic drawing so that all the components are enclosed in a rectangle. Do not include the title box.

2. Choose Edit > Properties... from the menu bar, which brings up the Properties spreadsheet.

3. Type each name into the PCB Footprint field of the Properties spreadsheet. All the resistors have same footprint so use copy and paste for speed.

Faster methods of entering identical footprints are described in section B on page 50.

Tip for Layout users: PCB Designer comes with a small library of footprints compared with the extensive libraries that were provided with Layout. I've been told that this is because most users have their own libraries. Where there is a need, somebody will offer a service: Online libraries of footprints are available – for a fee.

PCB Editor has no convenient way of copying the names of footprints into Capture from a library, as in Layout. I describe a feeble substitute in section C.12 on page 64. PCB Editor also lacks anything like the library manager in Layout. ❦

2.4 Design rules check

The next step is a Design Rules Check to ensure that no errors have been introduced.

1. Click on the Project Manager window and highlight your design (with extension .dsn).
2. Select Tools > Design Rules Check... from the menu bar.
3. Under Design Rules select both Run Electrical Rules (probably selected already) and Run Physical Rules (probably not).
4. Click OK. A dialog box may report One or more errors or warnings were encountered. Do you wish to view the messages in the session log? Agree to this and review the report in the Session log window. No positive message is given to confirm that all rules have been passed successfully, just an absence of complaints. *Ask for help if you do not understand a message* – don't just ignore it.
5. Return to your drawing and correct any errors, shown by green circles (a strange choice of colour). Repeat until the Design Rules Check runs silently.
6. You may wish to run the Design Rules Check and select Action > Delete existing DRC markers to get rid of the green circles. They do not vanish by themselves.

2.5 Make a bare board in PCB Editor

The simplest way of creating a PCB is first to set up an empty PCB, then to add your components and connections to the board. This follows the design flow shown in figure 1 on page 4. See section C.2 on page 53 for a more conventional flow where you make the netlist before defining the board.

First create a directory allegro within your directory for the current project. PCB Editor likes to keep its files here. Choose Start > Programs > OrCAD 16.3 > OrCAD PCB Editor, which opens the OrCAD PCB Designer application (Cadence seem muddled about the name). I'll leave the details of the interface until later because we need only one dialogue box for this step.

Choose File > New... from the menu. In the first dialogue box, set the Drawing Type to Board (wizard). Click Browse..., navigate to your new allegro directory and give the board a name such as bare.brd. Click Open then OK to bring up the new board wizard. This takes you

through several screens to define the parameters of the PCB. Some of these are obvious, such as the size of the board, while others set up the *design rules* – the width of tracks on the PCB, how much space must be left between them, and so on.

1. The first screen is purely descriptive. Read it, then click Next >.

2. This asks for a board template. We don't have one so select No (probably the default) and click Next >.

3. You are next asked for a 'tech' file. This is short for a *technology* file, which specifies the design rules. Again we don't have one so select No and click Next >.

4. This asks for a board symbol. Select No again and click Next >.

5. We now reach the screens for the parameters that must be set up. The units should be Mils. These are not millimeters but the American term for thousandths of an inch; 1 mm $\approx$ 40 mils. All dimensions are given in these units so get used to them.

   Leave the drawing size at A. This is an American size but you aren't allowed European A4 if the units are mils. Leave the origin at the centre.

6. Set the grid spacing to be 100 mils.

   The Etch layer count is the number of copper layers on the board – the number of layers of tracks for signals and power. Leave this at 2, although we shall use only one layer in the first design.

   Select Generate default artwork films, which is the default.

7. Leave the names of the layers as Top and Bottom and their types as Routing Layer.

8. Enter 25 for the Minimum Line width (in mils). This value propagates into the other boxes. It means $0.025''$ or about 0.64 mm, which is very wide for a track nowadays but makes the board easy to solder by hand.

   For the Default via padstack, click on the button with ... and choose Via26. This design is far too simple to need vias, which carry a signal from one layer of the PCB to another, but they may be required later.

9. Rectangular board (it's curious that a circular board is the default).

10. Enter a width of 3000 and height of 2000 mils. This defines the board outline as $3'' \times 2''$. There is no corner cutoff.

    Specify the Route keepin distance as 100. A *keepin* means that objects must be kept inside the specified region. In this case it means that tracks cannot go any closer than 100 mils to the edge of the board. It gives a border around the PCB to aid handling and manufacture. (We'll encounter keepouts as well later.)

    Set the Package keepin distance to 250. Components must be placed within this keepin and therefore cannot be closer than 250 mils to the edge of the board. The gap between the two keepins allows you to run tracks around the outside of all the components, which is often helpful on a more complicated board (although hardly necessary here).

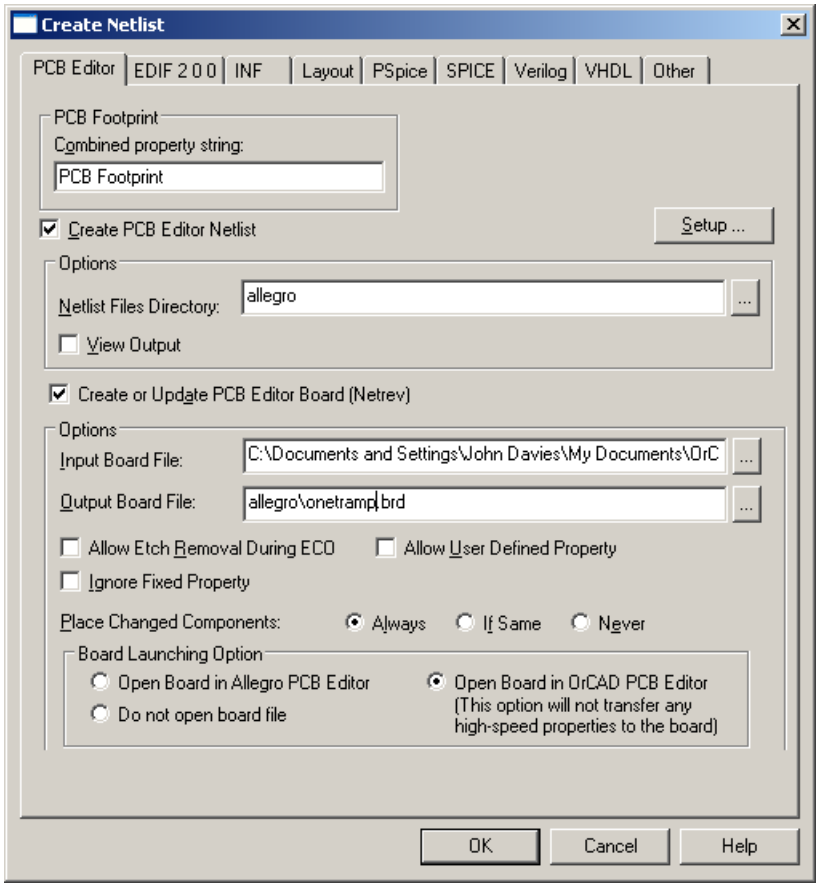


Figure 4. Completed dialogue box for netlisting the design and sending it to PCB Editor. Your file names will be different.

11. Click Finish – that's it.

This has set up the design rules and made an empty board, which you can see in the design window of PCB Editor, shown in figure 5 on page 15. Three rectangles are visible for the board outline, route keepin and package keepin. Choose File > Save and close PCB Editor.

The next step is to return to Capture and send the circuit to PCB Editor so that it can be added to the bare board.

Tip for Layout users: PCB Designer does not come with a library of technology files, as did Layout. Cadence expect you to have your own. Fortunately it is easy to export a tech file from a board file that you have set up to your liking; see section C.4 on page 54. ❦

2.6 Create a netlist

The information about your design is sent from Capture to PCB Editor in the form of a *netlist*, which contains a description of the circuit and its components. (The netlist comprises three files but you rarely need to look at them.)

1. Highlight your design (the object whose name ends in .dsn) in the Project Manager window of Capture.

2. Select Tools > Create Netlist... from the menu bar, which brings up the dialogue box in figure 4 on the preceding page. Make sure that the PCB Editor tab is active.

3. Confirm that the PCB Footprint box contains PCB Footprint and that the box underneath for Create PCB Editor Netlist is selected.

4. Under Options, the Netlist Files Directory should be shown as allegro. Select Create or Update PCB Editor Board (Netrev). *Netrev* is the application that merges the netlist, footprints and other information into the database used by PCB Editor, hence its central position in figure 1 on page 4.

5. For Input Board File, choose the bare board that you have just set up. Click on the '...' button to navigate.

6. The Output Board File usually shows something sensible automatically; edit it if not. It should use the new allegro directory.

7. Under Board Launching Option, select Open Board in OrCAD PCB Editor if your licence doesn't cover the full version of Allegro.

8. The entries in the dialogue box should now resemble figure 4 on the preceding page except except for the pathnames. Click OK to dismiss this dialog box and start the netlister.

You are warned that your design will be saved by Capture, then a Progress box shows the various processes needed: Netlisting the design followed by Updating OrCAD PCB Editor Board. PCB Editor is then launched with your new board.

- You may see a Warning box, which tells you that Netrev succeeded with warnings. Check the Session Log if this happens. Messages about RVMAX and CMAX can be ignored; these are maximum voltage ratings of the components and are not important for this circuit. *Pay attention to any others!*

- OrCAD PCB Editor gives you a warning that Database was last saved by a higher tier tool, which you can ignore.

You should now see your empty board outline on the screen of PCB Editor again; the components have been added to the database but are not yet visible.

Note. *The netlister in some versions of 16.x has a nasty bug (the pxllite bug).* The symptoms are that the Netlist Files Directory does not show as allegro automatically in figure 4 on the previous page and that nothing happens when you run the netlister – not even an error message. Netlisting for PCB Editor must be performed once on each computer by a user with administrator privileges before it will work for anybody else.

PCB Editor is almost always launched even if there was a fatal error during netlisting: It is vital to check the session log. Many students don't bother, and discover only later that components are missing.

Check the search paths if PCB Editor complains that it can't find components. This shouldn't occur if you use the standard libraries but may arise with local libraries. Choose Setup > User Preferences... from the menu bar, which brings up the User Preferences Editor, then look at Design_paths in the list of Categories. ❦

Tip for Layout users: This process is similar to creating a netlist in Layout – it just uses a different tab in the Create Netlist dialogue box.

Where are my components? Layout automatically displays the components on screen, ready for you to move on the PCB. Allegro does not do this: You must place them yourself. The Quickplace command, which I'll describe in section 4.2 on page 28, achieves the same effect as Layout. ❦

3 OrCAD PCB Editor

The interface of PCB Editor may feel unfamiliar because the application was originally developed for unix and has been ported to Windows with minimal changes. Some distinctive features are obvious almost immediately.

- The design window, which shows your board, has no scroll bars.
- One design is always open; you cannot open more than one, nor close the current design without opening a new one or exiting the application.
- There is no 'null' tool, such as the pointer shown by most drawing applications when no other tool is selected.

An important aspect of the interface is that tools can be used in two ways.

- First choose a command, either from the menu bar or by clicking a button, then the element of the design on which the tool should operate.
- Select the object first, then the command from the contextual menu by right-clicking.

I shall use both methods in the tutorials, picking whichever seems most natural at the time. However, confusion can arise when you change from one method to the other. It is therefore a good idea when switching to disable any active tool (right-click and choose Done if it is offered) and clear any selection (left-click outside the board or right-click and choose Selection Set > Clear All Selections). See section C.1 on page 51 for a fuller description of the user interface.

3.1 The screen

PCB Editor needs a big screen – the elderly laptop that I have used to illustrate these instructions is not large enough to show all the toolbars! The main elements of the application are shown in figure 5 on the following page.

- **Design window**, occupying most of the screen, where you lay out the PCB. It always shows the board viewed from the top; the bottom layer is seen through the board as if it were transparent.

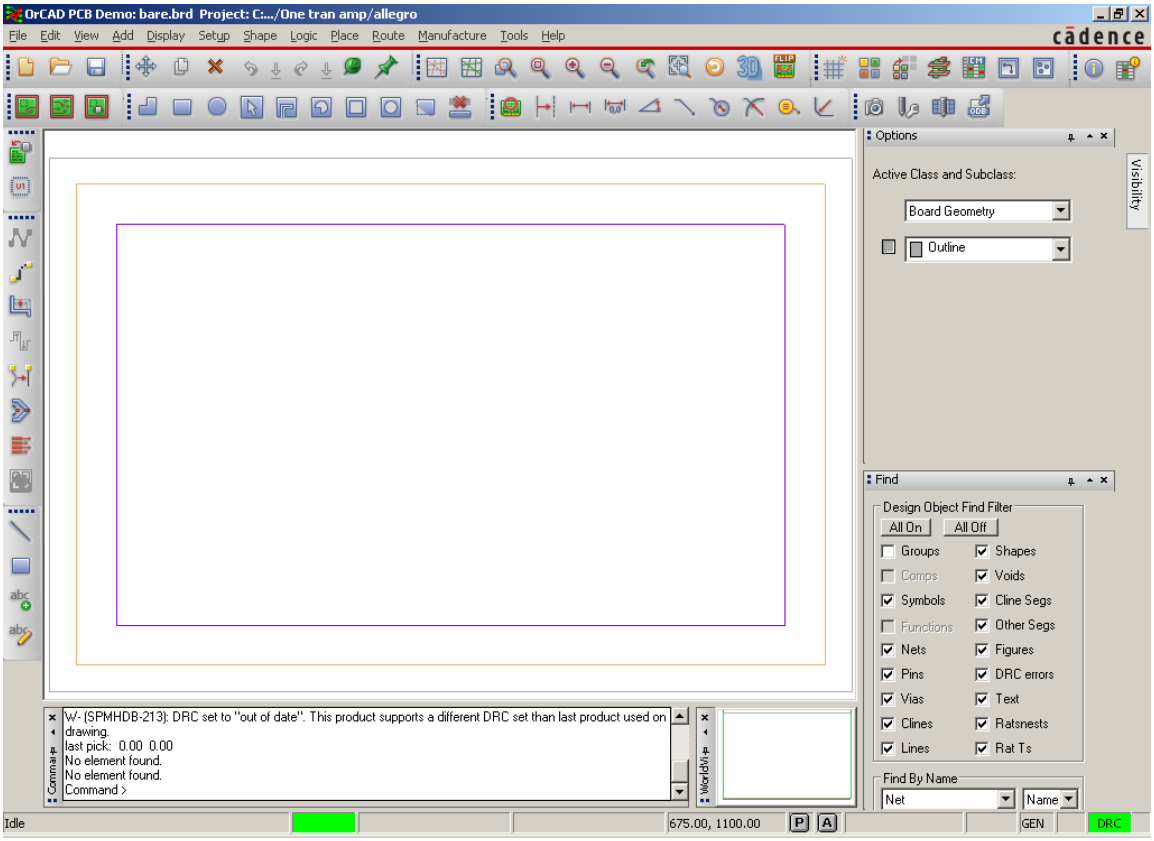


Figure 5. Screenshot of OrCAD PCB Editor with an empty board; the black background has been changed to white for a clearer printout. The rectangles show the board outline (outer), route keepin and package keepin (inner). The Find and Options control panels have been pinned open on the right.

- **Menu bar** along the top as usual.
- **Toolbars** in two rows under the menu bar and a further column down the left-hand side. Their arrangement depends on the size of the screen. Hover the pointer over a button to reveal its function.
- **Control panels** with tabs on the right-hand side. Each panel pops out when you move the pointer over its tab. Click the pin to lock a panel open.
  - Find selects the type of object that is highlighted when you move the mouse around the drawing.
  - Options changes according to the current mode and command; it selects the active class and subclass when PCB Editor is idle, then offers appropriate options when a command is chosen.
  - Visibility hides layers of etch while routing the board; predefined settings select the films of artwork that will be used to manufacture the PCB.

  I strongly recommend that you keep the Find and Options panels pinned open as in figure 5; Visibility is less useful in boards with only one or two layers of etch.

- **Command console window** at the bottom left of the screen. This prints a running log of your actions and is useful to show when Allegro is waiting for input from you. It also displays the output from commands such as Design Rules Check.
- **Worldview window** at bottom right shows how the relation between the board outline and the view in the design window. It is useful for moving the design window around the board as we shall soon see.
- **Status bar** at the bottom of the screen. It shows the coordinates of the pointer (crosshairs). The P (Pick) button is useful for typing coordinates instead of clicking with the mouse if your hand is unsteady.

  At the far right is a coloured block called DRC, which stands for Design Rules Check. It may be yellow because checking is not up to date. Usually it should be green to show that automatic checking is turned on and that no errors are detected.

A lot of jargon is associated with Allegro. It often refers to your design as the *database*, because that's what it is from the point of view of the computer. The various elements of the design are classified into *classes* and *subclasses*, which I'll write as class/subclass in the instructions. Here are some common examples.

- The **Etch** class includes the regions of copper that act as pads for the components and the tracks that carry the signals between them. The simple designs described here have two subclasses of etch, **Top** and **Bottom**. They are coloured green and yellow respectively by default.
- The **Board Geometry** class includes the **Outline**, which we have already seen. Subclasses **Silkscreen_Bottom** and **Silkscreen_Top** are used for text to annotate the board.
- We have also seen the **Package Keepin** class, used to prevent components being placed too close to the edge of the board. It has no subclasses.

The class and subclass can be chosen in the Options control panel but PCB Editor usually selects them automatically when you make a tool active.

Tip for Layout users: The colours used by PCB Editor are different from those used by Layout but can be changed if you wish with the Color Dialog, described in section 6.1 on page 39.

3.2 Moving around the design

Two methods can be used to *pan* or *roam* around the design – move the display to the region of interest.

- Use the arrow keys on the keyboard.
- Hold down the middle button of the mouse and drag. A confusing feature of this is that *it drags the window over the design*. This means that the design moves in the *opposite* direction to your drag. It is the reverse of the hand 'grabber' in applications such as Acrobat, which drag the design under the window.

  But I have only a two-button mouse! Many two-button mice have a scroll wheel, which acts as the middle button when pressed.

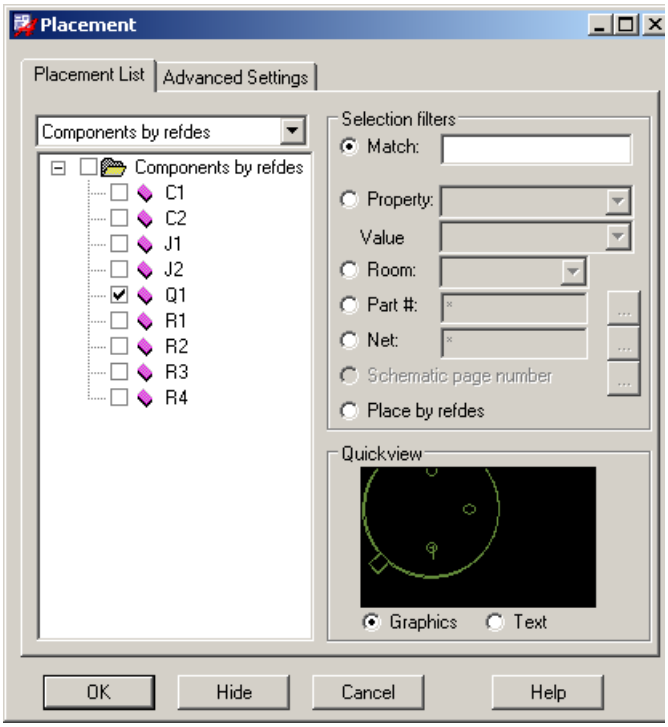


Figure 6. The Placement dialogue box, showing the components for the one-transistor amplifier. Transistor Q1 is ready to be placed on the board.

You also need to *zoom* into the design to concentrate on small details or zoom out to review the complete layout. Again there are two methods.

- Use the commands under the View menu or the corresponding buttons and shortcuts. Zoom Fit fills the window with your complete design, which is often helpful.
- The scroll wheel of the mouse zooms in and out, centred on the current position of the pointer.

The WorldView window can also be used to zoom and pan. If you drag a rectangle here, that becomes the area shown in the design window.

I could write a lot more about the interface (look at section C.1 on page 51 if you want to know) but it is more fun to place the components and route the PCB.

3.3 Place and arrange the components

Choose Place > Manually... from the menu bar to start placing the components. This brings up the Placement dialogue box shown in figure 6. The Placement List tab should be active and the list should show Components by refdes with the components in your design listed below.

Allegro can place components automatically (not in the OrCAD version) but it is straightforward to place them manually for this simple design. See figure 7 on the following page for guidance.

1. Start with the transistor. Click the box next to Q1 in the Placement dialogue. Its outline appears in the Quickview box (assuming that Graphics has been chosen).

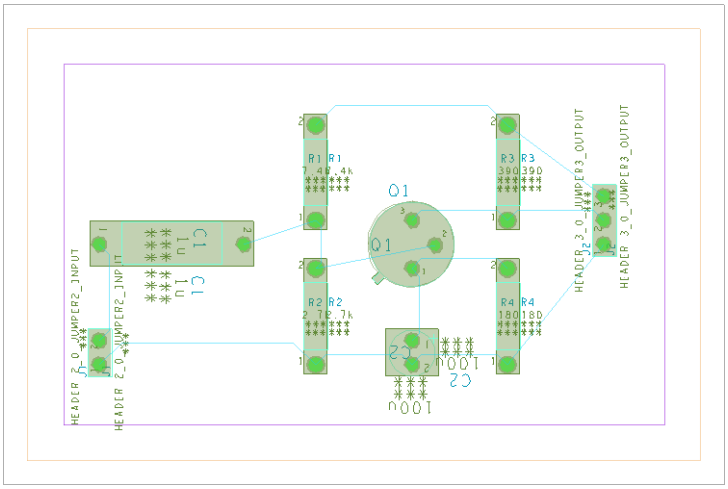


Figure 7. Screenshot of the board for the simple, one-transistor amplifier after all components have been placed and arranged. Cyan lines of the ratsnest show the connections between components.

2. Move the cursor out of the Placement box on to your design. The outline of the transistor follows the cursor. Left-click to place it centrally on your board. The outline fills in and a small P for 'placed' appears in the Placement box next to the refdes.

3. Place the connectors for input and output next. Select the boxes for both J1 and J2. Move the mouse onto the design and a two-pin header for J1 appears on the cursor. Click somewhere near the left-hand side to place it. Don't worry about its orientation for now.

4. The outline of J2 now appears automatically on the cursor. Place this on the right-hand side.

5. Next place the four resistors. Put them in the same positions relative to the transistor that they have on your schematic drawing. This makes the circuit easier to wire. Refer to your schematic drawing to identify each resistor.

   Keep all components inside the inner purple rectangle, which shows the Package Keepin. It turns green if you try to place any part of a component outside it.

6. Place the two capacitors in the same way. This completes the placement so dismiss the dialogue box.

Note. Components can be selected in Capture for placement in PCB Editor while the Placement dialogue box is open. See section C.3 on page 53.

If components are missing, there was probably an error during netlisting. Go back and check the session log in Capture.

*Why am I seeing the text double? – and why all the ***?* See section C.10 on page 60, which explains the purpose of the text and how to get rid of the surplus. ❦

The components are joined by a set of cyan lines called the *ratsnest* to show their logical connections. These lines will be turned into copper tracks when you *route* the board. The lines

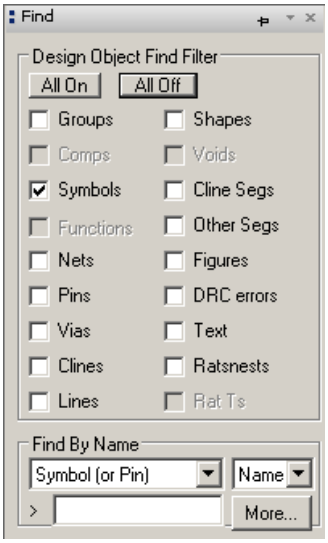


Figure 8. The Find control panel set up so that only symbols can be selected.

of the ratsnest simply take the shortest path between components and therefore cross other lines. Real tracks cannot do this. It is therefore vital to adjust the orientation and position of the placed components to reduce the number of crossings in the ratsnest and make routing easier.

Before doing this, experiment by moving the mouse around the design window without clicking. Elements of the design are highlighted and an explanatory note appears as the mouse passes over; there is no need to click on an object to highlight it as in many drawing programs. If you hover the cursor over the outline of the transistor, for example, the message Component Instance "Q1" is shown. The mouse may highlight the outline of a component, its pins, text or lines of the ratsnest. How can we be sure to move a *complete* component, not just a part of it? Moving a pin by itself would be a seriously bad idea, for example.

This is where the Find control panel is useful. Open it by moving the mouse over its tab if it is not pinned open already, click the All Off button, then select Symbols as in figure 8. Only complete symbols for components are now highlighted under the mouse. Individual pins are no longer selected, for instance. This makes it much easier to move and rotate components.

- The simplest way of moving a component is to left-click on it and drag, holding the mouse down.
- Alternatively, move the mouse over a component, right-click and choose Move from the contextual menu. Left-click in its final location.
- To rotate a component, right-click, choose Spin and move the mouse around to get the desired orientation.
- Both of these actions can also be chosen from the Edit menu and the toolbar has a Move button.
- Do *not* use the Mirror command, which is different from the commands with a similar name in Capture. Here it moves the component from the top to the bottom of the PCB.

The designs in this tutorial are not that ambitious. (It can be useful if you mix surface-mount and pin-through-hole components on a single-sided PCB.)

Move and rotate the components to simplify the ratsnest. This design is easy because no crossings are required if you follow the schematic drawing, which makes routing trivial.

Note. If some components have red outlines rather than the usual colour, and their text is in 'mirror writing', they have been mirrored and placed on the bottom of the board instead of the top. Select them and mirror them back to the top. ❦

When you have placed and arranged all the components, update the design rules check by choosing Tools > Update DRC from the menu bar. The DRC block near the bottom right of the window turns green and the Command window shows No DRC errors detected if everything is correct. If you have placed a component outside the keepin, for example, the message would be DRC done; 1 errors detected. The error is shown by a tiny red 'butterfly' marker on the design. Move the component inside the keepin and the marker disappears.

Tip for Layout users: PCB Editor lets you perform an action even if it leads to a DRC error, which it then marks. This contrasts with Layout, which forbids anything that would create an error. It's a different philosophy: PCB Editor assumes that you know what you are doing. ❦

Save your design with a new name for the populated board. Unusually, Allegro asks you if you wish to overwrite an existing file when you Save it. You may wish to save successive versions under different names in case you need to go back and repeat a step. Allegro does not save backups automatically.

3.4 Route the board

The electrical connections depicted by the ratsnest must now be replaced by copper tracks on the PCB. This procedure is called *routing* the board. The layers of copper are called *etch* in Allegro because of the usual manufacturing process. Tracks should be drawn on the bottom of the board with the components on the top (where they go by default). The wires from the components pass through the holes in the pads and are soldered to the tracks on the bottom of the board.

Jargon: *cline* is short for *connecting line*, a segment of a copper track. A plain line may show the edge of the board or the outline of a component and is not a conductor. ❦

Keep the layout of tracks as straightforward as possible – imagine that you are soldering the board yourself. Do not make life difficult by running tracks unnecessarily close to pads, for instance. You should aim for something like the layout shown in figure 9 on the following page but there is no need to follow this precisely.

Draw the tracks as follows. Before starting, check that no objects are selected (left-click outside the board or right-click and choose Selection Set > Clear All Selections) and that no tool is active (right-click and choose Done if it is offered). Pin the Find and Options control panels open, which makes it easier to control the tools.

1. Choose Route > Connect from the menu bar.

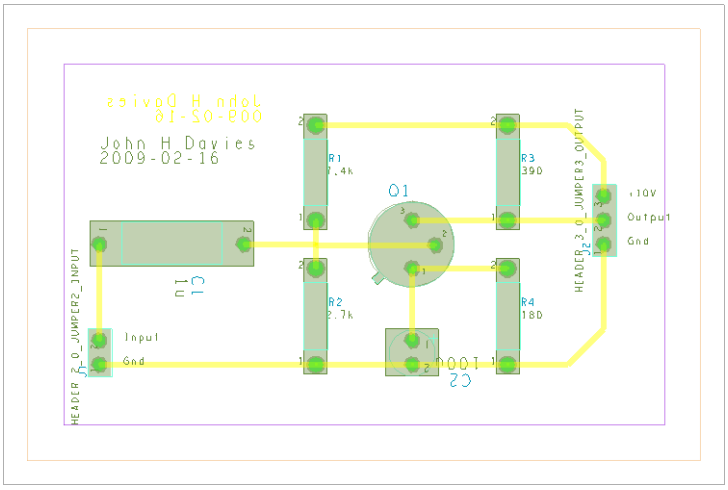
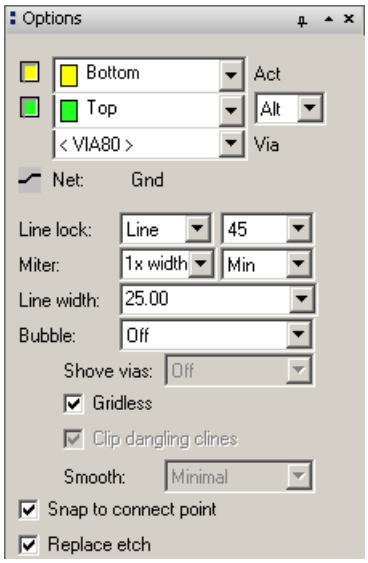
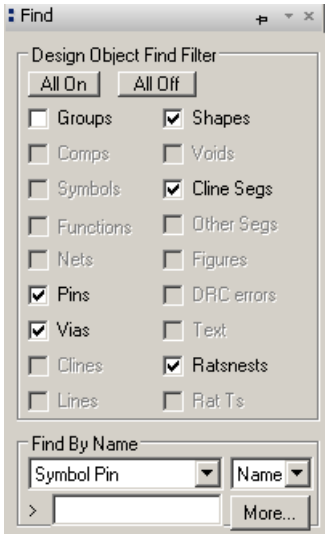


Figure 9. Screenshot of the routed board for the simple, one-transistor amplifier. The tracks are yellow, which shows that they are on the bottom of the board. Your screen may not match this image exactly because it depends on which classes are active at the time. I hid the surplus text on components as described in section C.10.

(a)



(b)



(c)

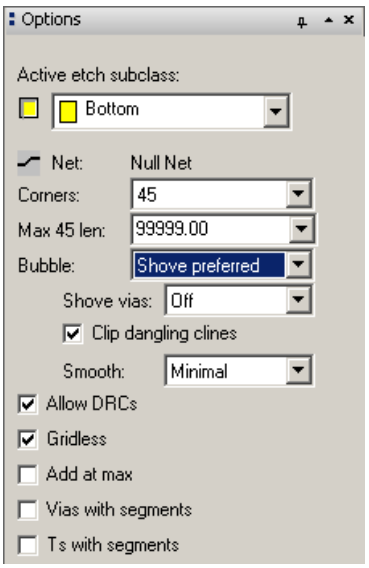


Figure 10. (a) Options and (b) Find control panels for the Add Connect command, and (c) Options for Slide.

2. The Options control panel changes to reflect the current activity and it now shows the layers available for routing. We want all the tracks to go on the bottom of the board so change the Act (active) layer to Bottom, which is painted yellow. You can also change the Alt (alternate) layer to Top, which is painted green, but we need only one layer for this circuit. Line lock should be 45 (degrees), which determines the allowed change in direction of a track. See figure 10(a) on the previous page.

   The Find control panel (figure 10(b)) is automatically configured to select the relevant objects for routing: pins, vias, shapes, cline segments and ratsnests. (*Shapes* are typically areas of etch, which is why they are active.)

3. Left-click on a pin to start routing a segment – the part of a track that runs from one pin to another. A segment of the ratsnest highlights to show that it is available for routing.

4. Move the mouse towards the pin at the other end of the highlighted ratsnest. A thick yellow line is drawn to show the copper track and replaces the line of the ratsnest.

5. Click at intermediate points to fix corners. These automatically turn through 45°, which is good practice. It is a bad idea to draw 90° corners because they are prone to breakage during etching.

6. Click on the destination pin to complete the track.

7. Repeat to route all segments of the ratsnest. Right-click and choose Done when you have finished.

Etch Edit mode provides a shortcut for adding connections. See section C.1 on page 51. Further tips for manual routing can be found in section C.6 on page 56.

Run a design rules check to detect any problems with routing. For further details, choose Display > Status... from the menu bar. The section on Symbols and nets should show that everything has been placed and routed, while DRC errors should be shown as Up To Date with no errors. Save your board.

Note. Some students put the tracks on the top instead of the bottom, in which case they appear green on the screen. Set the Find control panel for Nets, draw a rectangle around the board to select all the nets, right-click and change their layer to Bottom.

Another error is to draw tracks that don't match the ratsnest. Some students lay out the components incorrectly but draw the tracks to match figure 9. This causes a profusion of DRC errors.

A few students manage to draw tracks that bear no relation to the ratsnest at all and aren't even connected to pins. The underlying problem is usually that Pins are not active in the Find control panel. ❦

Oops! – I made a mistake

There are several ways of undoing an error.

- Right-click the mouse and choose Oops. This undoes the most recent partial action, such as drawing the last segment of a track.

- Right-click and choose Cancel, which undoes the last complete action.
- Try Edit > Undo to go further back.
- If you have made a complete mess, go to the menu File > Recent Designs and reload your design *without* saving changes (there is no Revert to Saved command). This abandons all changes since you last saved the file, which I hope was not too long ago. . . .

My tracks don't look very good: How can I improve them?

PCB Editor offers many ways of adjusting the tracks. First make sure that you are not still using the Connect tool by right-clicking and choosing Done if this appears on the contextual menu. Small adjustments to routed tracks can be made with the Route > Slide tool, which loads the Options control panel as shown in figure 10(c) on page 21. I suggest that you change Bubble from its default of Shove preferred, because this encourages Allegro to move tracks around in a startling manner; Hug only is more gentle. Click and release the mouse button on a segment to select it, slide it around and click again when you are satisfied with the result. Other helpful tools include Edit >Vertex and Edit > Delete Vertex.

For larger changes, you might wish to remove part of a track or the complete track and redraw it. Proceed as follows.

- Move the mouse over a cline segment, which should highlight. If it does not, open the Find control panel and choose All On.
- You can delete the etch at three levels using the contextual menu:
  - Delete removes the segment – a single straight line of track between corners or pins.
  - Connect Line > Delete removes the complete track (cline) between the two nearest pins or junctions.
  - Net > Ripup etch unroutes the complete net.
- Use Route > Connect to redraw the track.

This nicely illustrates the way in which PCB Editor allows a hierarchy of selections: just a segment, a complete line, or the whole net.

3.5 How to correct a layout if you spot an error in the circuit

It would be highly irritating if you had to repeat the whole layout after making a change to a circuit. The good news is that it is surprisingly easy to make corrections and that you already know the steps.

1. Save your board in its current state and quit from PCB Editor.
2. Re-open Capture and make the corrections to your circuit. Always run a DRC before proceeding.
3. Repeat the instructions in section 2.6 on page 12 for creating a netlist and sending it to PCB Editor with these small changes.

- For Input Board File, choose the board that you just saved in PCB Editor – the most recent version of your layout.
- Use a distinct name for the Output Board File to create a new board.

4. The new board opens in PCB Editor with the minimum number of changes to accommodate the revisions to your circuit. You must place any extra components and re-route any tracks that were disturbed.

The jargon is that Capture sends an *Engineering Change Order* (ECO) to PCB Editor.

More advanced techniques allow you to make changes to the circuit in PCB Editor. For example, you might wish to swap the two equivalent inputs to a logic gate to simplify the layout. Alternatively, you might wish to swap two identical gates or op-amps in a multiple package. Allegro offers the commands Place > Swap > Pins and Place > Swap > Functions to assist you. Such changes must be sent back to Capture to keep the design consistent. This is called *back annotation* and is explained in the manuals.

3.6 Add text

Next add some *silkscreen* text, which is printed on a commercial board using ink or paint. The outlines of components are often shown too. Each component automatically has its identifier (refdes) and value but it is helpful to add other text to make the board easy to fabricate and use. In particular, all connectors (headers) must have the function of each pin identified as on the schematic. Your name or that of the product would be useful too.

1. Start by putting your name on the board, which is always a good idea if you want to claim it. Choose Add > Text from the menu.

2. Open the Options control panel. You are probably getting the hang of the interface by now: choose a command, select options, then do it.

   - Text is normally placed in the silkscreen on top of the board so set the active class and subclass to Board Geometry/Silkscreen_Top.
   - However, for a home-made PCB without a silkscreen, you should put text such as your name on the bottom layer of copper because this is part of every board. The active class should therefore be Etch/Bottom. Text on the bottom of the board should be mirrored so that it reads correctly from below, so select the Mirror box.
   - Text block is a confusing way of specifying the size of text. A larger number for the block produces larger text. Something like 4 is about right for your name.

3. Click in the design where you would like the text to begin and type. Hit Return (Enter) to get a new line. Right-click and choose Done when you have finished or click to begin a new block of text elsewhere.

4. Add text on top of the board to identify the connectors. Put it in Silkscreen_Top if a silkscreen is available, Etch/Top if not. Reduce the size to text block 2. Do not mirror this text. Keep the text away from the pads if you use etch: It is printed in copper and could cause a short circuit.

Write labels for Input and Ground near the input connector and Power, Output and Ground by the output connector. (It is more reliable but tricky to transfer this information directly from Capture: See section C.9 on page 59.)

Congratulations! – you have finished your first PCB. Don't forget to save it.

3.7 Print the design

The simplest way of printing the design is to 'plot' it to a colour printer (the usage goes back to the days of pen plotters). Select File > Plot Setup... from the menu and choose the following settings.

- Usually the Plot scaling should be unity so that the size of the printout matches that of the PCB. This board is so simple that it is better to enlarge the drawing so enter 2 instead.
- Change the Default line weight to 10, otherwise the outlines are thin and indistinct.
- Select Auto center under Plot orientation.
- Set the Plot method to Color and close the dialogue box.

Open the Options control panel and set the active class to Etch/Bottom. This emphasizes the most important features. Now print your layout with File > Plot....

- Click on the Setup... button. Check that the paper size is correct and is in landscape orientation. Confirm also that the correct (colour) printer is selected.
- Choose OK to print your layout.

The result should resemble figure 9 on page 21 except that colours on the plot are opaque unlike those on the screen, which are partly transparent so that features underneath can be seen.

This plot is not useful for manufacturing the PCB. I'll explain the choices in section 6 on page 39 for a double-sided board, which shows the features more clearly.

4 Instrumentation amplifier – single-sided board

The second design is an *instrumentation amplifier* based on three op-amps, shown in figure 11 on the next page. In practice it is unlikely that the circuit would be built using three separate packages with single op-amps as in this design. Complete instrumentation amplifiers are available in 8-pin packages. Even if these were unsuitable, a quad package that contains four op-amps could be used although these lack the pins for trimming the offset voltage.

This design cannot be saved in the demonstration version of PCB Editor, which is limited to 10 components. Try omitting the decoupling capacitors, R_1 and R_3.

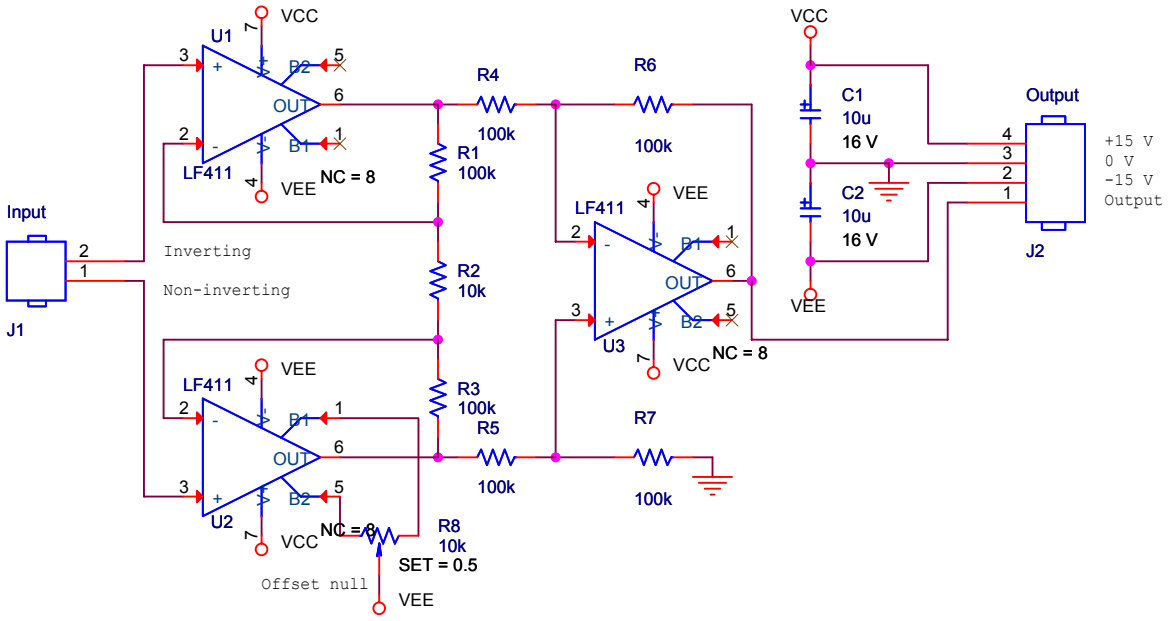


Figure 11. Instrumentation amplifier based on three op-amps. The label NC = 8 on the op-amps is not normally visible and will be explained later.

4.1 Schematic capture

Create a new directory for this design, as always, and start a new project in Capture. Place the components on the schematic but do not connect them yet. The only unfamiliar component should be the potentiometer, which is called POT – search for it.

Power supply rails are normally hidden to simplify schematic drawings. Here the power pins of the opamps are connected to named *power symbols*. Capture considers all power symbols with the same name to be connected together. Ground (earth) symbols work in the same way. (Often the power pins themselves are hidden and connected purely by name.) Connect the power supplies as follows.

1. Select Place > Power... or click the power symbol button on the toolbar and select VCC_CIRCLE from the CAPSYM library. Use the same symbol for both +15 V and −15 V supplies. Place one near each power pin, mirror it vertically if necessary and connect it to the pin with a short wire.

2. Double-click the name of each power symbol in turn and change the name to VCC for positive and VEE for negative supplies respectively. This is a standard usage (but there are many others). Check the orientation of the op-amps carefully! Some are mirrored vertically to make the circuit clearer and this reverses the power connections as well.

3. In the same way, select Place > Ground... or click the ground button. Use GND from CAPSYM for the ground (earth) symbols. These symbols must have the same name throughout your drawing or they will not be linked.

Wire the components and add text to identify the pins of the two connectors.

Table 2. Components and footprints for the instrumentation amplifier.

Part	Capture name	Footprint
Resistors	R	res400
Capacitor, electrolytic	C_elect	cap196
Connector, input	HEADER 2	jumper2
Connector, output and power	HEADER 4	jumper4
Op-amp	LF411	dip8_3
Potentiometer (trimmer)	POT	pot

Two of the op-amps have unconnected pins. These pins are intentionally unused because they are for offset adjustment and it is only necessary to do this on one op-amp. PCB Editor must be told about this, otherwise it assumes that you omitted the connections by mistake and flags an error. Show that the pins are deliberately unconnected by choosing Place > No Connect from the menu bar or clicking the appropriate button, then clicking on the pins. A small cross appears as in figure 11 on the preceding page. PCB Editor requires every pin to be connected or explicitly marked as not connected.

Next enter the footprints. Table 2 shows suitable choices from the Cadence library for the new components.

Fixup. Incompatibilities between Capture and PCB Editor must again be corrected before making the netlist. First, the pins of the electrolytic capacitors are wrongly numbered. Repeat the instructions in section 2.3 on page 8 to fix this. ❦

Fixup. A new problem is that only 7 pins are defined on the electrical symbols for the op-amps but the package has 8 pins. You might hope that the software would assume that undefined pins are not connected but it does not: It must be told this formally.

1. Select one of the op-amps and choose Edit > Part, which brings up the Part Editor.
2. Choose Options > Part Properties. . . , which brings up the list of User Properties.
3. Click the New. . . button. Give the new property the name NC, which stands for No Connect, and the value 8, which is the number of the unconnected pin. (Use a list separated by commas, such as 7,8, if more pins are not connected.)
4. Click OK to get rid of the dialog boxes and close the Part Editor. Choose Update All so that this change is applied to all LF411 parts in your design.

I have made the NC property visible on the schematic in figure 11 on the previous page, which therefore shows NC = 8, but you would probably not do this in practice. ❦

Run a Design Rules Check and correct any errors. Print your schematic when it has been completed and survived the DRC.

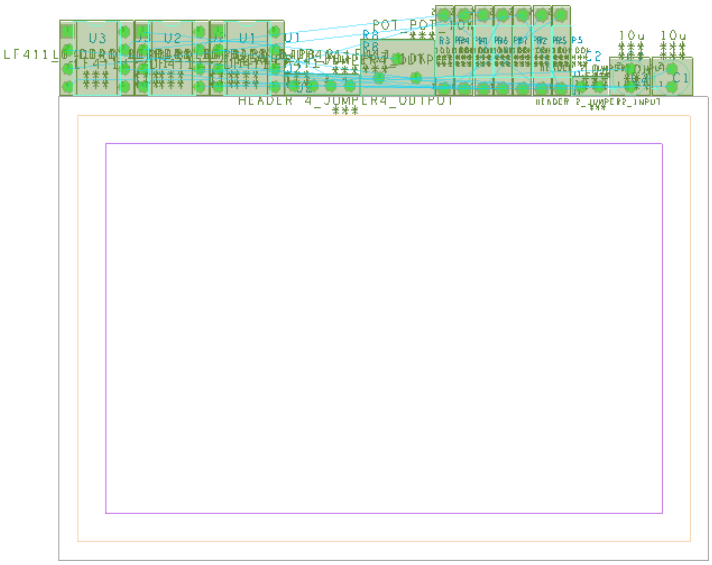


Figure 12. Quickplaced components for instrumentation amplifier just above board outline.

4.2 Create the PCB and place the components

Remember to make an allegro directory first. Set up the board as before (section 2.5 on page 10) but make it $3.5'' \times 2.5''$, which gives you plenty of room for the larger number of components. Save the board and quit from PCB Editor. Back in Capture, create a netlist and send the design to PCB Editor as before. Check the Session Log: Ignore any warnings about RVMAX but investigate any others.

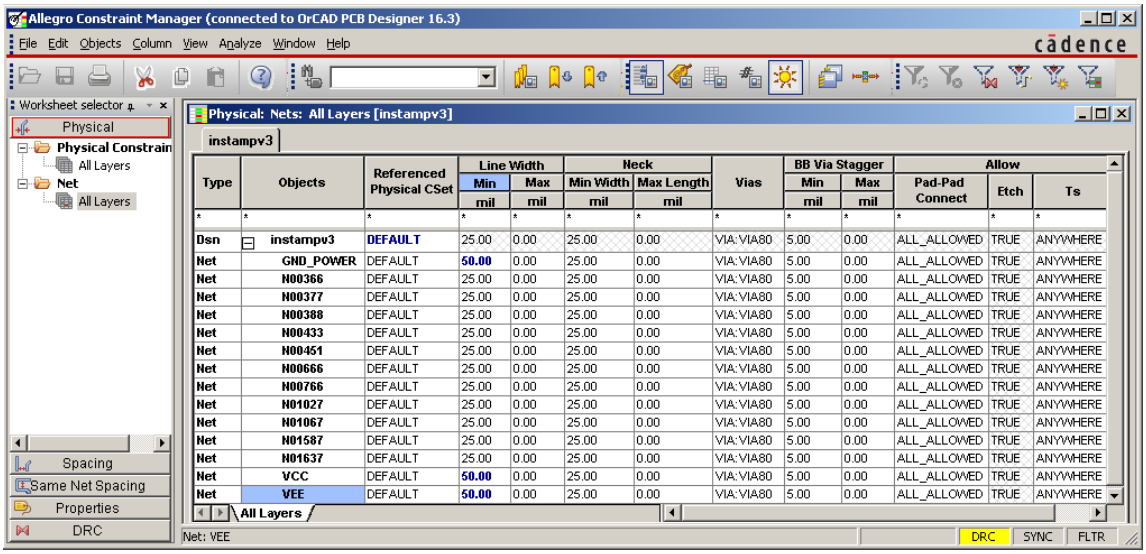
We'll place the components using a different technique this time. Choose Place > Quickplace... from the menu bar. The defaults should be suitable (Place all components, Around package keepin, Top). Click Place then OK. Your components are now arranged at the top of the board as shown in figure 12, ready for you to move them into position. (OrCAD Layout did this automatically.)

Move the components onto the board, arrange them to resemble the schematic drawing and adjust them to make the ratsnest simple with as few crossings as possible (it is not possible to eliminate all of the crossings). *This step is really important.* It is easy to route the tracks on a well-placed board; conversely, a poorly-placed board needs long, convoluted tracks or may even be unroutable.

Run a Design Rules Check when the components have all been placed and save your board.

Note. Some students complain that Quickplace has not placed their components. The usual problem is that the screen has been zoomed to fit the board but the components are above the board and therefore out of sight!

Sometimes PCB Editor hides the ratsnests for the power and ground nets; it depends on how the nets were configured in Capture. See section C.5 on page 55 to restore them. ❦



Type	Objects	Referenced Physical CSet	Line Width Min mil	Line Width Max mil	Neck Min Width mil	Neck Max Length mil	Vias	BB Via Stagger Min mil	BB Via Stagger Max mil	Allow Pad-Pad Connect	Allow Etch	Allow Ts
*	*	*	*	*	*	*	*	*	*	*	*	*
Dsn	instampv3	DEFAULT	25.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	GND_POWER	DEFAULT	50.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	N00366	DEFAULT	25.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	N00377	DEFAULT	25.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	N00388	DEFAULT	25.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	N00433	DEFAULT	25.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	N00451	DEFAULT	25.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	N00666	DEFAULT	25.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	N00766	DEFAULT	25.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	N01027	DEFAULT	25.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	N01067	DEFAULT	25.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	N01587	DEFAULT	25.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	N01637	DEFAULT	25.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	VCC	DEFAULT	50.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE
Net	VEE	DEFAULT	50.00	0.00	25.00	0.00	VIA:VIA80	5.00	0.00	ALL_ALLOWED	TRUE	ANYWHERE

Figure 13. Constraint manager after changing the widths of the three power nets.

4.3 Add mounting holes

Most PCBs need to be mounted inside a piece of equipment and therefore need holes for fixings. Mounting holes and similar features are called *mechanical symbols* and are placed in a slightly different way from electronic components because they are not part of the netlist.

1. Select Place > Manually... to open the Placement dialogue box, bring the Advanced Settings tab forward and choose to Display definitions from Library. This is necessary because the symbols are not in the database imported from Capture.

2. Return to the Placement List tab and select Mechanical symbols from the drop-down list.

3. Use the same procedure as before to place a MTG156 symbol near each corner of the board. This is a hole of diameter 156 mils or $\frac{5}{32}''$. Do not place the holes too close to the edge or the board may break when it is drilled.

Mounting holes are shown on my routed PCB in figure 18 on page 34.

4.4 Preparation for routing

Power tracks are usually made wider than signal tracks because they have to carry more current. Our tracks are already so wide that it's barely necessary but we'll do it for future reference.

1. Choose Setup > Constraints > Physical... from the menu bar. This brings up the Constraint Manager and a Tip of the Day if you are unlucky (sigh).

2. The left-hand part of the window shows the various properties that can be edited. Click on All Layers under Net. See figure 13 for guidance.

3. The design part of the window now shows a list of the nets in your design. Most of them have random-looking numbers, such as N17311, but a few are named. These are the nets that carry power, to which we assigned names in Capture: VCC, VEE and GND_POWER or something similar, depending on the symbol that you chose.

4. Change the minimum width for these three nets from 25 to 50 mil. These are in the column under Line Width and Min. (I have changed other defaults in figure 13 but don't worry about these for now; I'll explain in section C.6 on page 56.)

5. Choose File > Close to return to PCB Editor.

Save a copy of your board before routing so that you can use it for double-sided routing.

4.5 Autorouting a single-sided board

The instrumentation amplifier is simple enough that it is easy to route the tracks by hand and this gives the best layout. However, manual routing is impracticable for large boards and we shall therefore use the autorouter to gain experience of the procedure. You will do this twice: first as a single-sided board as in the one-transistor amplifier, and later as a double-sided board. It is possible to route all tracks on the single-sided board if you have laid it out well but the double-sided board should have a simpler layout with a smaller total length of track.

Two approaches are available for routing the board automatically, both shown in figure 1 on page 4: Everything can be done from within PCB Editor or you can run the router as a separate application. The first is more convenient but the second offers finer control.

Autorouting may not be possible with the demonstration version of PCB Editor.

Autorouting from within PCB Editor

Choose Route > PCB Router > Route Automatic... from the menu bar. This brings up the Automatic Router dialogue box shown in figure 14 on the next page. Unfortunately it often causes a fatal error message that SPECCTRA quit unexpectedly with an exit code of 3, in which case you must use the other method.

Note. I have no idea what causes this; some computers in a classroom work while others fail, despite a nominally identical installation. ❦

Select Use smart router for the Strategy. For a single-sided board deselect the box next to the TOP Routing Subclass. You might wish to experiment with the Routing Direction for the bottom layer. Click Route and wait for the results to come back. Use the Results button to get a report on the routing and check the Completion percentage to ensure that all nets were routed successfully. Confirm this with Display > Status... and save your board.

If you can't locate DRC errors, choose Tools > Quick Reports > Design Rules Check Report from the menu bar. This gives a table of all errors including hyperlinks to their location.

After all tracks have been successfully routed, choose Route > Gloss... from the menu bar. *Glossing* means to tidy up the design. This includes spreading tracks apart where possible and replacing 90° corners by 45° bends (mitering). Accept the defaults and gloss your design. Finally, use Tools > Quick Reports > Etch Length by Layer Report to find the lengths of the tracks and add them up. In general, a better design has shorter tracks.

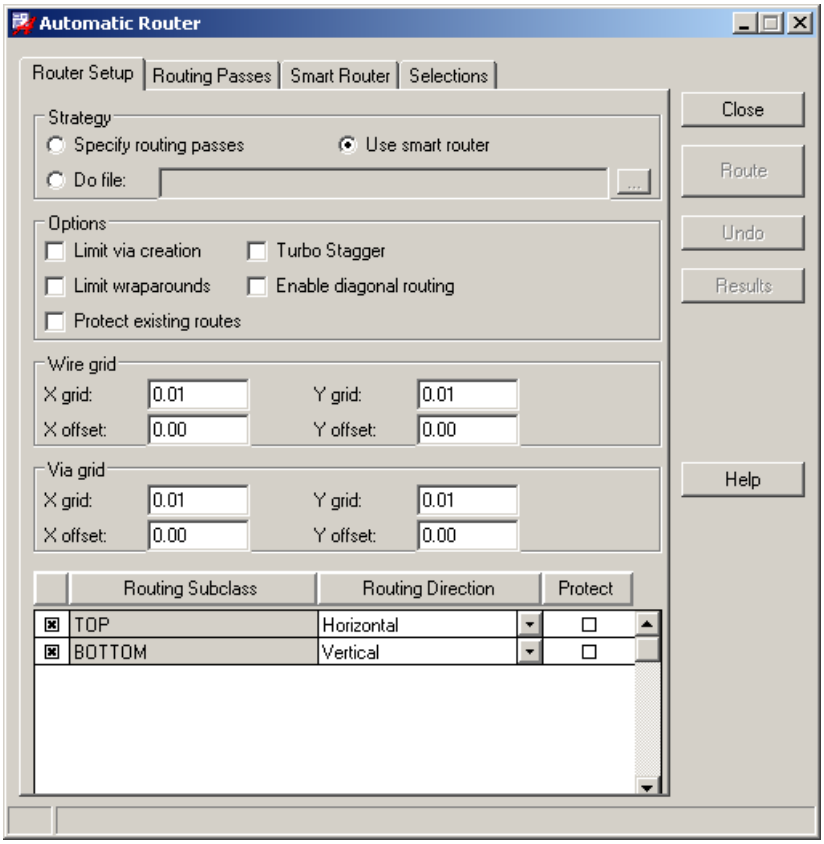


Figure 14. Dialog box for running the autorouter from within PCB Editor.

Note. The gloss command occasionally appears to unroute some of the tracks, which revert to lines of ratsnest. Use View > Refresh to redraw the display and check carefully. Abandon the glossing if it has damaged your routing. ❦

Autorouting with OrCAD PCB Router

Use the manual equivalent of the flow described in the previous section if automatic routing does not work from PCB Editor. It's a bit clumsier but gives better control over the process and makes it easier to experiment with different settings.

Note. At some point you may get a Licensing Error warning from PCB Router. Click Ignore Feature for This Session if it appears. ❦

1. Choose File > Export > Router from the menu bar of PCB Editor. It asks you for a name for the Auto-Router Design file and you can probably accept the suggestion. Click Run. You may be warned about overwriting the file, which isn't a problem. A message Translation Completed should appear, after which you can close the box.

2. Start OrCAD PCB Router from the Windows Start menu. You are presented with the fairly complicated dialogue box shown in figure 15 on the following page. Use the Browse... buttons to open the following two files.

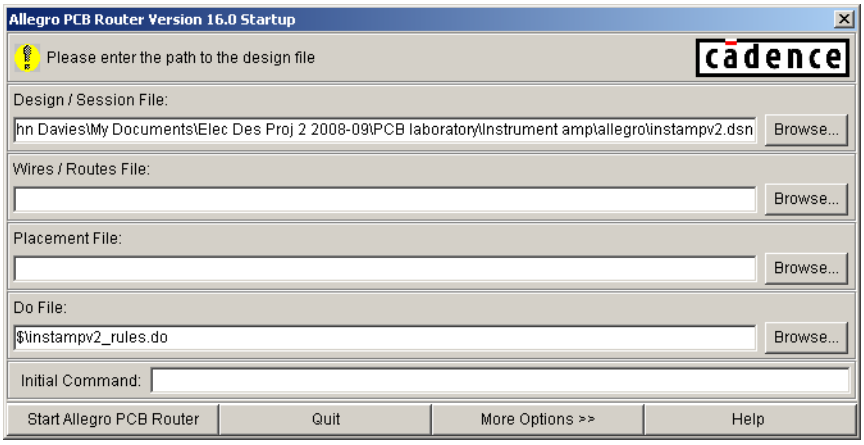


Figure 15. Startup dialogue box for importing a design into PCB Router.

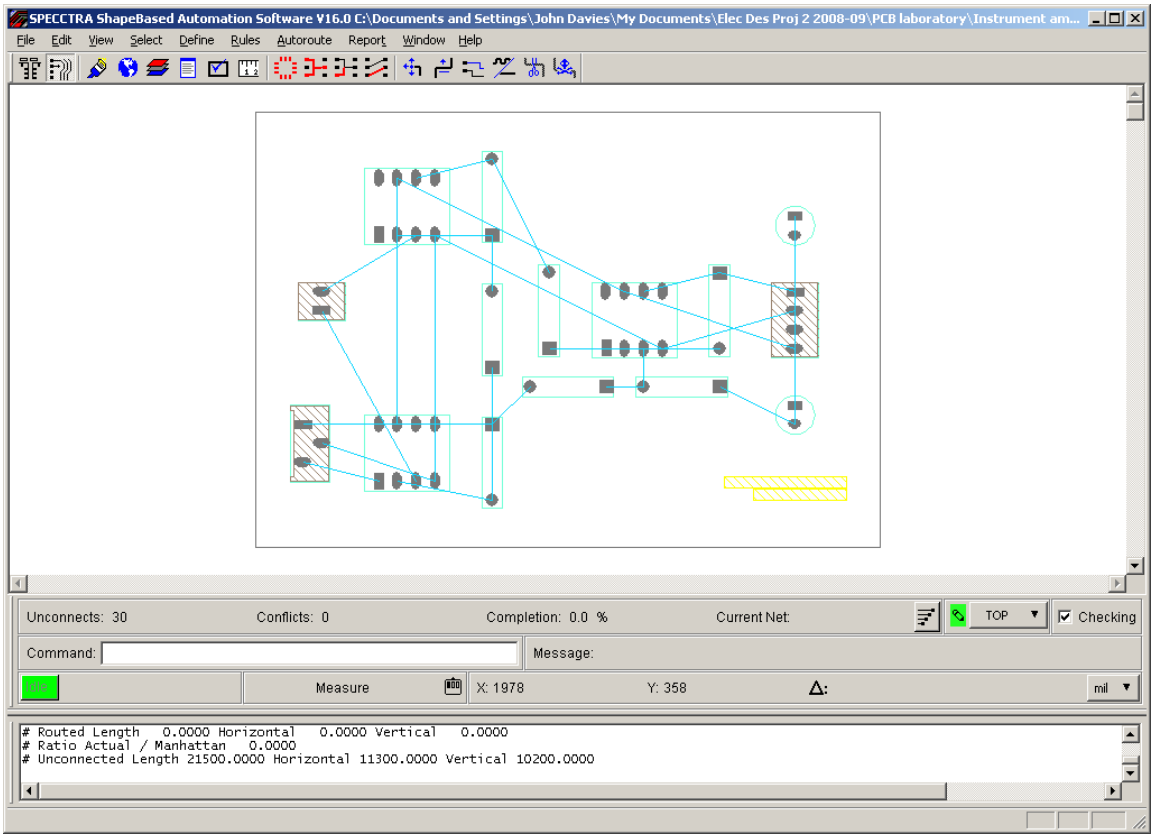


Figure 16. Screenshot of PCB Router with the instrumentation amplifier. I have changed the background of the window to white for a clearer printout. This design uses different footprints and the diagonally hatched areas show route keepouts, where tracks are forbidden.

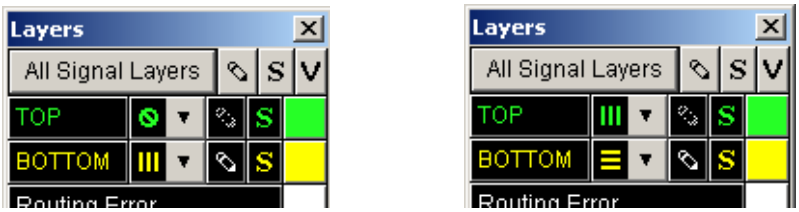


Figure 17. Settings in the Layers box for single-sided routing on the bottom layer and double-sided routing on both layers.

- For the Design / Session File (the first), choose the file that you just exported from PCB Editor.
- For the Do File (the last), choose the file with _rules appended to the name of your board file.

Click Start Allegro PCB Router to dismiss the box. PCB Router starts and you should now see your components joined by the ratsnest within the outline of the route keepin as in figure 16 on the previous page. Some components have shaded footprints, which I'll explain later.

3. Tell PCB Router to route only the bottom layer. Choose View > Layers... from the menu bar. Turn routing off for the top layer by clicking on the drop-down menu next to TOP as shown in figure 17 and selecting the ⊘ symbol. You might like to experiment with the setting of the BOTTOM layer. The directions are hints to the router but in practice tracks are drawn in both directions. Click Close when you have finished.

4. Choose Autoroute > Route.... Leave Smart selected and click OK. The autorouter works away and you will see Message: Smart_route finished, completion rate: 100.00% if all is well. The tracks should be in colour if they are routed successfully, yellow for the bottom. Sometimes they are drawn white, which should indicate a design rules error, even when they are correct – I don't know why.

   See the suggestions below if the autorouter is unable to route your board.

5. Two further commands improve the tracks for assembly. First choose Autoroute > Post Route > Spread Wires... and accept the defaults. This spreads the tracks away from each other and from the solder pads.

6. You'll have noticed that the autorouted board has 90° bends in the tracks, which I told you to avoid when you routed the board by hand. We'll now sort this out. Run Autoroute > Post Route > [Un]Miter Corners... and accept the defaults. Corners are rounded off and tracks run diagonally where possible.

7. To see the details of the finished layout, choose Report > Route Status. This may show a lot more than you want to know! Look near the bottom and confirm that the Unconnected length is zero. The Routed length is also given here.

8. Choose File > Quit... and agree to Save and Quit. This writes a *session* file that describes the routed tracks.

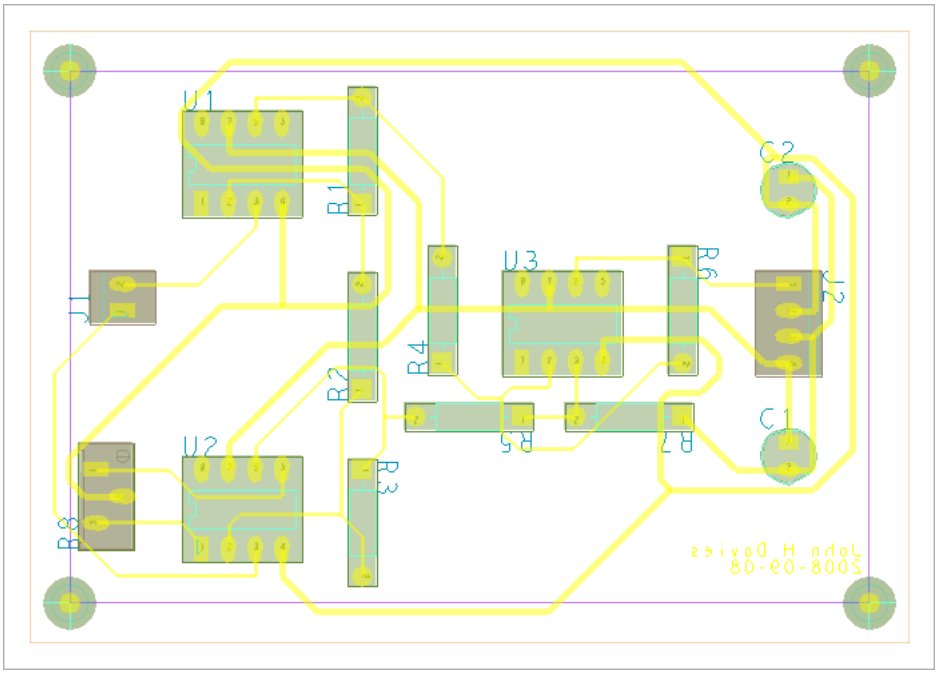


Figure 18. My one-sided layout after autorouting. The total routed length was 29.3″. The footprints are not taken from the Cadence library.

9. Return to PCB Editor and choose File > Import > Router.... Locate the Session File whose name matches your board and click Run. You should see a message Translation Completed. Close the box.

10. The window now shows your design with tracks instead of the ratsnest. Save it under a different name to preserve the unrouted board for later.

Help! – My board won't route

Here are some suggestions for helping the autorouter.

1. If routing has almost worked (only one or two unrouted segments), try changing the hints given to the router. For the one-sided board there is only the suggested direction of tracks. It is best to unroute the board and begin afresh. Choose Edit > Delete Wires > All Wires from the menu bar of PCB Router or reload the unrouted version of your board in PCB Editor.

2. If you are far from success, look at the layout to see where the problems lie. Often one particular track prevents successful routing. Can you rearrange the components to solve the problem?

   Quit from PCB Router *without* saving, or reload the previous version of your board in PCB Editor. Rearrange or reorientate components to make the ratsnest simpler and ease the problem before trying the autorouter again.

If none of this works, get advice from a more experienced PCB designer.

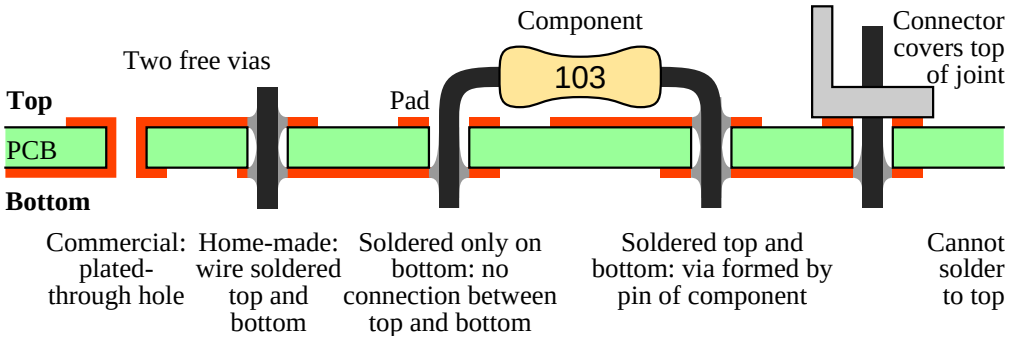


Figure 19. Cross-section of a double-sided printed circuit board showing free vias formed by a plated-through hole and a wire through a non-plated hole soldered top and bottom. A via can also be formed using a pin-through-hole component but not at a connector because it covers the top pad.

4.6 Final touches

Put your name on the bottom etch layer, run a final design rule check, save your routed board and make a coloured plot as before. My layout is shown in figure 18 on the previous page. It is a poor board in many respects despite the successful routing. The power tracks are excessively long in particular. It is not hard to see how the components could be rearranged to improve the layout.

5 Instrumentation amplifier – double-sided board

We will now route the board using both sides like many commercial PCBs. Having said that, *use a single side wherever possible* if your PCB is made using an old-fashioned process. Many problems occur with double-sided PCBs, mostly from badly placed vias, as I'll now explain.

Figure 19 shows a cross-section of a double-sided PCB. Commercially produced PCBs have *plated-through holes* (PTHs), which means that the copper plating extends through the holes and joins the pads on the two sides of the board. A *free via* is a hole that is used purely to move a track from one side of the board to the other, rather than to mount a component. The plating carries current between the layers. Simple, manual processes cannot plate through holes, in which vias need more effort: A wire must be pushed through each hole and soldered top and bottom to join the layers of etch.

The wires of through-hole components can also be used as vias. This works well for some components, such as resistors and capacitors. However, it fails for others, such as connectors, because it is impossible to solder the pad on top of the board – it is hidden under the base of the connector. The pins of an integrated circuit can be used as vias if they are soldered directly to the board but it is safer to put ICs in sockets for PCBs that are assembled by hand and these hide the pads too. *Vias must therefore be placed with great care if the PCB does not have plated-through holes.*

To illustrate these problems, figure 20 on the next page shows the two-sided layout of the instrumentation amplifier as it might come from the autorouter. (I should admit that I fiddled the layout to make it worse!) It obeys the design rules but is hard or impossible to assemble by

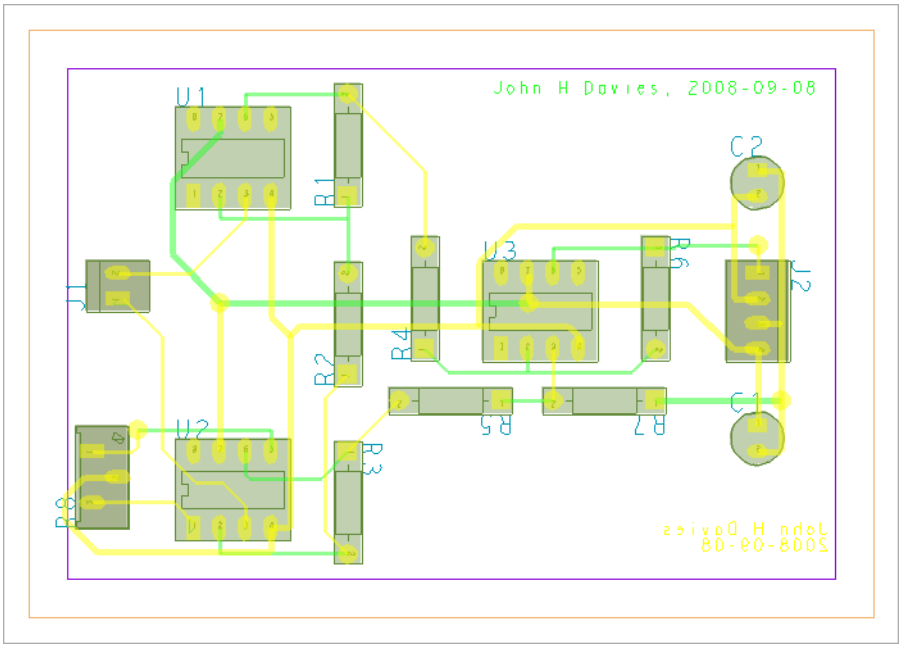


Figure 20. Screenshot of a poor double-sided layout with several badly-placed vias.

hand.

- The board has five free vias, far too many for a board that could be routed successfully with only one layer. The worst via is under U3, which is unacceptable for a home-made via because the wire in the via would obstruct the integrated circuit. (There would be no problem on a commercial board with plated-through holes.) Another via is very close to the trimmer (R8) and it would be difficult to solder this without damaging the trimmer. You would have to solder the via first and keep it neat.
- Several pins of resistors act as vias – R3 has two, for instance. These are easy.
- The pins of the integrated circuits are connected to tracks on both the top and bottom. This is not a problem if the IC is soldered directly to the board but won't work if it is in a socket.
- The connectors (J1 and J2) and the trimmer (R8) have tracks only to the bottom of their pins. This is why the via is needed near R8. No tracks run to the top because the symbols for these components have *route keepouts* on the top, which forbid the router from placing tracks there. The footprints have diagonal shading in PCB Router to show this, visible in figure 16 on page 32.

The general rule is to *avoid vias wherever possible* if your manufacturing process does not plate through holes. Every via requires two soldered joints (top and bottom), which dramatically reduces reliability.

Now route your board for the instrumentation amplifier using both sides.

1. Re-open the unrouted version of your board.

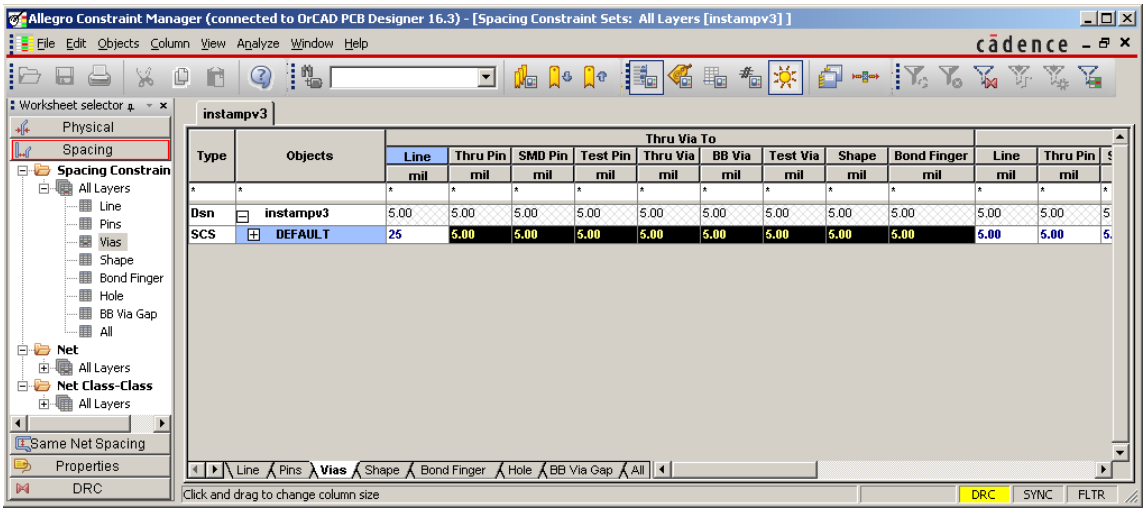


Figure 21. Constraint manager for changing the spacing around vias. The row of cells under Thru Via To has been selected and the value 25 typed into the first cell. This will fill the other cells selected after hitting the Enter key.

2. Remember the Default via padstack when you used the new board wizard? We specified VIA26. Unfortunately this has a bug because another type of via called simply VIA appears in the design and is used wrongly by default. This VIA is much too small so we must get rid of it.

   Fixup. Choose Setup > Constraints > Physical... from the menu bar and select the upper All Layers spreadsheet under Physical Constraint Set. This resembles figure 13 on page 29 but has only a DEFAULT row. The column headed Vias probably shows VIA:VIA26. Click in this cell to open the Edit Via List. Remove VIA from the Via list on the right and click OK. The cell now contains only VIA26, which is what we want. Close the Constraint Manager and return to PCB Editor. ❦

3. The new board wizard set up several spacings based on the minimum line width of 25 mils. Unfortunately it does not set up the spacing around vias, which is only 5 mils by default. This is too small for reliable construction by hand and should be increased to match the other spacings.

   Fixup. Choose Setup > Constraints > Spacing... from the menu bar to open the Constraint Manager and select All Layers > Vias as in figure 21. Drag the mouse to select all the cells under Thru Via To in the DEFAULT row. Type 25 and hit Enter, which copies this value into all cells selected. Close the Constraint Manager and save your board. ❦

4. Run the autorouter from within PCB Editor or export the board to PCB Router as before. This time you should allow routing on both layers, which is the default. You might like to experiment with the directions. Note the routed length and the number of vias; a good

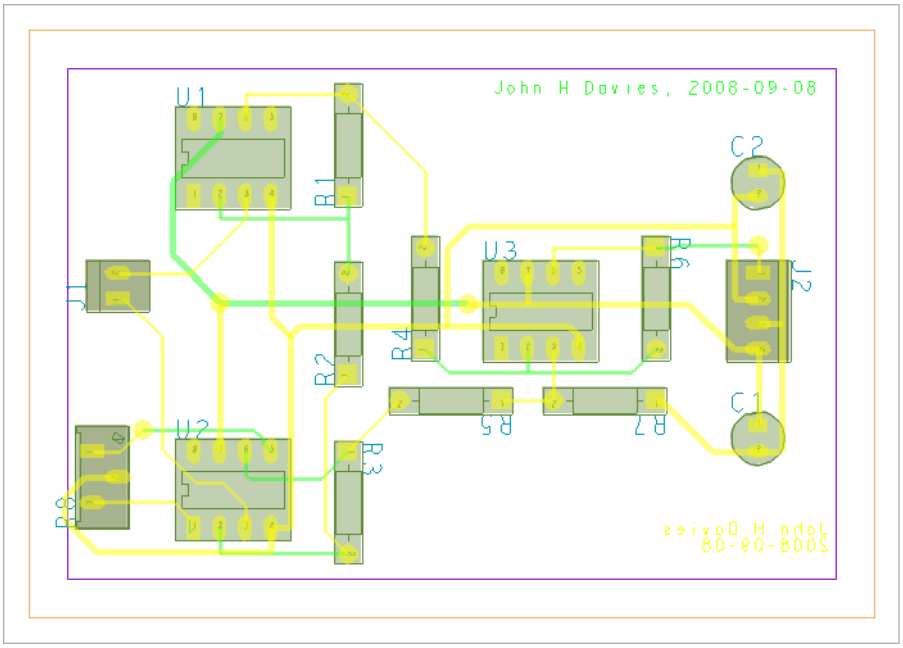


Figure 22. Double-sided layout after improving the layout and moving the badly-placed vias.

design may have none at all, which is a bonus. Remember to gloss or space and mitre the tracks.

5. Import the tracks into PCB Editor if you used PCB Router. Save the routed board under a new name.

You must move any vias in inconvenient places, such as that under U3 in figure 20 on page 36. If you are lucky you may be able to Slide the via but it is often better to rip up the complete track and re-route it by hand. Other tracks must often be moved to create space for the via.

- Select the cline or net with the offending via, right-click and choose Delete or Ripup etch from the contextual menu.
- Select the connect tool and check in the Options control panel that the active and alternate layers are correct.
- Draw out the segments of the track as usual.
- Double-click when you reach the point where a via is needed. A via is inserted and routing switches to the alternate layer.
- Continue routing to complete the track.

I made several changes to the board to get the final version in figure 22.

- The via was moved from under U3 to a clear region of PCB.
- Another via was moved away from R8.

- The via near C1 was eliminated by rerouting the tracks slightly.
- Several tracks were moved from the top to the bottom, which makes the board easier to solder by hand.
- It would have been better to edit the board further so that all tracks leave the ICs on the bottom of the board. This would require extensive rerouting and more vias to be inserted. (Better still, I could have added a route keepout on the top layer of the footprint for the ICs. We have a local library with features such as this to help inexperienced students.) I also prefer to avoid vias in the tracks for power and ground.

When you have finished editing your board, add text to both layers of etch to identify them. It would be embarrassing if the top of your board was processed with the bottom of somebody else's. Finally, plot the finished board in colour.

6 Artwork and drill files

The next step is to get the board made! Many routes are possible, depending on whether the board will be produced manually or automatically. You typically send a set of electronic files to a commercial manufacturer. Each company specifies its preferred formats and you should obviously follow this advice. Two types of file are typically needed.

- **Artwork** files contain images of the conducting (etch) layers and silkscreen, one file per layer. These are often known as *gerbers* after a well-known company, whose formats are widely used.
- **Drill** files provide a list of holes to be drilled, as you might guess, with their positions and diameter. These are often called *excellon* files after another company.

Further information, such as placement files, may be needed if the board is to be assembled automatically. Other processes may use ODB++ rather than artwork and drill files but lie far beyond the scope of this tutorial.

I'll first explain how to produce photomasks directly from PCB Editor, which is useful if the PCB is made manually. The remaining sections show how to generate files for a commercial process.

6.1 Photomasks for manual production

This section shows how to get a black-and-white plot that can be printed onto tracing film to act as a photomask, which is used to manufacture your board manually. I'll explain the most basic procedure here, which gives solid pads on the plot. Such boards may be drilled by hand as well, in which case it is helpful to leave open holes in the pads to guide the drill. This is more tricky so I've deferred it to section E on page 65. *Save your design before starting this procedure* in case you make a mistake and wreck the board. The major step is to change the colours so that only the desired features are visible and to plot these in black.

Tip for Layout users: You will be used to similar manipulations with the post-processing and colour spreadsheets. ❦

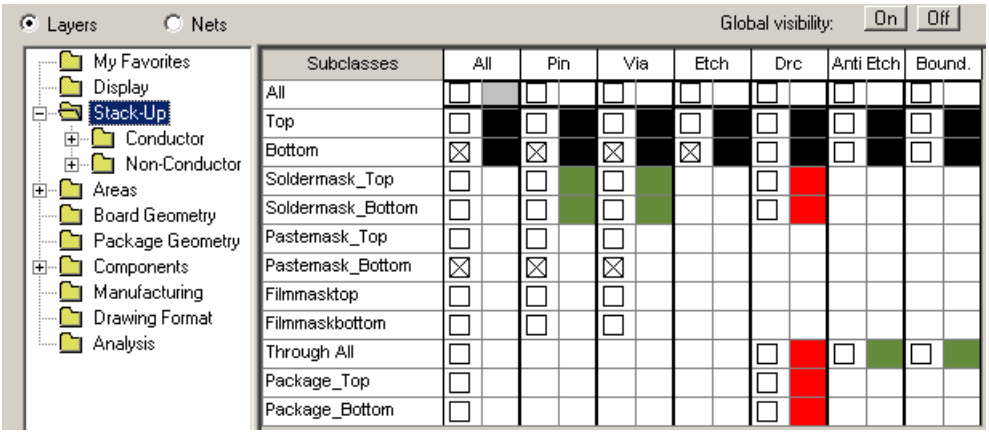


Figure 23. Part of the Color Dialog box, showing the settings for the Stack-Up to plot the bottom layer. Ignore the Pastemask_Bottom, which is is explained in section E.3 on page 68.

1. Open the Color Dialog box with Display > Color/Visibility... from the menu bar.

2. Click the button to turn Global Visibility Off, agree to Make all classes invisible in the small dialogue and click Apply in the main dialogue (this is needed after every change to see the effect). The design vanishes from the design window.

3. Click the Display folder in the list on the left. We must change the Background colour of the window so that tracks show up after their colour has been changed to black. Click on the white swatch in the Color swatches (samples of each colour) near the bottom of the window, then click the swatch next to Background, which turns white. Click Apply to update the design window, which also turns white.

4. Now we need make the desired features visible again and paint them black. Start by selecting Board Geometry from the list on the left. This brings up a set of Subclasses to the right. Select the checkbox next to Outline to turn it on. Change its colour to black by clicking in the black swatch in the Color region, then the swatch next to Outline. Finally, click Apply and the board outline becomes visible in the design window.

5. This must be repeated for all the features that we wish to print. For the bottom of a PCB these are Stack-Up/Conductor/Bottom/Pin, Via and Etch. Activate and make them black as shown in figure 23. Click Apply and your tracks appear, which completes the bottom of the PCB. Close the Color Dialog.

6. Check the Plot Setup. Set the Scaling factor to 1.00 so that the mask has the correct dimensions for the finished PCB. Leave the Default line weight as 10 or text may be too thin for reliable etching.

7. Finally, choose File > Plot... as usual and you should get a beautiful picture with the board outline and etch.

8. Repeat these steps for the top of a double-sided board. Deactivate the bottom subclasses and make the top ones active instead. Open Plot Setup and choose Mirror under Plot orientation.

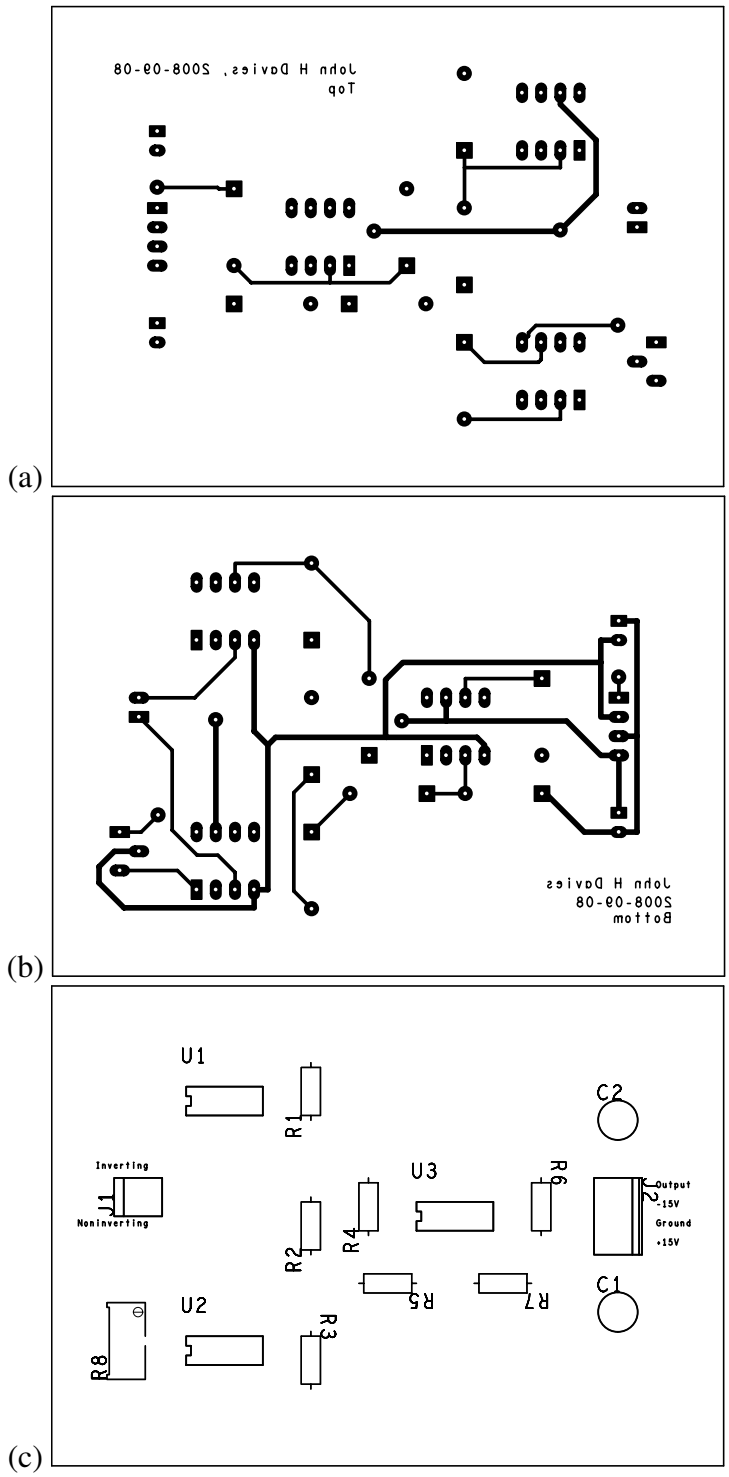


Figure 24. Printouts at actual size for the (a) top and (b) bottom of a double-sided board with (c) a silkscreen plot to assist assembly. Note that text appears mirrored on both the top and bottom. The instructions in section 6.1 produce solid pads; see section E if you want holes in the pads to guide the drill, as shown here.

The plot must be mirrored because the printed side of the mask is turned over and placed next to the copper when the photoresist is exposed. A good check is that text should be mirrored on both masks for a double-sided board. (The text on the bottom is also mirrored on your computer's screen but the text on the top is mirrored only on the plot.)

9. You might also wish to print a sort of 'silkscreen' to help you assembly the board. Use the same procedure and select the following classes.

   - Package Geometry: Assembly_Top and Silkscreen_Top subclasses
   - Components: All Cmp Val and Ref Des

   Check the display: you may need to adjust this selection, depending on how your symbols were drawn.

Figure 24 on the previous page shows my plots for the double-sided board. After all this, quit from PCB Editor *without saving* (or reload your design) to avoid messing up the colours next time you use it.

6.2 Drill files

This is the easy one! Choose Manufacture > NC > NC Drill from the menu bar and click the Drill button. PCB Editor writes a file with extension .drl in the widely accepted Excellon format. It is plain text so you can check it with a simple editor.

Open NC Parameters before creating the file if you need to change any settings to suit your manufacturer. European manufacturers may ask for metric drills, for instance. Choose Drill Legend from the menu if you want a drill chart. Each hole on the PCB is labelled with a symbol (hexagon, oval, ...), which is identified in a table that is added to the drawing. Layout users will find this familiar.

6.3 Artwork files for conducting layers

The next step is to produce an artwork file, also known traditionally as a film, for each conducting (etch) layer. The New Board Wizard had an option to Generate default artwork films (section 2.5 on page 10), which should have created settings for the top and bottom layers of etch. To preview these films, open the Visibility control panel and look in the drop-down list of Views. You should find Film: TOP and Film: BOTTOM. Select these to show the objects that will be drawn on the respective films: tracks, pads, vias and any other items that you added to the layers of etch.

Curiously there seems to be no way of restoring the original view other than reloading the design. Alternatively, open the Color Dialog (Display > Color/Visibility... from the menu bar or Color192 command), turn Global visibility On and turn off any unwanted classes.

Create the films

Define a photoplot outline before creating the films. This should be a rectangle that extends beyond the PCB. Choose Setup > Areas > Photoplot Outline from the menu bar (keepin photo

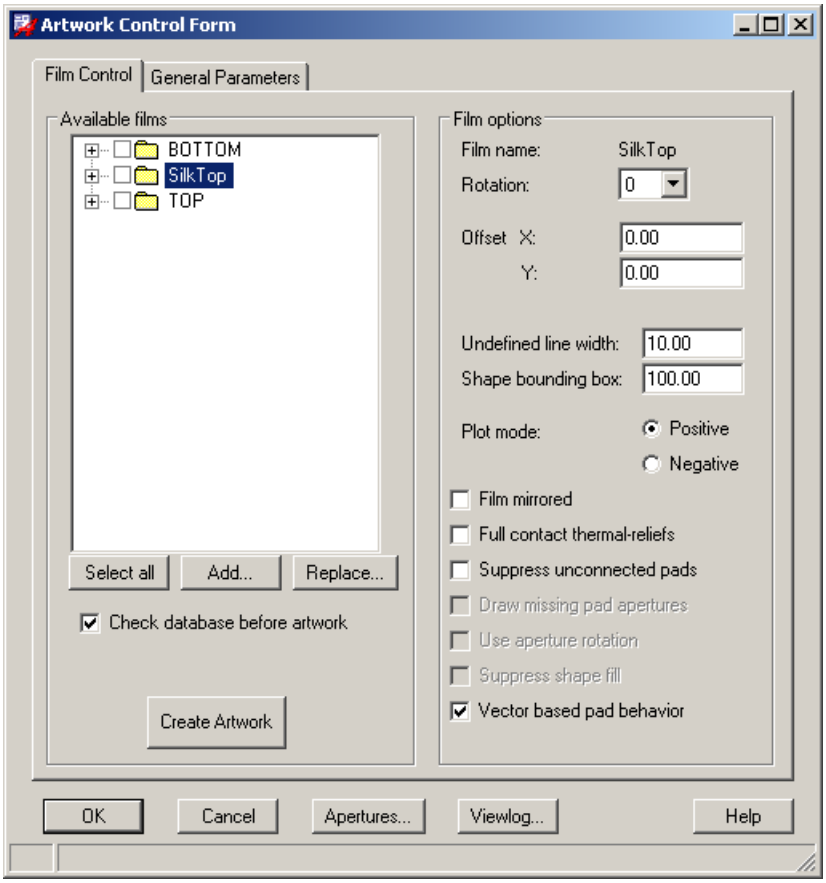


Figure 25. Film Control tab of the Artwork Control Form.

command). Click first to create one corner, then click again in the opposite corner to define the rectangle. Right-click and choose Done.

To create the films, select Manufacture > Artwork... from the menu bar (film param command), which opens the Artwork Control Form. Make the General Parameters tab active and choose the Device type that your manufacturer advises. The extended Gerber format with embedded apertures (RS274X) is widely accepted (the older RS274D format requires a separate list of apertures). You may receive a warning about the artwork accuracy. If this happens, increase the number of Decimal places in the Format section until the error goes away. The remaining parameters are probably satisfactory.

Return to the Film Control tab. It should resemble figure 25 except that the list of Available films contains only TOP and BOTTOM. Expand the tree for a folder to show the classes included in the film: etch, pin and via class. There is probably no need to adjust the Film options on the right for the etch layers unless you have included text, in which case you should enter a nonzero value for the Undefined line width. (The lines used to draw text have undefined width. Some manufacturers ask for text on etch layers to confirm which is top and bottom; the bottom should have mirrored text.)

Click the Select All button below the list, then on Create Artwork. A progress box appears and, with luck, it concludes with Successfully Completed. Unfortunately it is often overoptimistic so you should click the Viewlog... button and check for warnings. Look out for

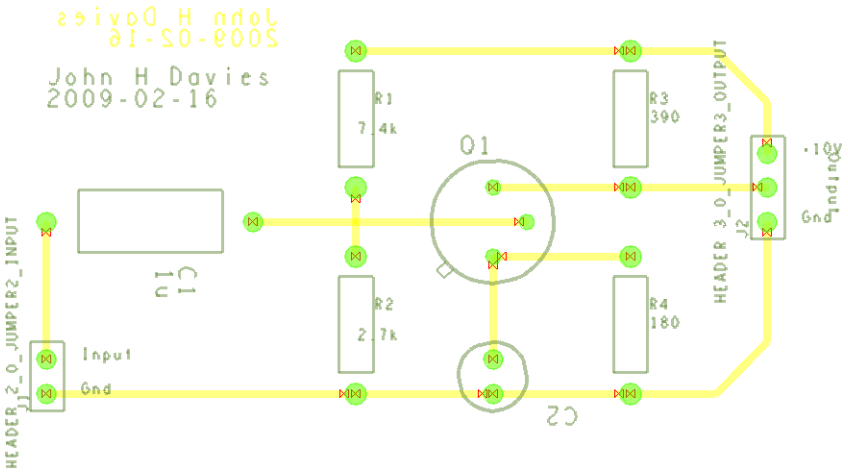


Figure 26. Review of artwork for top, bottom and top silkscreen films. The board outline is not included in the films.

undefined line widths in particular. The artwork files are called TOP.ART and BOTTOM.ART. They are plain text and can be opened with an editor if you are interested. Some manufacturers ask you to rename them so that their extension identifies the layer.

Review the films

Review the artwork before sending it away. This is clumsy. Create a new board file and choose File > Import > Artwork... from the menu bar (load photoplot command, also called load gerber). Browse for one of the films that you have just created, TOP say. The dialog box should change to show the correct Format, such as Gerber RS274X. Leave the Origin at its default of Absolute Origin. Select the appropriate class and subclass, Etch/Top in this case, then click on Load file (*not* OK, which closes the dialog box, really irritating). A rectangle appears, centred on the cursor, so that you can place the imported image. Click on the P (Pick) button in the status bar below the windows, type coordinates of 0 0 into the Pick box and click Pick. This ensures that the image is precisely positioned so that all layers are correctly aligned. (If you have a steady hand you can instead move the mouse to coordinates of 0 0 as shown in the status bar and click in the design window.) Repeat for the bottom film; the Pick box remains visible and holds its previous entry so you just have to click on Pick. Click OK when you have imported all the films. Figure 26 shows the result except that I have included a silkscreen film as well, as I'll explain in the next section.

Use the Visibility control panel to hide the layers of etch so that you can inspect each individually. I am not sure why the drawing is cluttered with DRC errors.

6.4 Silkscreens

Many classes of the database contain information in a silkscreen subclass so these must first be merged to produce a complete silkscreen. Choose Manufacture > Silkscreen... from the menu bar to open the Auto Silkscreen dialog box (silkscreen param command). Most of the options are reasonably clear. You may wish to turn off unwanted classes and subclasses, such

as Tolerance and User part number, by selecting None. Click the Silkscreen button when you have finished. PCB Editor then merges the separate silkscreen subclasses into the Autosilk_Top and Autosilk_Bottom subclasses of the Manufacturing class and displays the result. Check the command window for any errors.

The design looks cluttered if both the individual silkscreens and the new, composite silkscreens are displayed. Hide the individual silkscreens by opening the Color Dialog, selecting the components folder, and turning all items off with the top left check box. (Alternatively, use the button next to each class in the Options control panel.) You may also wish to deselect further silkscreen subclasses of Board Geometry and Package Geometry.

The next issue is how to write a file or files with the silkscreen data (I'll assume that there is only a top silkscreen). It can be printed as in section 6.1 on page 39 but the most common route is to create an artwork file like those for the etch layers. No films for silkscreens are defined by default so here is the procedure for creating them.

1. Open the Color Dialog, turn Global visibility off, then go to the Manufacturing folder and turn Autosilk_Top back on. Click OK, which leaves only the (top) silkscreen visible in the drawing.

2. Open the Artwork Control Form with Manufacture > Artwork. . . . Right-click on one of the available films and choose Add. (Do not try the Add. . . button, which is for selecting a previously created film record.) Give the new film a name such as Silkscreen_Top. It includes the classes that are currently visible in the drawing and is added to the list of available films.

3. Select the folder for the newly added film in the list, which brings up its options in the right-hand panel. Enter a nonzero value for the Undefined line width. A suitable value is 10 (mils); a smaller value is unacceptable to some manufacturers because silkscreens are produced at lower resolution than etch. *This step is essential* because many lines in the silkscreen have undefined width and are useless if they are drawn with a width of zero.

4. Select the checkbox for the new film and click Create Artwork. The photoplot log file will almost certainly appear with plenty of warnings. These are no problem if they warn you that the undefined line width has been used for 0 width lines and text. Otherwise, check.

5. Review the .art file as usual.

Further films are needed for the soldermask(s) and some manufacturers ask for a film with the board outline alone. Make these in the same way.

7 Summary: PCB design flow

This list is adapted from a handout by Mr I. Young. *Save your work frequently!*

1. Draw the circuit in Capture.
    - Make a new directory before starting each new design.
    - Check the circuit carefully before starting the layout.
    - Make sure that all integrated circuits have power connections. If power pins are hidden you must place matching power symbols on the supply rails.
    - Edit components with incorrectly numbered pins, such as electrolytic capacitors.
    - Mark all unconnected pins and add the No Connect property to packages with unused pins.
    - Add footprints from an appropriate library.
    - Run a Design Rules Check and correct any errors.
2. Set up a bare board in PCB Editor using the New Board Wizard.
    - First make an allegro directory.
    - Use appropriate design rules for your manufacturing process.
    - Make the size of board generous; you can reduce it later.
3. Netlist the design in Capture. Check any warnings carefully.
4. Place the components on the board in PCB Editor.
    - Arrange and orient the components to simplify the ratsnest as far as possible. *This step is critical to get a well-routed board.*
    - Add mounting holes if required. Do not place them too close to the edge.
    - Use wider tracks for the power supplies and fix the list of vias.
    - Run a Design Rules Check and correct any errors.
5. Route the board.
    - Manual routing is best for a simple design.
    - If you must use the autorouter, try a single-sided board first. Check that the completion rate is 100%.
    - If you cannot avoid a double-sided board, review the results of the autorouter carefully. Move any vias and tracks on the top that cannot be soldered easily.
    - Gloss the design in PCB Editor or PCB Router.
6. Add text to identify the board and connectors.
7. Generate artwork and other files to suit your PCB manufacturer.

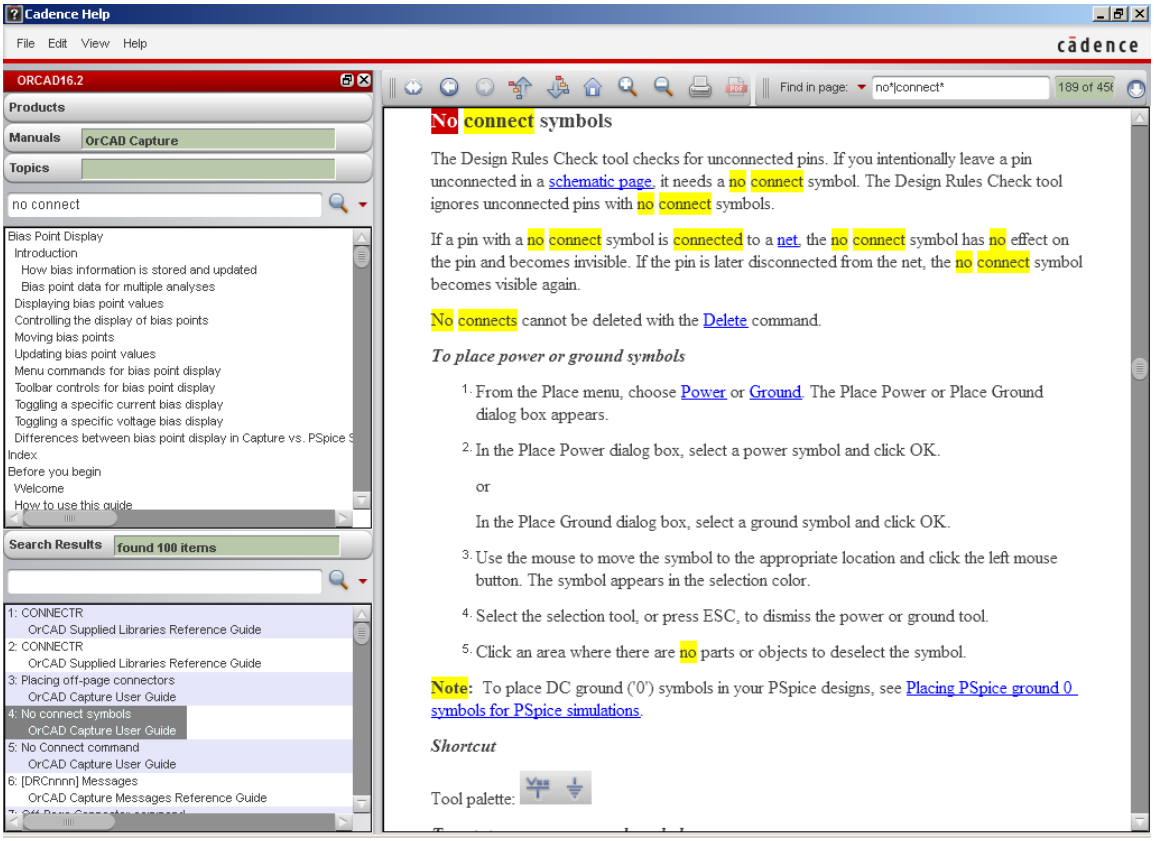


Figure 27. Cadence Help system with the Navigation pane opened.

A Where to learn more

Extensive documentation is provided with OrCAD, divided into over 100 documents. An unhelpful feature of the Cadence help system is that it opens only with the page associated with the most recent action rather than offering the full range of documents. Go to the menu bar of the Cadence Help page and choose View > Navigation > Show, which produces a screen like that in figure 27. Use the navigation panel on the left to choose the appropriate product and type the desired topic into the Topics box.

The manuals are also supplied as pdf files, which you may find easier to read. Unfortunately their names are cryptic and the interdocument links have been set up in a way that works only on unix. Here is a guide to the most helpful documents with their filenames (all have the extension .pdf, which I have omitted). The documentation is not entirely consistent with OrCAD PCB Editor, nor has it been updated thoroughout for version 16.3.

- The *OrCAD Flow Tutorial* (flowtut) takes you through the complete process of capture, simulation and PCB design and covers several techniques that I have not described in these notes.
- *OrCAD Capture User's Guide* (cap_ug) has a particularly relevant chapter on *Using Capture with PCB Editor*, which includes issues such as assigning the No Connect property.
- *PSpice User's Guide* (pspug) describes simulation and analysis.

- The *Allegro PCB Editor User Guide* (algromast) is the most helpful set of documents but is so long that it is split into thirteen parts, of which these are most relevant:

    1. *Getting Started with Physical Design* (algrostart). This is the most useful document for learning how to use Allegro.
    2. *Defining and Developing Libraries* (algrolibdev). Mostly devices, symbols and padstacks but also technology and parameter files.
    3. *Transferring Logic Design Data* (algrologic). Despite the name, this means importing from Capture or a similar application and includes analogue components.
    4. *Preparing the Layout* (algrolay). This includes the cross-section of the board, keepins and keepouts, padstacks and etch shapes – fills or pours.
    5. *Creating Design Rules* (algrodesrls). I've barely looked at this.
    6. *Placing the Elements* (algroplace). Most of this is rather advanced too.
    7. *Routing the Design* (algroroute). This describes different strategies for routing, both manual and automatic, and covers fanouts, which I have not mentioned.
    8. *Completing the Design* (algrodescmp). Another one that I have barely opened.
    9. *Preparing Manufacturing Data* (algroman). Covers the final steps needed to send a board for commercial manufacture – silkscreens, artwork (Gerbers) and drill files.

    You might also need the *Allegro Constraint Manager User Guide* (cmug). The *Allegro PCB Editor Tutorial* (algrotutorial) concentrates on the user interface.

- Routing from PCB Editor, both manual and automatic, is explained in the *Autorouting with Allegro PCB Editor Tutorial* (aleg_spec_tut). The *Allegro PCB Router Tutorial* (sptut) explains routing within PCB Router itself, for which the complete reference is *Allegro PCB Router User Guide* (spug).

- If you know precisely which PCB Editor command is involved, the files *A Commands* (acoms) to *Z Commands* (zcoms) contain comprehensive explanations of each command, often with helpful examples. The names of the commands are not always obvious, in which case the *Allegro PCB and Package Physical Layout Command Reference* (cmdrefmast) is the place to start. The new board wizard is under L (layout wizard), for instance. Figure 28 on the next page for the toolbars is taken from this manual. (It does not appear to have been updated for version 16.3.)

- The limits of the demo versions are in *OrCAD Demo Products Reference* (demoswitch).

Search the Cadence PCB Forum at www.cadence.com/community/forums/27.aspx if these references fail. The experts may have solved your problem already.

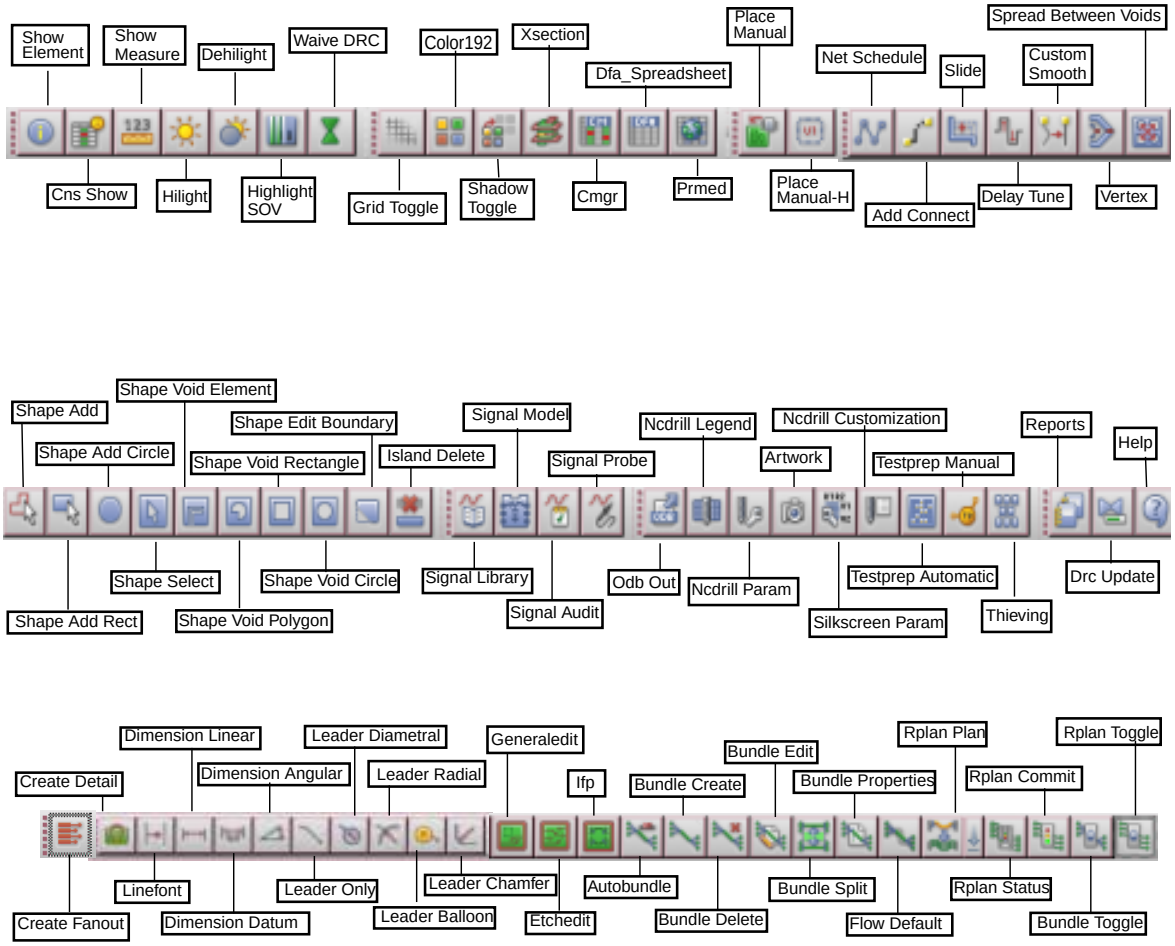


Figure 28. Toolbars in Allegro, taken from the *Allegro PCB and Package Physical Layout Command Reference*. It has not been updated for version 16.3. Not all of the buttons are available in OrCAD PCB Editor and many provide functions that I have not described.

Figure 29. Buttons on the toolbar in Capture for controlling the way in which objects are selected and whether wires are reconnected when an object is moved.

B Capture techniques

Entering repeated data into Properties

Here is a faster way of entering footprints into Capture if you have numerous components with the same footprint.

1. Select the identical components and open the Properties spreadsheet.
2. Click on the name of the property, PCB Footprint here, to select the whole row or column.
3. Right-click and choose Edit..., which opens a spreadsheet with as single cell.
4. Enter the value into the cell and click OK. This value is copied into all parts.

This sounds fine but how do you select all the parts with identical footprints? Capture offers several methods for dealing with large designs. Here's an example.

1. Make the project window active and choose Edit > Find.... Choose Parts and search for R*.
2. This opens the Parts Browser, which shows a list of the parts that match the search criterion. You can also open the browser with Edit > Browse > Parts, in which case it lists all parts.
3. Select the parts whose footprints should be identical and choose Edit > Properties... from the menu. This brings up a different form of properties spreadsheet.
4. Find the PCB Footprint column and enter the desired value into one cell. Copy it with the Copy button. Select the whose column by clicking on its heading and click Paste. The copied value now fills all cells.

Useful buttons on the toolbar

Figure 29 shows two handy buttons on the toolbar that are often overlooked.

- **Area select** controls the selection of objects by drawing a rectangle: whether they must be fully enclosed or merely intersected. This can also be chosen using Options > Preferences... and the Select tab.
- **Wire drag** controls whether or not objects are reconnected when they are moved around. (I find it hard to distinguish the two settings from the icons on the button.) This is useful if you wish to replace a component – you placed the wrong type of op-amp, for instance – and delete the incorrect object. By default Capture will not let you drop another op-amp into the empty space and connect it to the existing wires but this button permits it. The behaviour can also be set up using the Miscellaneious tab of Preferences.

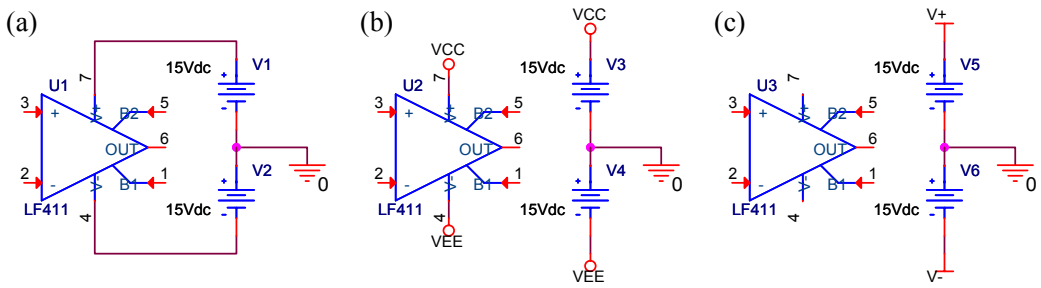


Figure 30. Three ways of connecting power pins to the supply rails.

Connection of power pins

Power pins can be connected to the supply rails in three ways, shown in figure 30.

(a) Complete wires are drawn, which rapidly gets clumsy in larger circuits.

(b) Power pins are wired to power symbols, whose names match corresponding symbols on the power rails. These are VCC and VEE here.

(c) Power pins have no wires at all; they are connected purely by name. Power symbols with the same names as the power pins must be connected to the appropriate supply rail. These are V+ and V– here (typical for op-amps). Sometimes the pins and their names are not shown at all.

The shape of power symbols doesn't matter, just their names. Automatic connection by name is a special property of power symbols and pins.

C PCB Editor techniques

C.1 Modes of operation

I didn't dwell on this because we would all rather try out the software than read a lengthy 'theory of operation' but here is a little more. The main point is that the tools in PCB Editor can be used in two different ways (see *Getting Started with Physical Design* for further details).

- **Menu-driven editing mode** or **verb–noun use model**. In this mode you first choose a command, either from the menu bar or by clicking a button, then the design element on which the tool should operate.
- **Pre-selection mode** or **noun–verb use model**. In this mode you first choose the object followed by the command, which is usually selected from the contextual menu by right-clicking.

Confusion can arise when you switch from one method to the other because the tools do not behave 'cleanly' if a command or object is already selected. Disable any active tool (right-click and choose Done if it is offered) and clear any selection (left-click outside the board or right-click and choose Selection Set > Clear All Selections) if things do not appear to be working correctly.

The verb–noun approach is a little more cumbersome but it is much easier to see what is happening, particularly if you keep the control panels open. For example, if you choose Add Connect, the Find panel automatically selects Pins, Vias and so on – the items to which a connection can be added. The Options panel displays the etch layers available and options for the tracks, such as width and angle of bends. If the Move command is selected instead, different options are offered and other classes are activated in Find. Figure 10 on page 21 illustrates this.

The noun–verb model is often more convenient when you know what you are doing and want to perform a set of operations on the same object. However, there is a huge number of possible operations and they don't all fit into a contextual menu. PCB Editor therefore has different *Application Modes*, which can be selected from the menu bar with Setup > Application Mode or with a button. These are the two most important modes.

- **General Edit** (GEN) is the most useful mode and is optimized for arranging components and adding connections.
- **Etch Edit** (EE) is for drawing new tracks and editing existing tracks.

Placement Edit (PLC) is not useful for the simple designs described here and Flow Planning (IFP) is not available in OrCAD. The current mode is shown near the right-hand end of the status bar below the windows.

The particular set of commands in the contextual menu depends on exactly what is selected. You may therefore need to adjust the Find control panel before you are able to select the desired element – a pin for Add Connect, for instance.

Use Setup > Application Mode > None to exit from the current application mode and return to a menu-driven editing mode (there is no button). No contextual menu is available and the Find control panel is deactivated until a tool or application mode is chosen again. PCB Editor appears 'dead' if there is no application mode nor tool selected.

If that isn't enough, further shortcuts are described in *Getting Started with Physical Design*. The following actions take place by default when you click on an object and drag it, often while holding a modifier key down, and are the quickest ways of performing the most common tasks. In general editing mode:

- dragging a symbol, text or via moves it
- control-dragging a symbol, text or via duplicates it
- shift-dragging a symbol rotates (spins) it
- dragging a cline segment slides it

Similarly, in etch editing mode:

- dragging a cline segment slides it
- double-clicking a pin or via adds a connection (this can be shortened further to a single click with the contextual menu Customize > Enable Single Click Execution)

That should be enough for now!

C.2 Alternative design flow

If you don't like the idea of the new board wizard, you can follow a more conventional flow to start the board. It gives a little more control.

1. Send the netlist from Capture to PCB Editor *without* first setting up a bare board. Leave the Input Board File empty in the Create Netlist dialogue box, figure 4 on page 12. PCB Editor opens with your new board.

2. Use Setup > Outlines > Board Outline to define the outline of the board and the route and package keepins, which are made identical. The same dialogue box can be used to change these outlines later. You might wish to draw a different route keepin with Setup > Areas > Route Keepin.

   I have not tried placing the components first and subsequently drawing the board outline and keepins around them. You would obviously have to ignore DRC errors and could not use Quickplace.

3. Import a technology file with File > Import > Techfile if you have one. Otherwise, work through the steps below.

4. Use Setup > Cross-section to define the number, names and types of layers. The default is two layers, which is fine.

5. Set up the grids with Setup > Grids. I suggest 100 mil for the non-etch layers and 25 mil for the etch.

6. Define the widths of tracks with Setup > Constraints > Physical and the separations with Setup > Constraints > Spacing. Select the upper All Layers spreadsheet in the tree on the left to bring up a row labelled DEFAULT on the right. Values entered here propagate into all nets, where you can override them for power nets and the like. While you are doing this, edit the vias in the Physical pane as described on page 37.

7. You might wish to tweak some of the parameters in Setup > Design Parameters > Display, such as the display of drill holes and the ratsnest. Their visibility is treated differently from other elements of the design. You can also enlarge the DRC markers.

C.3 More approaches for placing components

In section 3.3 on page 17 I suggest that you place components on the board roughly in position using the Placement dialogue box, then rearrange and reorient them later. I think this is the simplest approach but you can also rotate and mirror components using the contextual menu while the Placement dialogue box is open. Curiously the command for rotation becomes Rotate rather than Spin.

OrCAD Capture 16.3 is better integrated with PCB Editor than in previous versions and provides another method to place components. Keep Capture open after you have sent the netlist to PCB Editor. Open the Placement dialogue box in PCB Editor as described in section 3.3 on page 17, as if you were going to place the components manually. Instead of selecting components from this dialogue box, return to Capture and select a component on your schematic. This component is automatically selected for placement and attached to the cursor in PCB Editor.

Communication between Capture and PCB Editor can also be used to identify components.

- If you select a component in Capture it becomes highlighted in PCB Editor. There is an item PCB Editor Select on the contextual menu in Capture but it appears to be redundant in version 16.3 – the highlighting happens automatically. (The opposite happens if the last command in PCB Editor was Dehighlight.)

- If you highlight a component in PCB Editor it is selected in Capture. Do this by selecting a component and choosing Highlight from the contextual menu (often on the Symbol submenu), or by selecting Display > Highlight from the menu bar and clicking on a component. (There used to be a 'sun' button on the toolbar for highlighting but it has vanished in version 16.3. The 'eclipsed sun' for dehighlighting is still there, though. Strange.)

These features require Intertool Communication (ITC) to be enabled in Capture. This is the default; check the Miscellaneous tab of the Preferences dialog box if it seems not to be working.

C.4 Design rules

The suggested design rules of 25 mil tracks with 25 mil separation do not permit a track to run between the pads of of an integrated circuit, $0.1''$ apart. This produces a board that is easy for inexperienced students to solder but makes it more difficult to route. If you wish to allow tracks between the pads, reduce the Minimum Line width to something like 15 mils in the New board wizard or Constraint Manager (the number depends on the spacing between your pads, of course). Remember to spread the wires after routing the board, which you will need to solder carefully! Mitzner [3] and Jones [3] offer useful advice on design rules and you should of course follow the guidance of your manufacturer.

Use the Constraint Manager to change the tracks and spacing for an existing design. Figure 13 on page 29 shows the Physical constraints, which means the widths of tracks. Select the upper All Layers spreadsheet in the tree on the left to bring up a row labelled DEFAULT on the right. Change the widths, which are copied into all nets. Similarly, choose Spacing and All Layers to adjust the spacings.

I should say a little more about the entries in the Constraint Manager shown in figure 13. Several widths can be specified.

- Under Line Width, the Min (minimum) figure is used as the default and is the value specified in the New board wizard.

- I have made the Max (maximum) width double the minimum value. This is useful for parts of tracks that carry a high current.

- Sometimes it is helpful to make a track narrower than its usual minimum width for a short distance, perhaps to pass between pads. This is called a *neck*, for which you specify a minimum width and maximum length. I have given a width of 12 mil, about half the usual, with a length of 250 mil or $\frac{1}{4}''$, which is plenty to squeeze between a pair of pins. I'll explain how to use this in section C.6 on page 56.

Many more constraints can be set: See *Creating Design Rules* for an introduction. Full details are in *Allegro Constraint Manager User Guide* and *Allegro Constraint Manager Reference*, which have unfortunately been omitted from the documentation distributed with version 16.3. When everything has been set up perfectly, use the command File > Export > Technology File to write the constraints to a tech (.tcf) file, which can be used to configure future designs. This can also be done from PCB Editor.

C.5 Disappearing ground and power nets

PCB Editor likes to hide the nets for power and ground signals when it draws the ratsnest. This is obviously beneficial if you use separate ground and power planes but is unhelpful for one or two-sided boards. Unfortunately it has several ways of hiding the nets, which require different techniques for making them visible again. You might hope that Display > Show Rats > All would do what it says but it does not! Here is the simplest method.

1. Choose Edit > Net Properties... to bring up the Constraint Manager, then Net and General Properties.
2. There is a column headed No Rat and the entry may be On in the rows for the power nets. Change them to (Clear).
3. Quit from the Constraint Manager and the nets should appear in the ratsnest.

If that doesn't work, or the apparently unconnected pins are shown with a boxed X (like a checkbox), here is the next method.

1. Choose Edit > Net Properties... to bring up the Constraint Manager, then Net and General Properties.
2. Delete any entries in the column headed Voltage. These are constant (DC) voltages and therefore indicate a power supply.
3. Quit from the Constraint Manager and the nets should appear in the ratsnest.

If that doesn't work either, here's my final method.

1. Select the missing nets. That sounds tricky but is not. Set the Find control panel for Nets, hover the mouse over one of the unconnected pins and its net is selected (and named on screen). The pins appear in the worldview window too when the net is selected.
2. Right-click and choose Property Edit. Two boxes appear: Edit Property and Show Properties.
3. The list on the right-hand side of the Edit Property box should include Ratsnest_Schedule and its value is probably POWER_AND_GROUND. Click the Delete check box to get rid of this property. If there is a Voltage property, delete that too.
4. Click Apply and the net should appear. Click OK to get rid of the Property Editor.

C.6 Manual routing

PCB Editor offers many features to assist manual routing and I described only the most basic in the walk-throughs. More information is in *Routing the Design* with details in the references for individual commands, particularly add connect (20 pages!) and slide.

- Two methods can be used to change the width of a track along its length. For a narrower *neck*, left-click where the width should reduce and choose Neck mode from the contextual menu. The width of the track is reduced to the value specified in the physical constraints (section C.4 on page 54). Click to mark the end of the neck and select Neck mode again to return to normal width. A DRC error is flagged if the neck is too long.

- More generally, click where the width should change and type a new value into the Line width box of the Options control panel. The drop-down menu offers recently used values. Alternatively, the width can be changed with the contextual menu.

- When you are close enough to the finishing point of a track (the *target*) that it can be drawn automatically, choose Finish from the contextual menu. PCB Editor completes the track for you.

- When you have drawn part of a track from one end, Target > Route from Target allows you to draw the rest from the other end, which is sometimes easier. Before doing this, check that PCB Editor has the same target as you – it may be aiming for another point on the same net. Use Target > New Target and click on your target if necessary.

- While routing, Options can be set with the control panel or most from Options > ... on the contextual menu.

- Immediately after selecting the Add Connect command, the Options control panel shows No available via. Don't worry, it will offer something more helpful as soon as you start a track. Different nets may use different vias, hence the lack of a default.

- Add a via by double-clicking or by left-clicking to mark the spot, then right-clicking and choosing Add Via. Check the the correct via and layers are shown in the Options panel.

- You may wish to adjust the setting of the Bubble option. Its default is Shove preferred, which pushes other tracks out of the way vigorously to create room for the new track being drawn. I prefer Hug only, which draws the new track as close to the old ones as the design rules permit, without moving anything. Hug preferred is intermediate.

C.7 Where's the missing track?

Sometimes Display > Status reports that one or more nets or connections is unrouted but it's not obvious on the screen. Click on the yellow button next to Unrouted connections, which produces an Unconnected Pins Report. (This is also available from the menu bar using Tools > Quick Reports > Unconnected Pins Report.) The name is slightly misleading because it reports *all* unrouted segments, not just those attached directly to pins. Each missing connection is listed with hyperlinks to the two ends. Click a link to centre the corresponding point on the screen, which should make the unrouted segment obvious. If you still can't see it, use the

Visibility or Options control panel to hide the etch and make the ratsnest more obvious. And if it's still not visible, set the Find panel for Nets and drag a small rectangle around the centre of the screen, which should highlight the offending net.

I have found that most elusive unconnected tracks are on pads. Usually the track has been drawn on to the pad but not all the way to its centre, often because the grid is too fine. Select the Connect tool, click on the existing track to extend it, right-click and choose Finish. This should complete the track to the pin. Alternatively, draw the track close to the pin, right-click and choose Snap pick to > Pin; this is handy for other targets, such as vias.

C.8 Pours or fills

It is easy to fill the unused areas of an etch layer with conductor to provide screening. This is called a *dynamic etch shape* in PCB Editor and the procedures are described in *Preparing the Layout*. A dynamic shape is automatically redrawn in response to changes in other elements, unlike a static shape whose outline is fixed. Thus the filled area of a dynamic shape reflows around tracks and pads if they are moved.

Solid fill

I have used the one-transistor amplifier as an example, starting with the finished design at the end of section 3 on page 14. Figure 31 on the following page shows the PCB with a solid fill attached to the ground net. I'll make it cross-hatched later (not necessarily a good idea).

If you have routed the board already, it is best to unroute the ground net before adding the shape or you get both the tracks and the fill. Alternatively, hide the ratsnest for the net before routing. Follow the opposite procedure to one of those described in section C.5 on page 55; the simplest is to add a voltage to the Net Properties. This hides the net and shows the pins with a boxed X as a reminder that they are connected to a hidden power net.

1. Choose Shape > Global Dynamic Params... from the menu bar to set up the parameters first. There are several tabs.

   - Shape fill – increase the Line width and Spacing from 5 to 25 mils, consistent with the coarse design rules followed in this tutorial. The Border width becomes 25 automatically. I used the default Hori_Vert fill style.
   - Void controls – check the artwork format.
   - Clearances – increased to 25 mils.

2. Select Shape > Rectangular from the menu bar or click the Shape Add Rect button (shape add rect command).

   This is *not* the same as Add > Rectangle or the Add Rect button (add rect command), which produces an unfilled rectangle. Nor is it the same as Add > Frectangle (add frect command), which produces a *static*, filled shape.

3. Check the settings in the Options panel. The shape should be in the Bottom Etch layer and the fill should be Dynamic Copper. Select the name of the net to which the shape should be connected by clicking on the '...' button and choosing Gnd or whatever it is called. (Leave the net as Dummy Net if you don't want it connected to anything.)

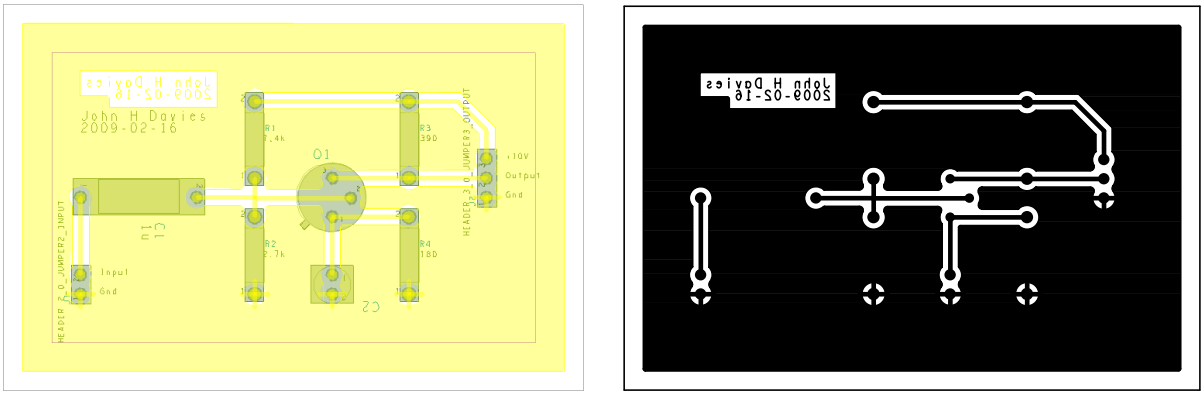


Figure 31. Screenshot and photomask for the one-transistor amplifier with a solid dynamic shape attached to the ground net. Pins are connected to the shape through thermal-relief pads.

4. Draw a large rectangle to include the whole board. It is automatically trimmed to the route keepin and PCB Editor creates spaces (voids) around the pins, tracks and text.

That's it! A screenshot of the filled board is shown in figure 31 and I plotted the photomask in the usual way. An empty area called an *antipad* is left around pins of nets that are not connected to the fill. You might have expected that grounded pins would be surrounded immediately by fill but instead each pin has a *thermal relief* around it. This is an empty region crossed by a few lines of etch to provide electrical contact.

Thermal reliefs are needed because copper conducts heat as well as electricity. A pin surrounded by a large area of etch therefore cools more quickly after it has been soldered than one that has only a pad and a track. All pins must cool at a similar rate to give consistent joints if the board is soldered automatically so thermal reliefs are used whenever pins are connected to planes of etch rather than tracks. Maxfield [2] and Mitzner [1] explain this clearly. It isn't such an issue when boards are soldered by hand; in fact the usual problem is overheating of small pads.

Some versions of PCB Editor do not plot the fill in solid black, in which case a satisfactory photomask cannot be produced. You must use crosshatch fill in this case.

Crosshatch fill

PCB Editor lets you create a solid shape with either static or dynamic fill but a cross-hatched shape must be created as static. This means that you must first create a dynamic shape with solid fill and change it to crosshatched. Be aware that many manufacturers recommend that fills should be solid rather than cross-hatched.

1. Choose Shape > Select Shape or Void from the menu bar or click the Shape Select button and select the desired shape.

2. Right-click and choose Parameters... from the contextual menu. Select the Shape fill tab and change the Fill style to Xhatch. Other parameters are inherited from the global dynamic parameters that you set up earlier.

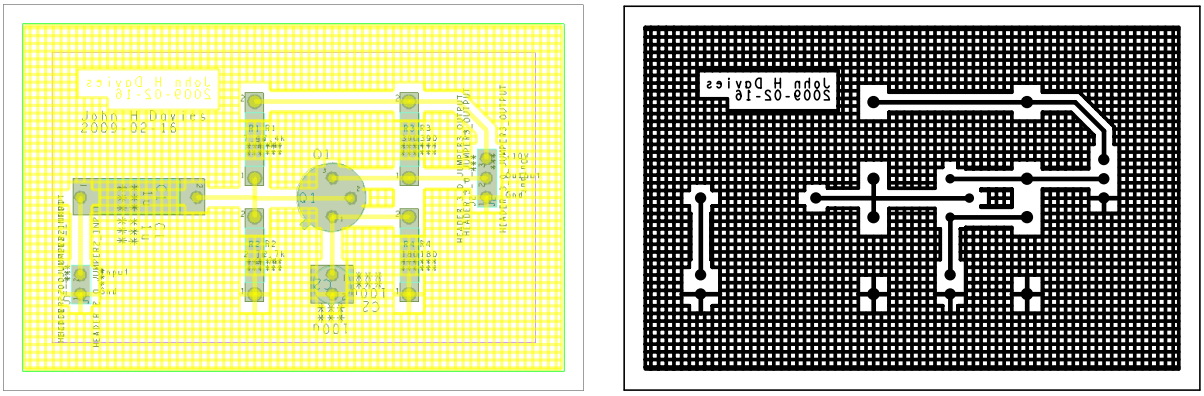


Figure 32. Screenshot and photomask for the one-transistor amplifier with a hatched shape attached to the ground net.

Figure 32 shows a screenshot and photomask for a hori_vert fill. An island has appeared to the right of the transistor, which is a poor feature. It can be removed with Shape > Delete Islands.

Mitzner [1] describes more advanced techniques of handling planes, such as splitting a ground plane into regions for analogue and digital signals.

C.9 Copying the names of pins from Capture to PCB Editor

In section 2.3 I ask you to label the pins of the connectors on the schematic drawing, as in figure 2 on page 7. Later, in section 3.6, I tell you to write the same text to label the pins on the PCB, as in figure 9 on page 21. This is a poor procedure because the two sets of labels might be inconsistent. It would be far more reliable if the names were copied automatically from Capture to PCB Editor. This can be done but is not as straightforward as it might be. These instructions are based on advice from Joewi, Bill Dempsey, tltoth and oldmouldy in threads 10494 and 10835 on the Cadence PCB Design Forum.

1. In Capture, select the components whose pins are to be named. Open the Property Editor and choose the Pins sheet.

2. Click New Row... (or New Column...) to create a new property and give it an appropriate name, such as SSNAME (for silkscreen name).

3. Enter names for each pin into the row for SSNAME. Make the property visible with Display... so that it shows on the schematic.

4. Two steps are needed in the Setup dialog box (figure 4 on page 12) for netlisting the design and sending it to PCB Editor. First, the easy one: Activate the checkbox for Allow User Defined Property.

5. Click on the Setup... button across from Create PCB Editor Netlist. The dialog box shows the Configuration File, called allegro.cfg. We need to Edit... this.

    - Add the line SSNAME=YES to the section for [pinprops] at the end of the file, which tells the netlister to include this property in the netlist.

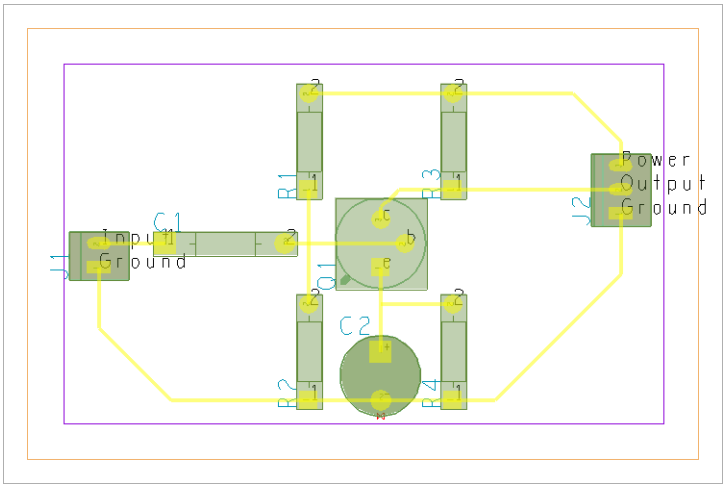


Figure 33. Board for one-transistor amplifier with all pins named.

- Save the edited configuration file in a different location, such as the allegro directory for the current project, or give it a different name in the default location. Do not overwrite the supplied file (even if you have permission).
- Still in the Setup dialog box, use the '. . . ' button to select the edited configuration file.

6. Run the netlister, wait for PCB Editor to open the board and place the components as usual. SSNAME is not yet visible.

7. Choose Display > Property. . . from the menu bar and select the Graphics tab. Scroll down the list of Available Properties and click on our added property, whose name has probably changed to Ssname. SSNAME appears under Selected Properties. Increase the Text block from its default of 1, which is tiny. The drop-down list for Subclass contains only the single entry PROPERTIES, which is part of the Manufacturing class. Click Create and the SSNAME text appears on the drawing. It can be moved and rotated in the usual way.

Whew! A slightly simpler alternative is to use Name, which is a standard property of a pin. Follow exactly the same procedure except that you do not need to define the new property. Curiously, you must still select Allow User Defined Property even though it was not defined by the user. The snag is that the name is now shown for *every* pin, which can clutter the board – see figure 33.

C.10 Controlling the display of text and other elements in PCB Editor

The footprints supplied with PCB Editor contain a great deal of text. This clutters the screen, as shown in figure 7 on page 18 for the one-transistor amplifier. Four items (classes) are displayed:

- **ref des**, such as C1
- **component value**, such as 1u

- **tolerance**, to which I did not assign a value and therefore appears as ***
- **user part number**, which I did not use either

The device type is shown for components that do not have a value, such as the jumpers. Two subclasses are shown for each of these:

- **silkscreen_top**, which is merged with the silkscreen_top subclasses from other classes to produce the complete top silkscreen by running the Auto Silkscreen command.
- **assembly_top**

I suggest that you hide the tolerance and user part number (unless you use them, of course) and keep only the silkscreen_top subclass visible. Here are two ways of doing this.

Options control panel

Pin the Options control panel open.

1. Set the active class to Tolerance/Assembly_Top
2. Click the colour swatch to the left of the drop-down list of subclasses. It turns black to show that this subclass is now hidden and the corresponding text disappears from the drawing.
3. Repeat this for the Silkscreen_Top subclass.
4. Repeat these steps for all the other classes and subclasses to be hidden.

Color Dialog

Open the Color Dialog with Display > Color/Visibility. . . .

1. Select the Components folder in the list on the left.
2. Click the All check box for the Assembly_Top row twice: the first click turns on the visibility for all subclasses and the second clears them all.
3. Do the same for the Tol. and UserPart columns to turn all of them off.
4. Click Apply or OK to update the drawing.

It is a good idea to save the colour settings when you have turned off unwanted elements. Use View > Color View Save from the menu bar (colorview create command) to save the current settings to a file. Its name appears in the list of Views in the Visibility control panel in the same way as the artwork films.

The same methods can be used to hide other unwanted classes, such as the individual silkscreens after the composite silkscreen has been created.

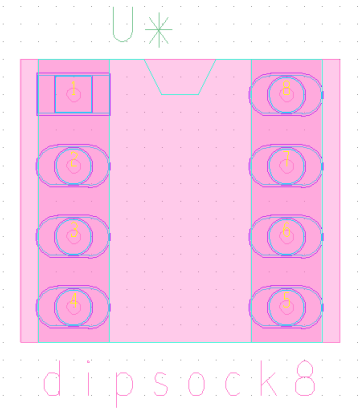


Figure 34. Package symbol (footprint) for a DIP8 in a socket.

C.11 Creation of package symbols (footprints)

It is straightforward to create a new package symbol (footprint) in PCB Editor and the procedure is clearly described in *Defining and Developing Libraries*. Two files are associated with each symbol.

- The **drawing** (.dra) file is used to create and edit the symbol with PCB Editor in its symbol mode. This offers a slightly different set of menus and toolbars from the usual layout mode. For example, the menu bar gains Layout while losing others, such as Route.
- The **package symbol** (.psm) contains additional information, such as a place-bound rectangle. It should be stored in a library, where it can be found when the symbol is placed on a new board. PCB Editor compiles the symbol automatically whenever you save the drawing, contrary to statments in some of the manuals.

Other types of symbol include mechanical symbols (.bsm) for features such as mounting holes.

Here is a quick guide to creating a minimal package symbol for a pin-through-hole component. Figure 34 shows the result with a few embellishments. I recommend placing the pins with the Package Symbol Wizard; it is easy to get the origin wrong if you add pins by hand.

1. First identify or create the padstacks needed.
2. Run the Package Symbol Wizard, most of which is fairly obvious. Choose the symbol origin to be at Pin 1 for a pin-through-hole component to ensure that the pins line up with a 100 mil grid when the component is placed.

   The wizard creates numerous elements in the drawing that may be superfluous. I often delete everything except the pins and the refdes on the top silkscreen.
3. If you prefer to place the pins yourself, choose Layout > Pins from the menu bar. In the Options control panel, choose the padstack for pin 1 by clicking on the "..." button. Place this pin at the origin, either by clicking at the correct point or (more reliably) by clicking on the P (pick) button, typing "0 0" (zero space zero) and clicking Pick.

Choose the padstack for the remaining pins in the same way. You can either place them manually (a 100 mil grid helps) or use the Quantity settings to place several at once. Right-click and choose Done when all pins are placed.

4. Draw the outline of the body of the component on Package Geometry/Assembly_Top. (The wizard produces a plain rectangle but a DIP should have a notch to mark the end with pin 1.) Reduce the grid spacing to 25 mil.

   Use Add > Line for the drawing; it is really a polygon tool because each click adds a segment to the end of the previous line. Zero width is fine. I have found it better to use the line tool even if the outline is a rectangle. Add any further features desired, such as a + sign for a polarized component.

5. Copy the outline on to Package Geometry/Silkscreen_Top as follows. Make sure that no elements are selected, then choose Edit > Copy. Set the Options for only lines, then drag a rectangle around the objects that you have drawn to select them all. Click on the original to pick them up, then click again to place a copy well clear of the original. Right-click and choose Done. Now drag a rectangle around the copy to select it all, right-click and choose Change to Layer > Silkscreen_Top (alternatively use Edit > Change). Finally, choose Edit > Move, drag a rectangle around the copy to select it, click to pick it up and click again to drop it over the original. Choose Done.

6. Add text to show the value of the component. Use the special command Layout > Labels > Value and choose the Silkscreen_Top subclass. Text block 3 is a suitable size. (Alternatively, the usual Add > Text command seems to do exactly the same.)

   The text is replaced by the value of the component when it is used on a board so I type the name of the symbol into this field. This is helpful if you place your new symbols into an empty board drawing to make a catalogue of your library (something that was handled *much* better in Layout).

7. Repeat this for the Refdes if you did not use the Package Symbol Wizard, which adds this automatically. Enter a placeholder such as U* for an IC.

The symbol in figure 34 on the preceding page contains a few extra features. It is intended for a dual-in-line IC mounted in a socket on a board without plated-through holes.

- The outline (cyan) shows the socket as well as the DIP8 IC itself.
- A rectangular route keepout (magenta) surrounds each row of pins. This prevents tracks running to the top pads of the pins, where they cannot be soldered because the socket is in the way. Use Add > Frectangle and set the active class to Route Keepout/Top. In fact you can use Add > Rectangle or the Add Rect button, which are officially for unfilled rectangles, but PCB Editor creates filled rectangles automatically where appropriate. For a more complicated shape use Shape > Polygon. The Options default to the type Static solid, which is appropriate.
- Another rectangle for Via Keepout/All surrounds the whole symbol. This excludes hand-soldered vias where they would obstruct the socket.

- The padstacks have smaller pads on the top than the bottom because no tracks should run to the top; the top pads are markers only.

The completed symbol should be stored where PCB Editor can find it. Use the design's allegro folder if the symbol is needed only once, but symbols are normally kept in in a library to make them generally available. The default location for a local symbol library on my computer is

- C:/OrCAD/OrCAD_16.3/share/local/pcb/symbols/

Folders at the same level hold padstacks and tech files; a README.TXT file explains what should go where. PCB Editor searches these directories automatically but must be told where to look if you store the libraries elsewhere. Open the User Preferences Editor with Setup > User Preferences... (enved command) and choose Paths/Library in Categories. Click on the ... button for psmpath to open its list of items, add your directory to the system default ($psmpath) and move your directory to the top so that it is searched first. Do the same for padpath if you have created padstacks as well.

C.12 Miscellaneous tips

- PCB Editor seems to have no Unroute Board command, which would be helpful if you made a complete mess of routing. One method is to reload the design, assuming that you saved it first. Alternatively, do this.

  1. Select Nets only in the Find control panel.
  2. Drag across the design to select all the nets.
  3. All the nets are now highlighted in the design window. Right-click and Ripup etch.

- The conversion of libraries from Layout is described under the orcad in command in *O Commands*. Names of symbols are highly restricted in PCB Editor so you may find that you have to rename all your footprints (sigh...). I found the conversion generally reliable but the text for values vanished and a few symbols acquired DRC errors.

- It would be convenient if the schematic circuit could be drawn once with both 'virtual components' such as sources for simulation and sockets for the real PCB. Unfortunately this cannot be done without editing the components in the pspice library because some have pins numbered 0, which allegro rejects. Many of the libraries are full of bugs. Some components have pins 'numbered' with letters (such as the electrolytic capacitor) and some aren't numbered at all. Avoid the libraries in oldlibs (as you might expect but students find them strangely attractive).

- I find it helpful to adjust the grids provided by the new board wizard, which are the same for everything. Choose Setup > Grids... from the menu bar. I suggest spacings of 100 for Non-Etch (essentially the components) and 25 for etch. If you enter a value for All Etch it is copied to all etch layers, which saves some typing.

- Lines in the ratsnest are 'jogged' by default. If you prefer to join the components with straight lines instead, choose Setup > Design Parameters... from the menu to bring up the Design Parameter Editor. Select the Display tab and adjust the Ratsnest geometry to Straight.

- Two types of 'design' file both use the extension .dsn but have entirely different contents.
  - Capture has a design file to hold its database (Windows calls it a Data Source Name)
  - PCB Editor uses a design file to export the board to the autorouter.

  Don't mix them up! This is one reason for setting up a separate allegro directory.

- There is a high chance of error if you copy names of footprints from a document and type them manually: It is better practice to select them from a library. Unfortunately this is clumsy in PCB Editor.

  1. Choose Place > Manually... from the menu bar.
  2. Click the Advanced Settings tab and choose to Display definitions from Library.
  3. Return to the Placement List and select Package symbols from the drop-down list. You now see a list of all packages in the libraries.
  4. Scroll down to find the outline that you want, res400 for example. Click in the check box next to the component and a graphic appears in the Quickview window. This helps you to confirm that it is the correct outline, although there is no scale.
  5. Select the Text radio button and the name of the component appears. You can copy this and paste it into the Properties Editor in Capture.
  6. Dismiss the Placement box with Cancel when you have finished and quit from PCB Editor without saving any changes.

  A listing of the directory might be easier! Layout was *much* better.

D PCB Router techniques

Tracks can be edited in PCB Router instead of PCB Editor. This is handy for moving badly-placed vias; I found it easier than PCB Editor. Right-click in the window, which brings up the INTERACTIVE ROUTING MENU. Move mode is probably the most useful. You can then select tracks or vias and move them. Do this before the finishing touches of spreading and mitring. In fact you can do most of the placement in PCB Router as well as the routing but I didn't want to describe yet another interface.

If you export a fully or partly routed board from PCB Editor to PCB Router, the imported tracks are protected against changes in PCB Router. Choose Edit > [Un]protect > Wires by Net... (or Wires by Layer List...) to remove the protection. You can then unroute these tracks and reroute the board.

E Plots with open drill holes

If your PCB is drilled by hand, rather than with a CNC machine, it is helpful to leave holes in the middle of each pad to guide the drill. Several approaches can be taken, depending on exactly what you want. Full-size holes are easier but provide a poor guide to the tip of the drill. A smaller hole is better and my technicians recommend 20 mils, compared with the full diameter of typically 30–40 mils. The small hole in the pad acts rather like a centrepunch.

- **Drill holes at full size** are easy in version 16.3 because an option has been added to plot them. You are out of luck with earlier versions.
- **Small holes to guide the drill** are harder: You must edit the padstacks. This works in earlier versions as well. There are two options:
  - Reduce the size of the drill hole to act as a guide rather than show the true diameter of the hole. This is easier but ruins the padstack for automatic drilling.
  - Add an extra layer to the padstack to show the guide hole. This can be the pastemask in version 16.0 because it is unlikely to be required for boards that are drilled by hand. A further layer, the filmmask, has been added in version 16.3 and is a better choice because it has no predefined function.

I'll explain these three methods in detail.

E.1 Full-size drill holes using standard padstacks

No modification is needed to the padstacks but a few more steps must be added to the procedure in section 6.1 on page 39 to plot the photomasks. First, make the drill holes visible before opening the Color Dialog.

1. Open the Design Parameter Editor with Setup > Design Parameters... from the menu bar and bring the Display tab to the front if it is not shown automatically.
2. Select the checkboxes against Display plated holes and Display non-plated holes. (Display padless holes is automatically selected as well.)
3. Leave everything else alone and click OK to confirm the changes. Your board should now show a black circle for the hole in the middle of each pad.

These holes must be made white so that the pads appear open on the plot. This requires another manipulation with the Color Dialog.

1. While the Display folder is active to change the background of the window, change the colour of Drill holes to white in the same way.
2. After the etch has been coloured black, the pads should show white drill holes as desired.
3. Check in the Plot Setup that the Plot method is Color. (Yes, I know that we want only black and white but this is essential!)

The plot should now show drill holes open, larger than those in figure 24 on page 41 which were reduced as described in the following sections.

Note. The Plot method in Plot Setup *must* be Color to leave drill holes open, even though the image is black and white. If you plot in Black and white, the drill holes are printed black and do not show up! ❦

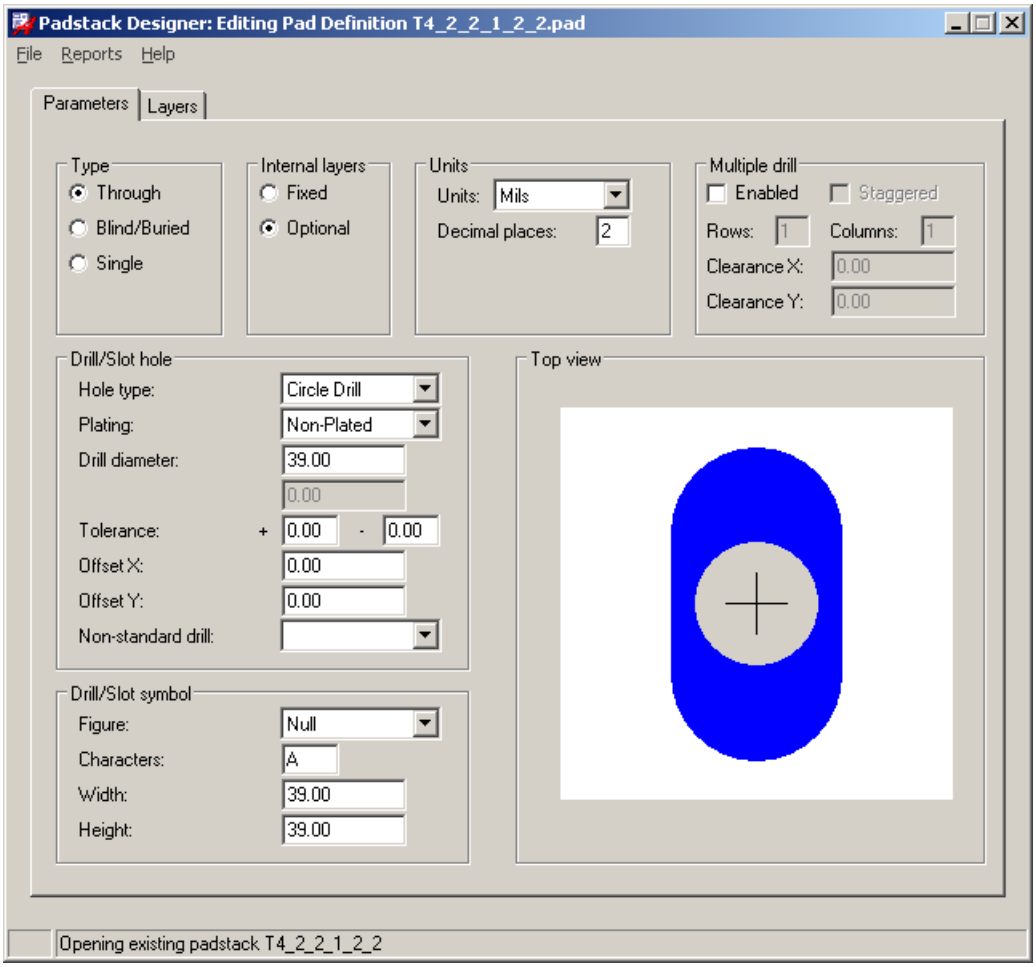


Figure 35. Parameters tab of the Padstack Designer to edit the Drill diameter.

E.2 Modified padstacks with narrow drill holes

You must edit all padstacks in both this method and the following one. This can be done for a design but it would be unacceptably tedious to do it every time. Unless you need to do this only once, you should edit the padstacks in your library. Make a copy of the original padstacks first! They should be in a folder called padstacks (what a surprise! – but curiously the padstacks of the Cadence library are in the same folder as the symbols). Each padstack has a separate file with extension .pad. See *Library Padstacks* in *Defining and Developing Libraries*, *Layout Padstacks, Vias, and Etch Shapes* in *Preparing the Layout*, and *Padstack Designer* in *P Commands* for full details of the Padstack Designer. The name of its window varies slightly, depending on whether it was started in standalone mode or from PCB Editor.

Run the Pad Designer from the Start menu (it is in a subfolder OrCAD PCB Editor Utilities) and open a padstack with the File menu. You should see a window similar to figure 35; click the Parameters tab if it is behind the Layers tab. Change the Drill diameter to 20 mils or the value recommended by your technician and choose File > Save. Carry on and do all of the padstacks that you need... you might wish to learn how to write scripts!

The procedure is very similar if you wish to modify the padstacks of a design. *This does*

not affect the library because the board file contains a copy of each padstack used. Choose Tools > Padstack > Modify Design Padstack... and open the Options control panel, which shows a list of padstacks in the design. You have a choice of editing an Instance, which means the padstack for a single pin, or Definition, which means all copies of a particular padstack in the design. Select one of these and click the Edit... button. The Padstack Designer opens and works in the same way as before.

Alternatively, right-click on a pin (which must be active in the Find control panel) and choose Modify Design Padstack > All instances. This does exactly the same.

If you have edited the library and want to apply the changes to an existing design, open it with PCB Editor and choose Tools > Padstack > Refresh.... This replaces the board file's copy of the padstacks with fresh versions from the library. Further commands replace padstacks and purge unused padstacks from a design.

Plot the design with drill holes open as explained in the previous section (E.1).

E.3 Modified padstacks with filmmask (or pastemask)

This approach is slightly more complicated because you must edit the padstacks and do a bit more with the Color Dialog when plotting the design. The advantage is that the padstacks retain drill holes at full size, which allows you to produce correct excellon files for a CNC drill.

Edit the padstacks to include guide holes for drilling

Here's how to fix the padstacks so that they can be plotted with a guide hole for drilling. The trick is to use the pastemask or filmmask layer for the guide hole. I'm grateful to Bill Dempsey and other contributors to the Cadence forum for help with this. The illustrations are for version 16.0, where you must use the pastemask, but I recommend the filmmask instead in version 16.3.

Open a padstack to edit as described above in section E.2 and make the Layers tab active as in figure 36 on the following page. The rows for the pastemasks are probably blank. Click on PASTEMASK_TOP to edit it. In the group below for Regular Pad, choose the Geometry to be Circle and the Width to be 20. Repeat this for PASTEMASK_BOTTOM. These layers now have small circles that become the guide holes in the final plot. The other layers can be left unchanged. Save the pad and do the rest of them.

Display the filmmask or pastemask on the plot

Two further steps are required in addition to those listed in section 6.1 on page 39.

1. While you have the Color Dialog open to edit the Stack-Up, click the checkbox in the All column of the filmmask or pastemask layers to activate them and change their colour to white. See figure 23 on page 40.

2. After you have closed the Color Dialog, the masks will probably not appear on the screen because they are 'under' the etch. Go to the Options control panel, choose the Pin class and the subclass with the drill guides for the current layer, Pastemask_Bottom for example. This activates the subclass and draws it on top of everything else. Pale holes appear on the pads as desired.

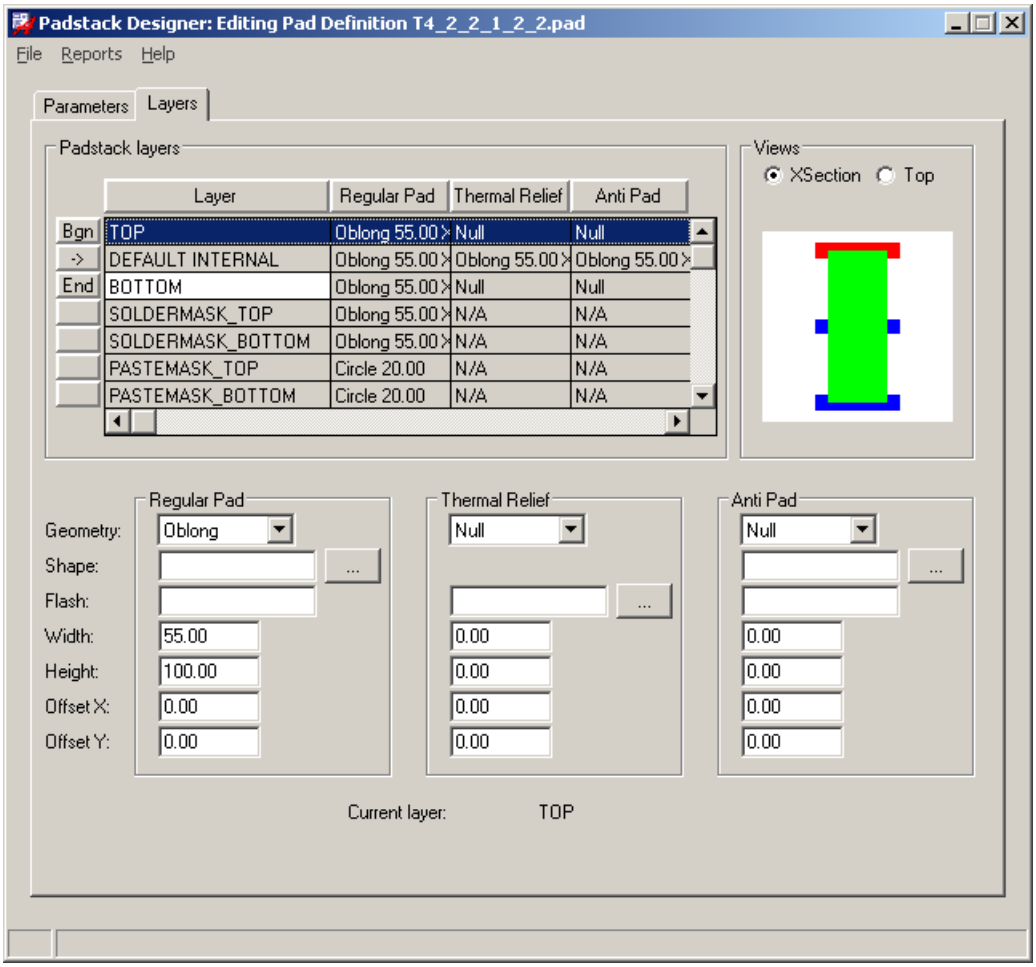


Figure 36. Layers tab of the Padstack Designer settings with pastemasks to act as a dummy hole.

3. Plot the design, ensuring that the Plot method is Color.

You should see something like figure 24 on page 41, which was produced in this way. Whew!

References

[1] Kraig Mitzner, *Complete PCB Design using OrCAD Capture and PCB Editor*, Newnes (Elsevier), 2009, ISBN 9780750689717, about £40. This covers PCB Designer in far more detail than this tutorial including many advanced techniques that I haven't mentioned including split planes and gate swapping. It also includes general aspects of PCB design, not just OrCAD. Highly recommended. (I might not have written these notes if Mitzner's book had been available at the time.)

[2] Clive Maxfield, *Bebop to the Boolean Boogie: An unconventional guide to electronics*, 3rd edition, Newnes, 2009, ISBN 9781856175074. You might not guess from its title but this includes a wide-ranging description of modern components and construction including PCBs. It's an entertaining read as well.

[3] David L Jones, *PCB Design Tutorial*, www.alternatezone.com. This is a good, practical guide to the design and manufacture of PCBs but not specific to OrCAD. The comments on CAD software are a little out of date but it is full of real-world advice.