HSPICE

The Gold Standard for Accurate Circuit Simulation

Overview

HSPICE® is the industry's "gold standard" for accurate circuit simulation and offers foundry-certified MOS device models with state-of-the-art simulation and analysis algorithms. With extensive usage in analog/RF/mixed-signal IC design, cell and memory characterization, and chip/package/ board/backplane signal integrity simulation, HSPICE is the industry's most popular, trusted and comprehensive circuit simulator.

Foundry-Certified Models

Device models are the ingredients for accurate circuit simulation. HSPICE is consistently first to provide new advanced device models and HSPICE models are first to be foundry-certified. Over the years, HSPICE has consistently engineered leading-edge modeling technology for advanced node CMOS, FinFET and FDSOI processes that ensures the most advanced and accurate set of industry-standard device-model implementations. Synopsys collaborates closely with leading commercial and proprietary foundries to ensure that their HSPICE model parameters are timely and accurately validated to their fabrication process. The comprehensive set of HSPICE models have been extensively proven over the broadest set of semiconductor technologies, ranging from the Compact Modeling Council (CMC) standardized models (BSIM, PSP, HiSIM, etc.) on the latest technology nodes to proprietary models (HVMOS, TFT, etc.) for specialized applications (high voltage, display, etc.). See www.HSPICE.com for an up-to-date list of device models supported in HSPICE.

Triple DES Encryption

HSPICE offers robust 192-bit encryption compliant with Triple Data Encryption Standards (DES). This feature enables users to distribute their HSPICE custom netlists and models without revealing sensitive information. Third-party recipients of encrypted HSPICE netlists can run simulations with but cannot print encrypted parameters or internal node voltages. The third-party user simulating the encrypted netlist sees devices and circuits as black boxes, which provide only terminal functions. This enables netlist providers to keep their propriety models and designs confidential while allowing third-parties to perform transistor accurate simulations without changing their flows.

Analog/RF/Mixed-signal IC Design

Runtime Performance - Single and Multicore simulation

HSPICE's simulation accuracy, "out of the box" convergence, and runtime performance across all circuit types continue to be the number one focus of the HSPICE R&D team. Release to release, Synopsys R&D improves HSPICE's runtime performance without sacrificing accuracy. Over the last 2 years, HSPICE's runtime performance on one core has improved, on average, over 5X on large pre and post layout analog, mixed-signal, and memory designs. In addition, HSPICE deliverers superior multi-core scalability with an average of additional 8X speed up on 16 cores.

Integration with Synopsys Custom Compiler™ and Custom WaveView™

Synopsys Custom Compiler provides Analog, RF, and mixed-signal designers with a front-to-back, schematic-to-layout, modern era design cockpit with full HSPICE support. Please see: www.Synopsys.com > Silicon Design & Verification > Custom Design.

Verilog-A Behavioral Modeling

Verilog-A has been shown to be an ideal language for describing analog circuit behavior and complicated test bench input stimuli. Using HSPICE's compiled LRM 2.4 compliant Verilog-A simulation, users can mix transistor level and Verilog-A behavioral descriptions in the same netlists and improve runtime performance.

Reliability Aware Verification - Process Variability and MOSRA Device Reliability Analysis

Sophisticated analyses such as HSPICE MOSRA, worst case corners, Monte Carlo, ACMatch, and DCMatch allow a user to optimize a circuit that satisfies the design constraints across various processes, voltages, temperature ranges and device ages. In addition to device process variation, HSPICE and StarRC together can support interconnect variation. HSPICE not only reports the effect of variation on yield but also identifies the critical yield limiting devices and parameters. HSPICE design for yield features include:

- Corner Case Analysis: HSPICE can easily explore process corners and operating conditions for a design in order to analyze its yield, power, and performance
- Smart Monte Carlo sampling: Latin Hypercube sampling and Low Discrepancy Sequences for efficient and accurate yield analysis
- Sigma Amplification: increases process variation in SPICE model by a scale factor to cover high σ variation analysis with fewer samples and faster turn-around time. Ideal for large mixed-signal IP robustness validation
- ACMatch and DCMatch: for analyzing parameter mismatch effects due to local variation
- Variation Block: powerful and flexible mechanism for defining process variation effects
- MOSRA device reliability analysis: simulate HCI and NBTI device aging effects

Loop Stability Analysis

HSPICE's loop stability analysis enables users to analyze loop gain and phase characteristics on feedback circuits in frequency domain.

Transient Noise Analysis

HSPICE's transient noise analysis enables users to predict the effects of device noise (channel, thermal, flicker, and shot noise) on time domain waveforms. Transient noise analysis can be used to characterize phase noise and jitter for PLL applications.

Multi-sample Monte Carlo samples generate an ensemble of noise stimulated waveforms for statistical evaluation. HSPICE supports noise bandwidth and scaling controls and enables the user to plot histograms of the simulation results.

Large Signal Periodic Steady-State Analysis

HSPICE can perform key large signal analyses including periodic steady-state (PSS) analysis, periodic noise and phase-noise analysis, and periodic AC analysis and much more using either the Shooting Newton (SN) engine (for strongly non-linear circuits) or the Harmonic Balance (HB) engine (for weakly non-linear circuits). HSPICE can quickly and accurately simulate large non-linear, high-frequency designs. With a complete array of specialized analyses, HSPICE is the clear choice for both traditional RFIC applications and high-frequency phase noise and jitter analysis.

Cell and Memory Characterization

HSPICE is ideal for performing accurate cell and memory characterization and provides versatile waveform measurement functions based on simulation data. A data-driven parameter sweep automates characterization by simultaneously varying parameters to conveniently handle hundreds of HSPICE simulations parameters.

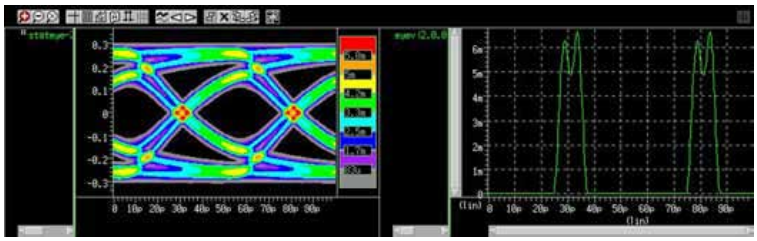

Figure 1: HSPICE StatEye Displayed in Custom WaveView

Improved Performance

HSPICE has significantly enhanced its performance (read-in, simulation, and total throughput) while maintaining the same high level of accuracy. The improved simulation performance is achieved by an enhanced time-step control algorithm, combined with a simplified simulation control interface. The user can scale simulation options simultaneously using a single control option eliminating the need for users to adjust multiple option settings. HSPICE automatically adjusts each time-step size and other simulation options to meet the desired accuracy level.

Improved Integration

HSPICE's client server mode option enables users to speed up simulation and total turnaround time. When running HSPICE with the client server mode option, HSPICE shortens total turnaround time by minimizing the re-reading of models and netlists and minimizing the number of license check-ins and check-outs. With improved performance and integrations with cell and memory characterization environments, HSPICE can quickly and easily explore multiple process corners and operating conditions across large cell and memory libraries.

Chip/Package/Board/Backplane Signal Integrity (SI) Simulation

Advanced Elements and Sources

As chip and board speeds continue to increase, new design and verification challenges emerge. HSPICE reveals signal integrity problems caused by jitter, crosstalk, ringing, ground bounce, and other noise sources. With extensive model and element support, HSPICE is the only simulator that can satisfy your silicon-to-package-to-board-to-backplane SI simulation needs.

Statistical Eye Diagram Analysis (with IBIS AMI)

With HSPICE's new StatEye analysis, designers can accurately simulate bit error rate measurements in a single simulation and display bathtub plots in what used to require a million transient simulations to attain the same coverage. For accurate modeling of SERDES equalizers, HSPICE's StatEye supports the Algorithm Modeling Interface (AMI), part of the IBIS 6.0 specification.

S-element

Users can readily create accurate S-parameter models based on direct measurements from a network analyzer or the solutions of a field solver. HSPICE supports S-parameter models with an arbitrary number of differential and single-ended ports. HSPICE's recursive convolution algorithm can quickly and accurately simulate S-parameters with over 1000 ports for large packages and other applications. HSPICE provides for S-parameter extraction directly using the .LIN command, resulting in more accurate, detailed measurements.

W-element

By handling dielectric loss, HSPICE's W-element can accurately simulate 50-inch, 50-GHz transmission lines. In addition, S-parameters can be incorporated in the W-element for interconnect simulation.

More Sources, Elements and Models

HSPICE supports pseudo-random and bit-pattern sources, E & G elements, IBIS models and much more for all your SI simulation needs.

Operating Systems

- Redhat Enterprise Linux v6.6-6.8, v7.1-7.3
- SUSE Linux 11-SP4, 12, 12-SP2
- Windows 7, 10, Server 2016