Integrated Circuits Electronic Design Automation

Dobromir Gaydazhiev,
GLOBALFOUNDRIES

Scope

- The Design Cycle and Process Design Kit (PDK) Modules
  - Models
  - Parametric Cells (Pcell)
  - Design Rule Checking (DRC)
  - Layout vs Schematic (LVS)
  - Layout Parasitic Extraction (LPE/PEX)
- PCB vs. IC
- IC technology classification

Design Cycle and Process Design Kit (PDK) Modules

Feasibility study & Specification Creation

Circuit Design & Circuit Simulation

Layout Design & Layout Verification

DRC

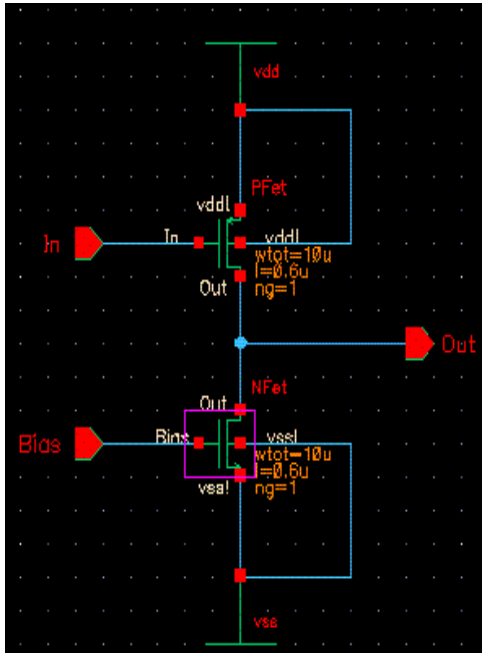
LVS

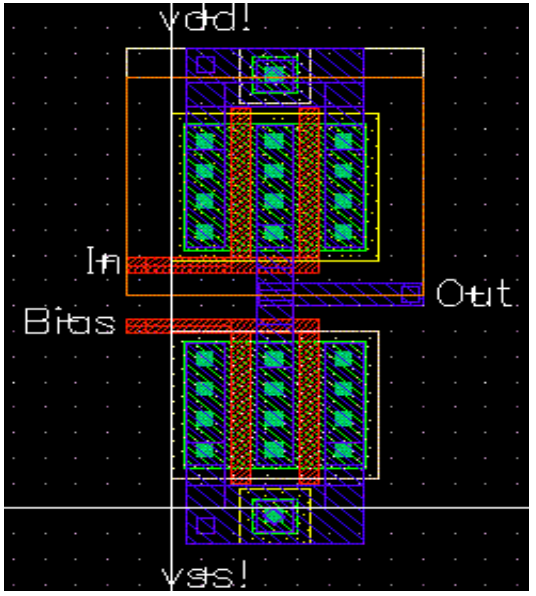
PEX/SI

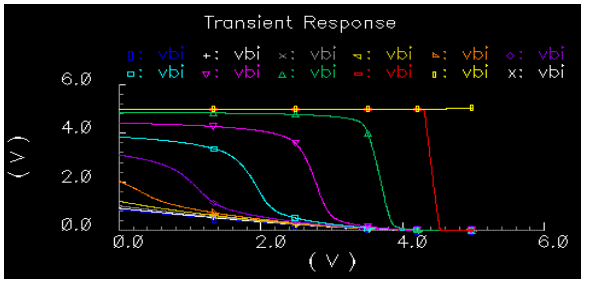
Design for Test
Design for Manufacturability

Masks preparation
Prototype Fabrication
& Test

Production







Device Models

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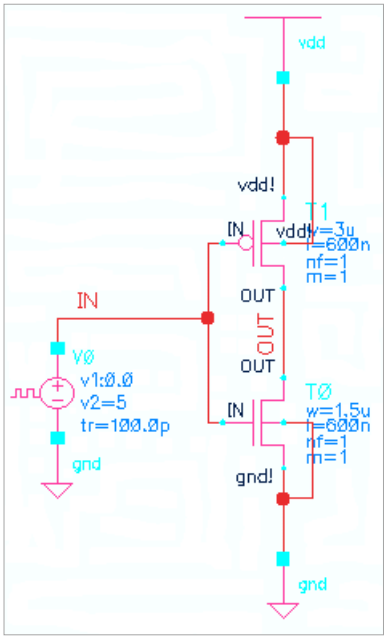
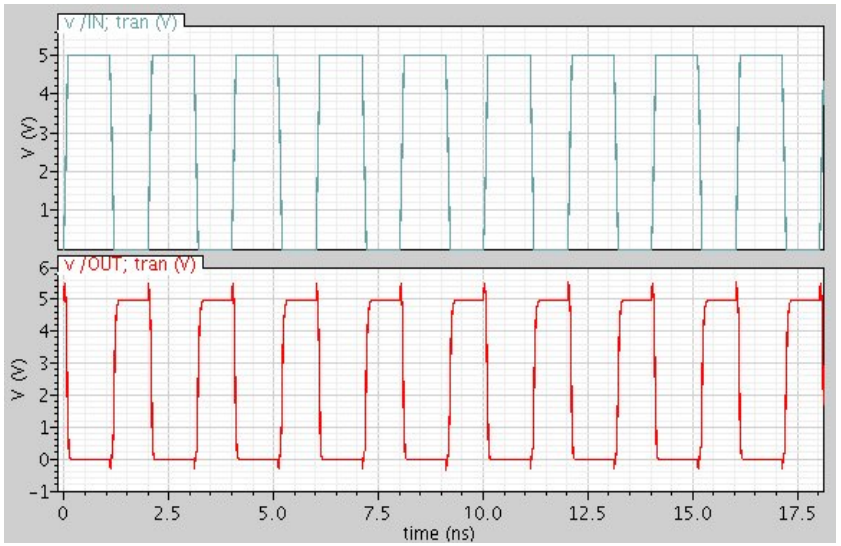
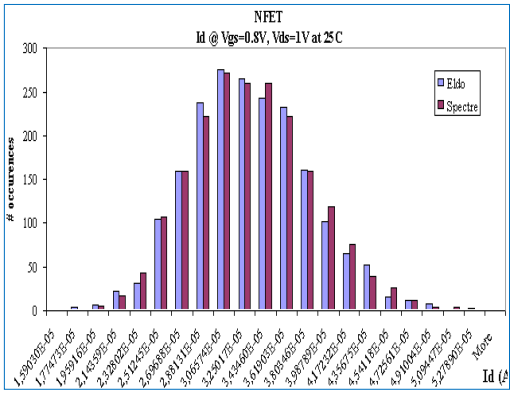
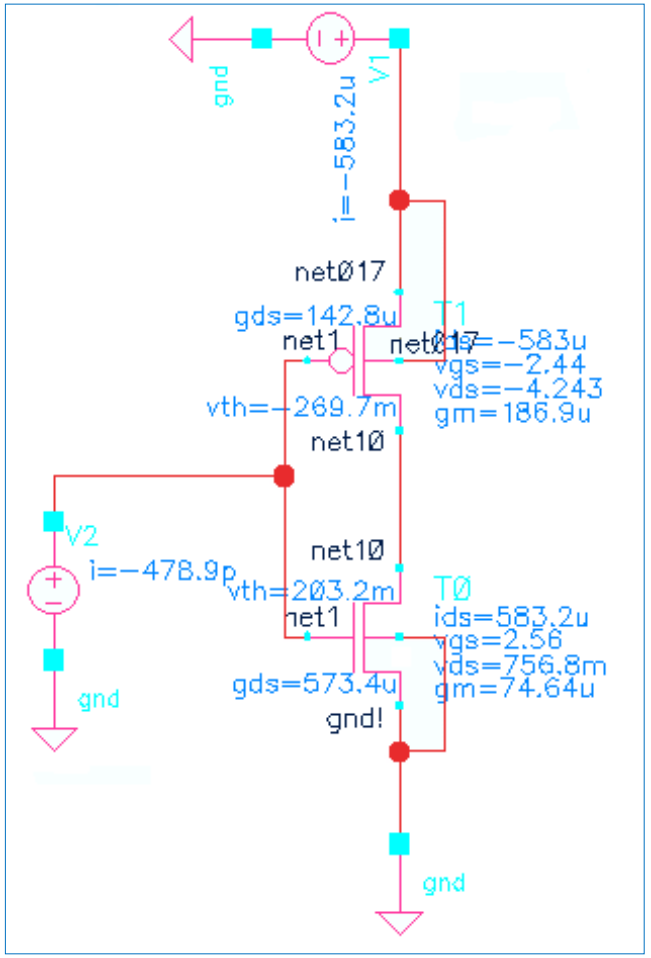


Fig. 10. MOS Inverter with pulse voltage source



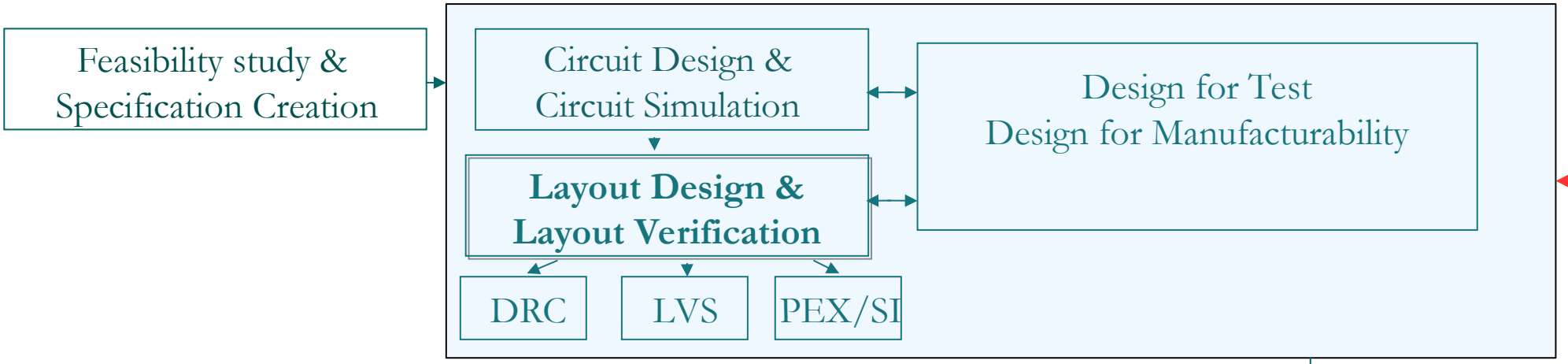


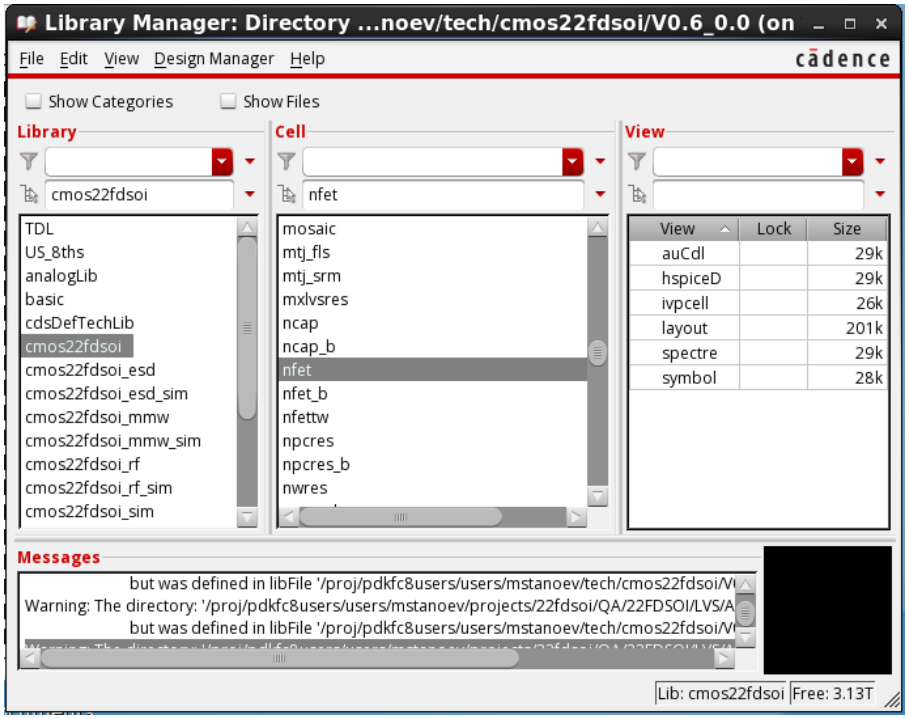
Device Models

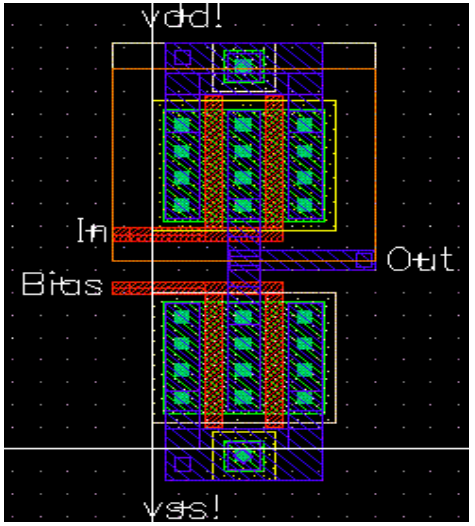


- In the process of technology development the first revision of the models is based on TCAD simulations or models from previously developed technology nodes. As the technology development advances the TCAD data is substituted by measurement data.
- The accuracy of the models together with yield, device performance targets and design rule maturity are the major factors determining whether a technology is production ready.
- The statistical distribution of the model parameters is a crucial part of the device models.
- Spectre and Hspice are the most commonly used simulators. In certain cases Eldo, ADS and GoldenGate are also supported.

Cadence Library (PCells)







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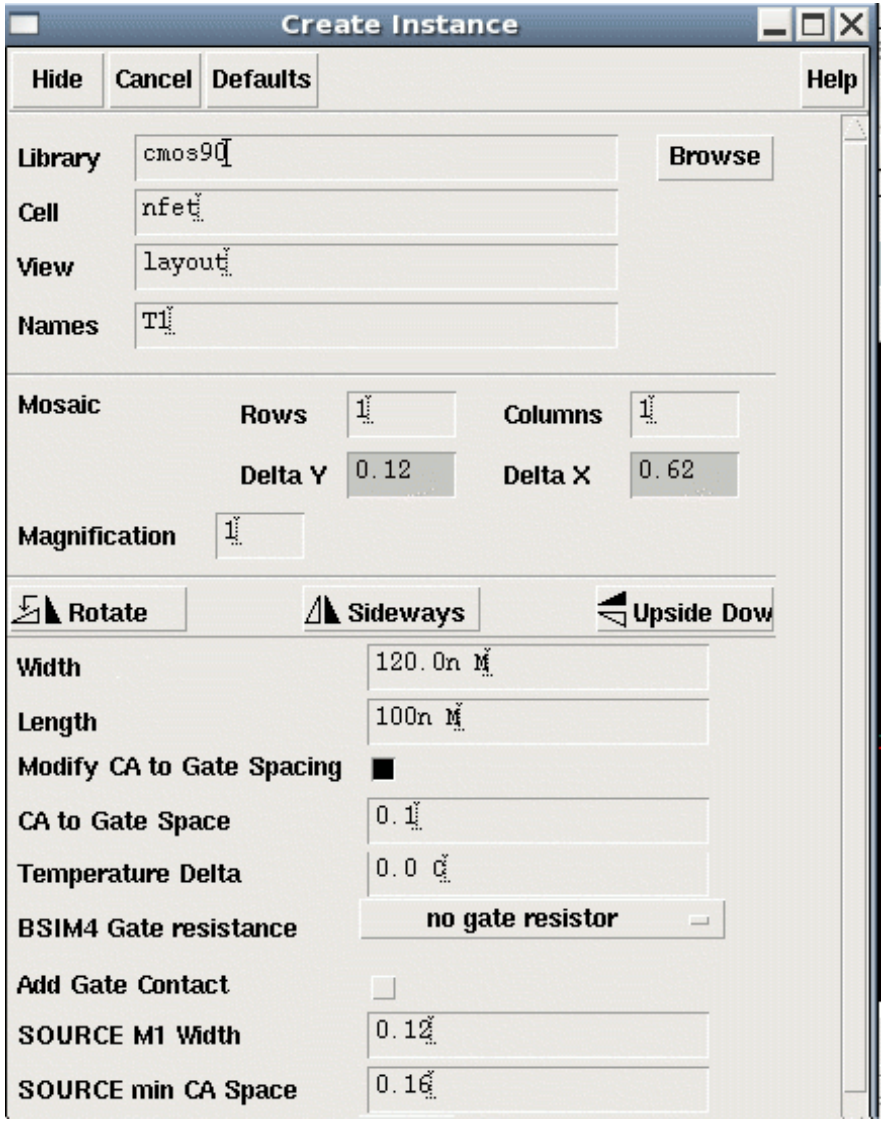
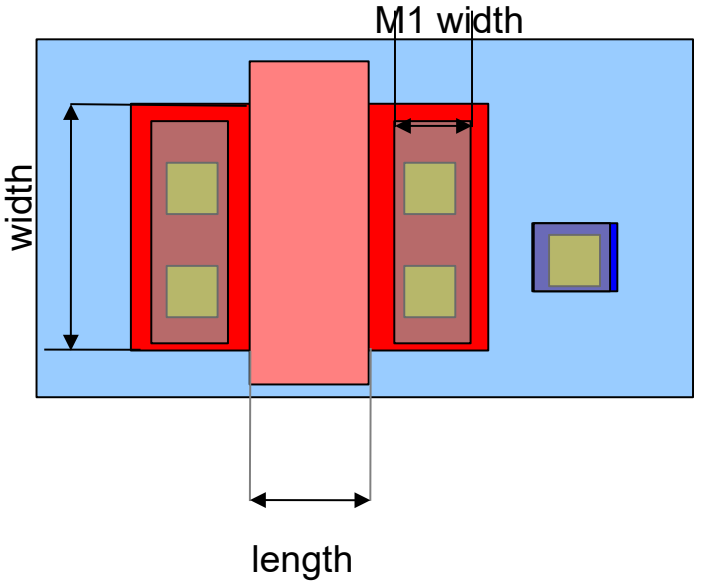
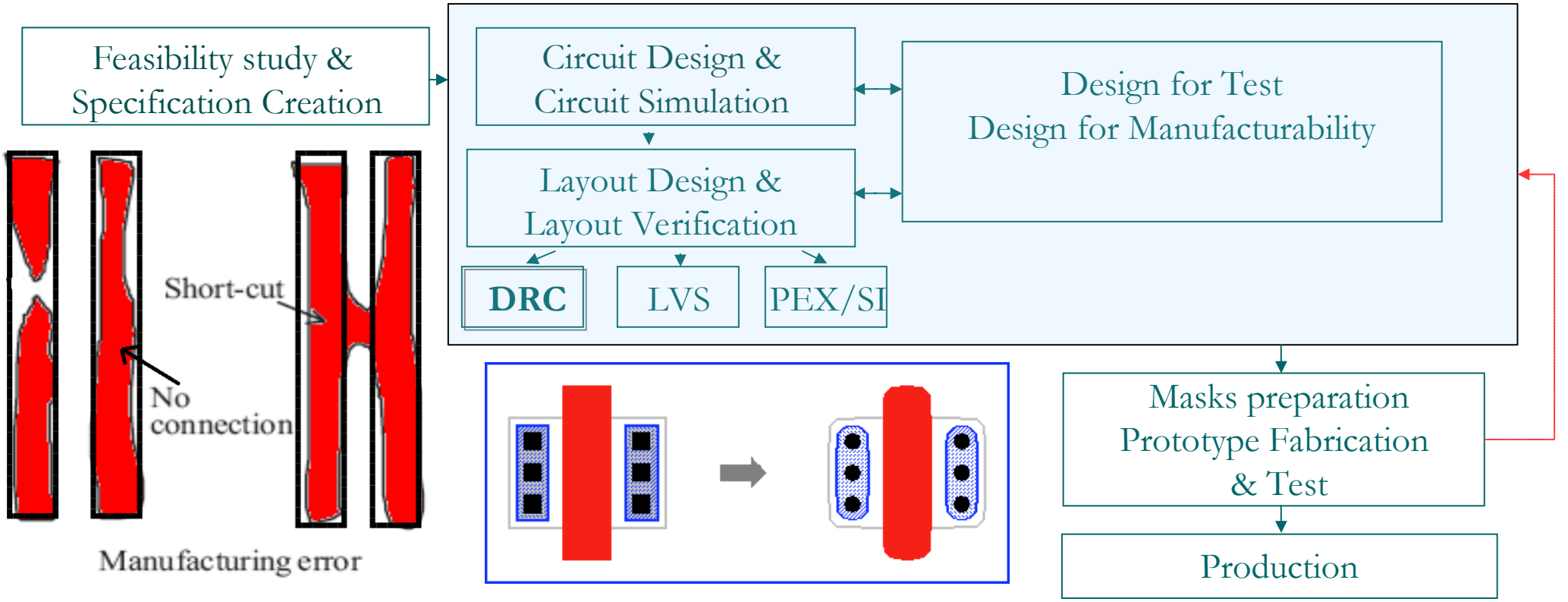




- The Cadence Library contains: device parametric cells (pcells), technology file, CDL parameters, netlisting information, etc...
- Cadence IC is the industry standard tool for schematic and layout design.
- Cadence SKILL is most commonly used to develop this module.

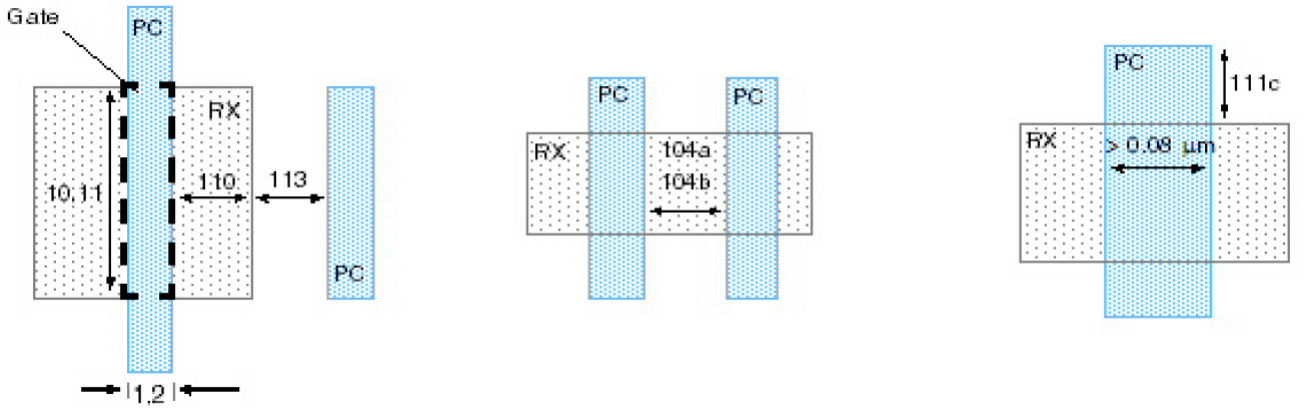
Design Rule Checking (DRC)



Rule	Notes	Description	Operator	Value
504	-	M1 minimum space to (M1 with width > 0.156 µm) for run length > 0.000 µm.	≥	0.066
504a1	-	(M1 with width > 0.156 µm) minimum space to (M1 with width > 0.072 µm) for run length > 0.000 µm.	≥	0.074

Design Rule Checking (DRC)

- Each process has its restrictions that have to be obeyed to produce a working chip i.e. the resolution of the lithographic equipment imposes restriction on the minimum shape sizes and spacings.
- A DRC rule is the logic definition of a process restriction i.e. GR.M1.S.1: "*The spacing of shapes on METAL1 should be > 100n".*
- A modern technology often has several thousand rules grouped in different categories: spacing, latch-up, antenna, density, multiple-patterning etc..
- Calibre nmDRC, ICV DRC, Assura/PVS DRC are the most commonly used tools for DRC verification.



Rule Set 10: Required Antenna Design Rules

Rule	Notes	Description	Operator	Value
130a	-	For each PC intersecting RX, the ratio of (the PC area over RX) to (the total PC area) must be > 1% [areas checked for same net PC].	-	-

Layout vs Schematic (LVS)

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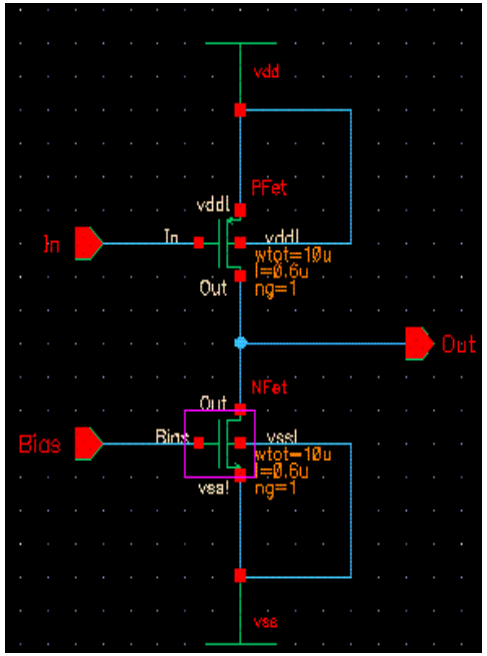
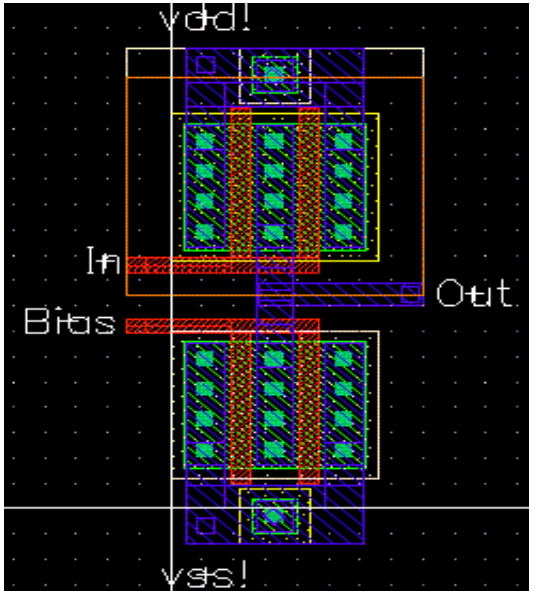
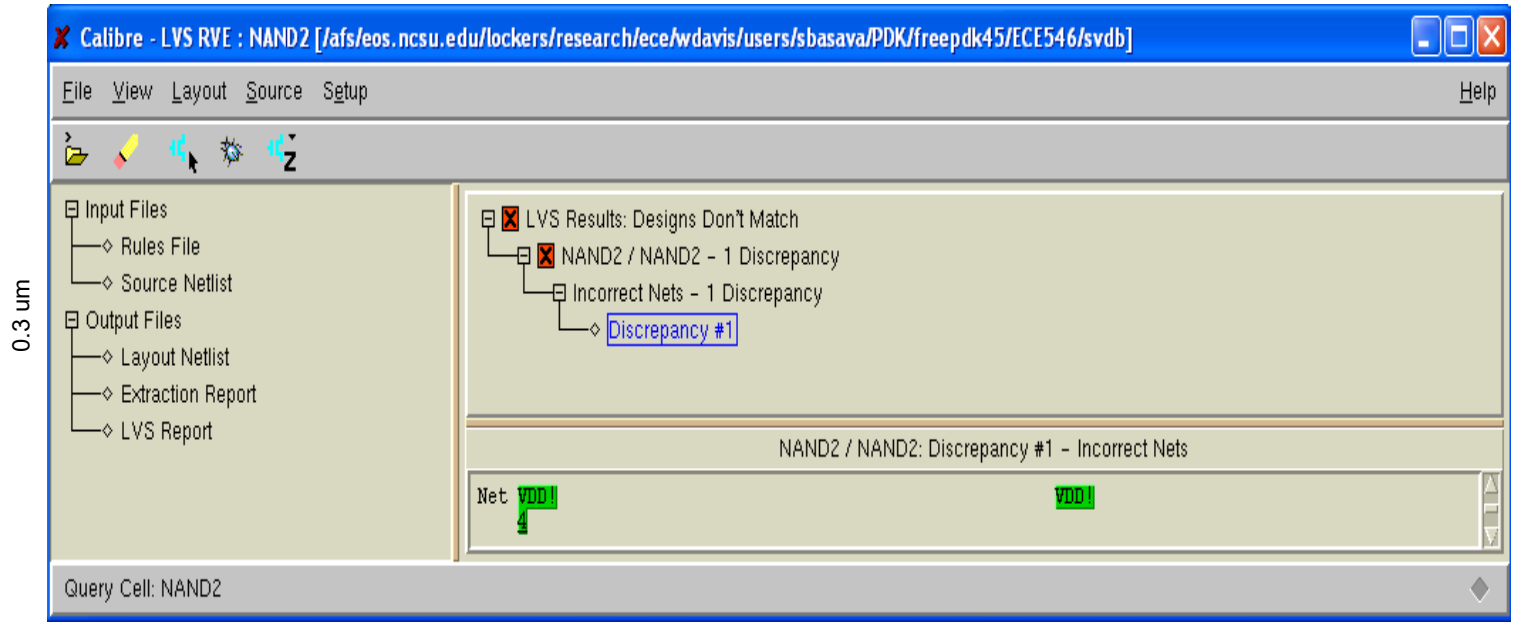


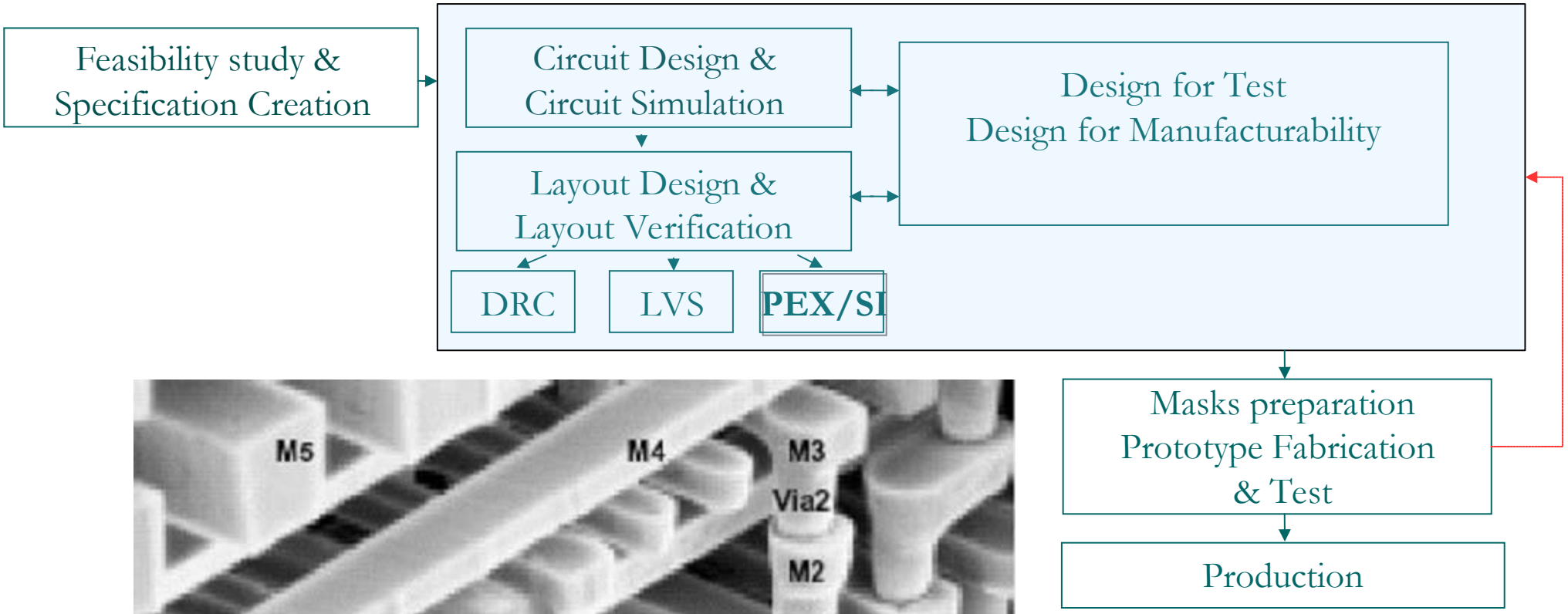


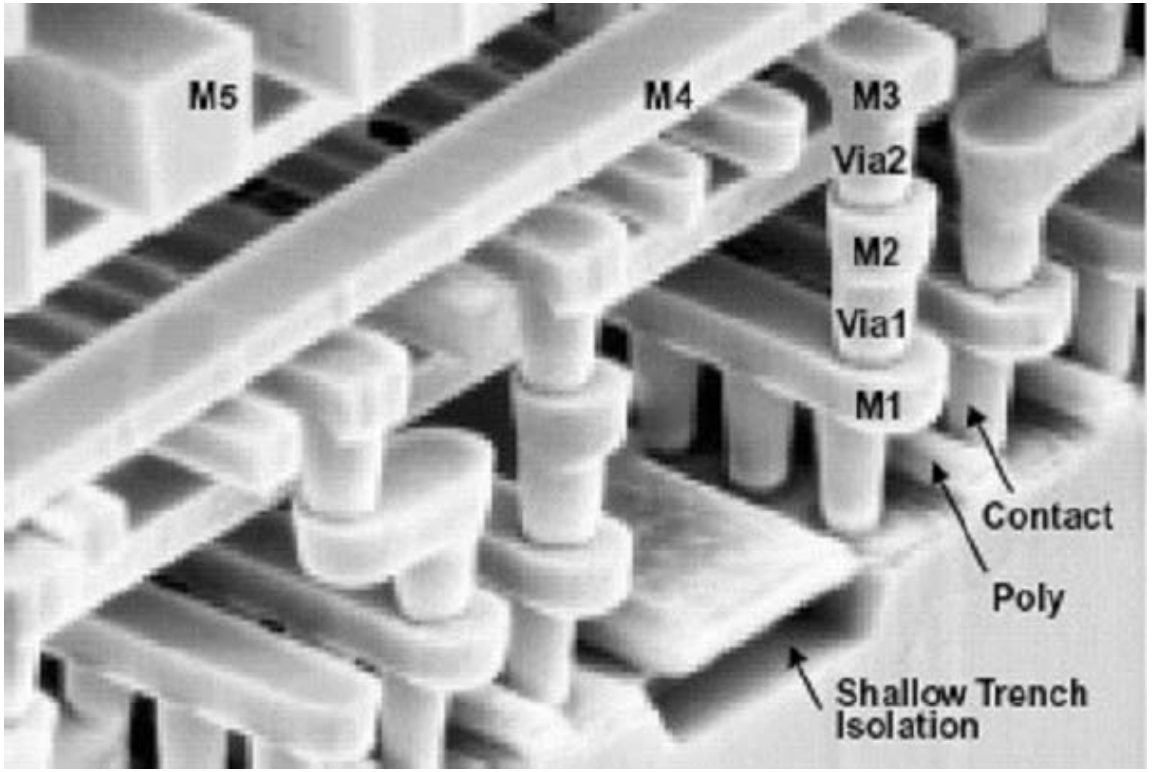
Layout vs Schematic (LVS)

- Verifies the electrical equivalence between schematic and layout. Flags any device, connectivity or parameter mismatches including forbidden circuit transformations.
- Runs in to steps: extract and compare.
- In the extract step a spice-like netlist is extracted from layout based on the technology “rules” for device formation and routing.
- In the compare step, the layout extracted netlist is compared to the schematic generated netlist and all discrepancies between the two are reported.
- Calibre nmLVS, ICV LVS, Assura/PVS LVS are the most commonly used tools for LVS extraction and comparison.



Parasitic Extraction

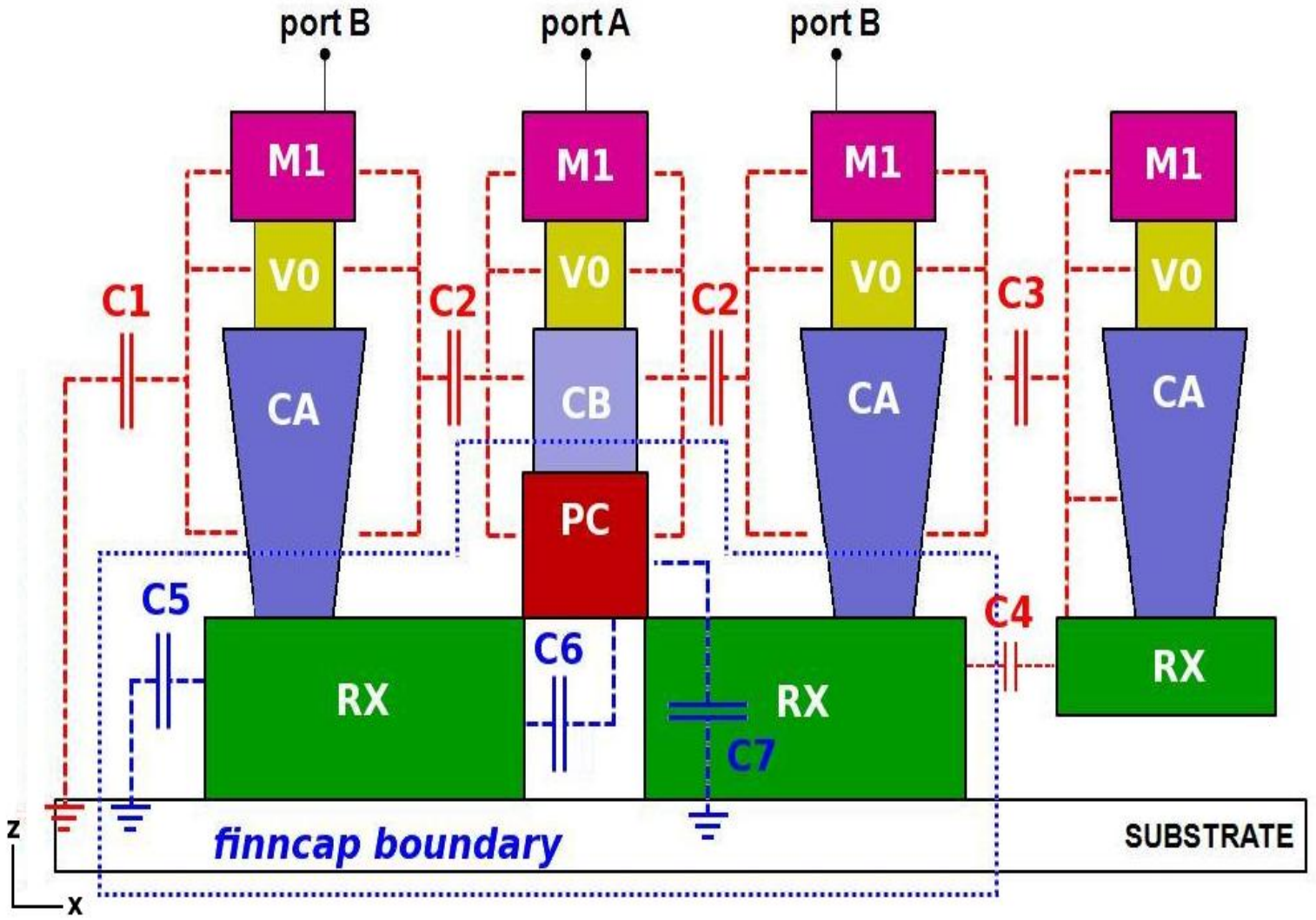




Parasitic Extraction

- Used to identify and quantify passive parasitic components (R, C, L) formed during the layout design.
- The PEX PDK module contains information about conductive layers' resistivity, oxide dielectric constants, etching profiles, metal curving radius and other local layout effects defining the parasitic R, C, L components.
- The layout design and the LVS extracted database are used as inputs.
- The output is an extended netlist that contains also the extracted parasitic components. This netlist is used for resimulation.
- Star RCXT, Calibre xRC and Qauntus QRC are the most commonly used tools for PEX analysis.

Parasitic Extraction



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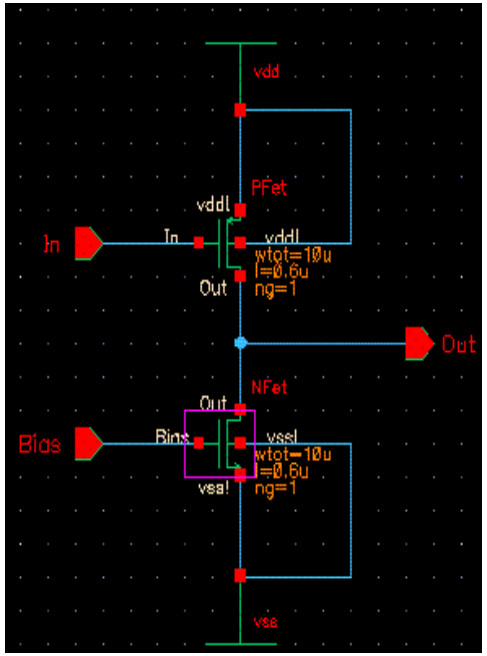

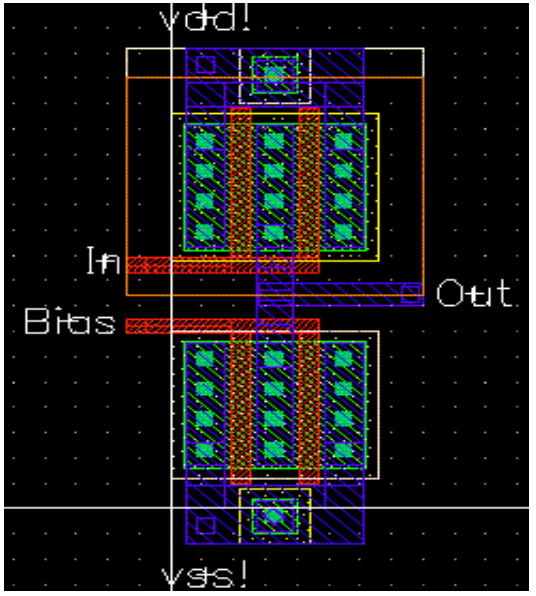

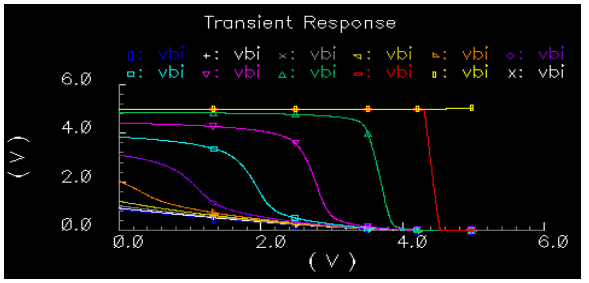

Other Modules

- Electrostatic Discharge (ESD) Protection: specialized device models, additional schematic and layout ERC rules. Often Calibre PERC and PERC LDL is used to implement the ERC checks.
- Electromigration (EM) and Supply Voltage Drop (IR) analyses. Cadence Voltus and Ansys RedHawk/Totem in combination with specialized PEX module and Spice simulations are used to implement those analyses.
- Yield improvement. A combination of “recommended” DRC rules, statistical simulations and yield analysis module (i.e. Calibre YieldAnalyzer).
- Multi patterning decomposition modules.

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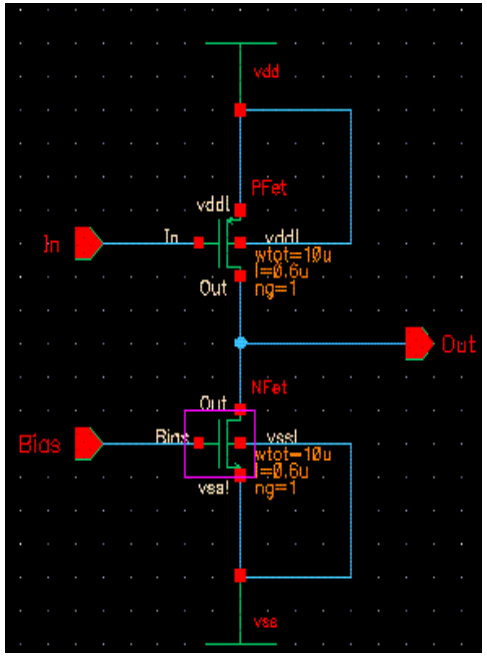
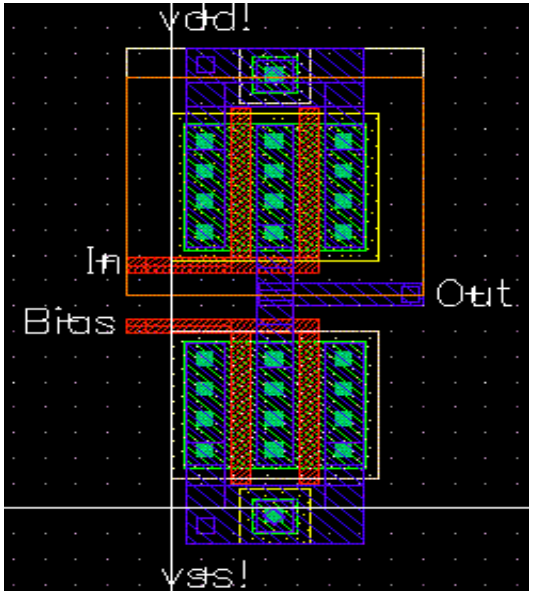
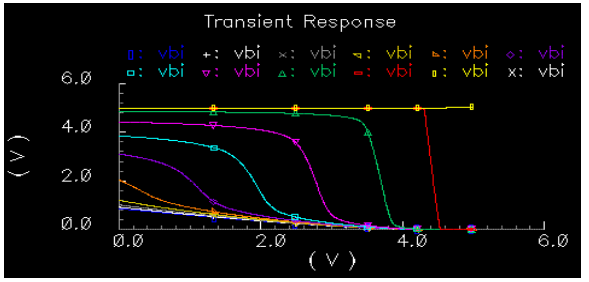
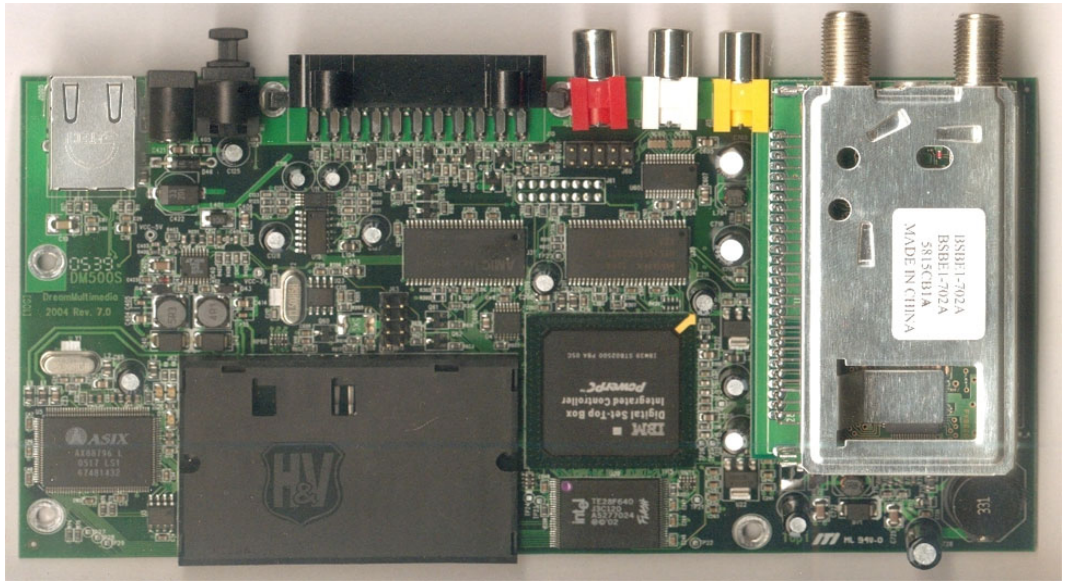
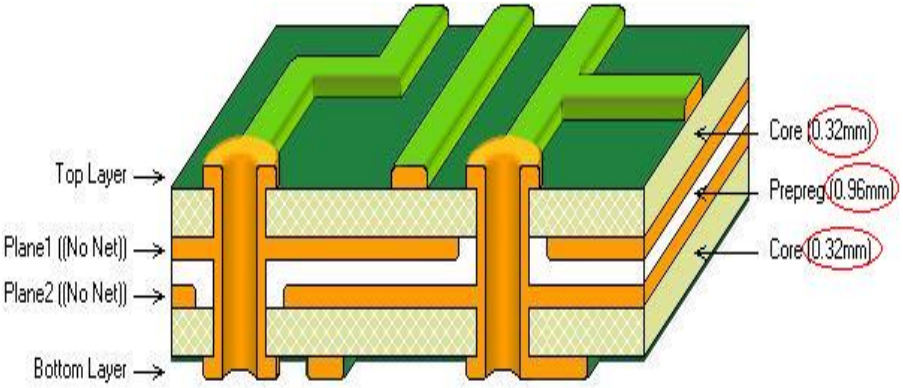






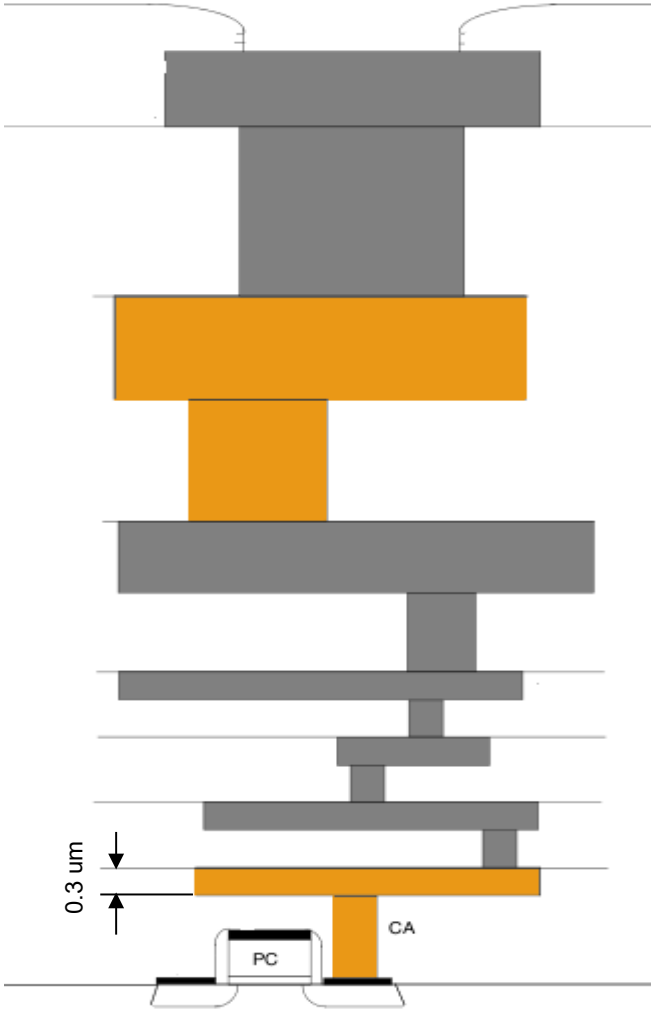
PCB vs. IC - Similarities and differences





- Integrated circuits, bulk components and interface connectors are used as building blocks of PCBs.
- On a singe board different interfaces can be combined – electrical, mechanical, thermal, optical etc.
- The manufacturing technology for PCBs is well established and standardized. The designers may choose the manufacturing site after the PCB has been layed out.
- The parasitic components that are formed are passive (R, L, C).

PCB vs. IC - Similarities and differences



- The scale is different - IC:PCB ≃ 1:10 000, hence the Frequency, Area, Price.
- The IC designers have control over the physical parameters of the semiconductor devices. This introduces flexibility but also complexity. Both passive and active parasitic (diodes, transistors) components that can be formed during layout.
- Each IC design is strongly dependent on the process by which it will be manufactured. The Fab/Foundry should be chosen prior to the design cycle start.

IC technologies

• **CMOS** – a base technology. Uses Si substrate in which the semiconductor devices are formed, and supports 2-20 metal layers separated by dielectric ($Si0_2$) above the substrate. Most of its devices are available also in the other types of technologies mentioned below. Active nodes: 22nm, 14nm, 10 nm. In development: 7nm an 5nm.

• **BiCMOS** – After CMOS has been enabled, process steps to form bipolar transistors can be added. Usually a 2-3 generation older CMOS technology is used as a starting point. Active nodes: 350nm – 90nm.

RF-CMOS – Thick metal layers and Low-k dielectrics have to be available to enable support of inductors, transmission lines and metal-insulator-metal capacitors. Once those devices are enabled the technology can address RF applications. Active nodes: 350nm – 90nm.

• **Electro-Mechanical** – Can be derived from a CMOS process, or developed separately. In both cases the sizes (scale) fall several generations behind a modern CMOS process. Used for manufacturing of MEMS.

• **Electro-optical** – Can be derived from a CMOS process, or developed separately. In this field a lot of new materials are tested to achieve higher luminosity, new wavelengths, higher photo-sensitivity etc. Usually several generations behind CMOS.

Thank you!