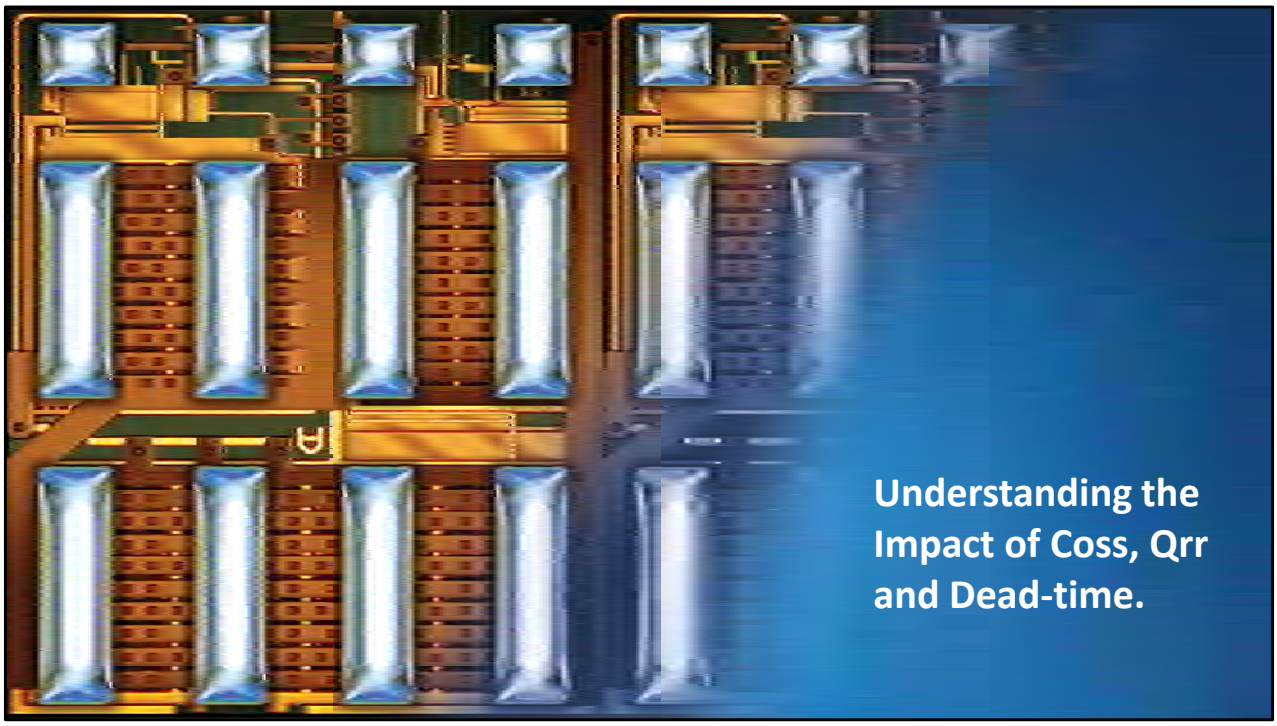


Welcome to the third installment of our How2GaN summer series.

In this webinar, we will talk about understanding the impact of output capacitance (Coss), reverse recovery charge Qrr and dead time on efficiency.

Motivation

- Switching loss is often dominant loss.
- Unfortunately switching loss is often poorly understood.
- Deadtime plays a major role in hard-switching losses.

Motivation

(Build 1) Switching loss is often the dominant loss.

(Build 2) Unfortunately switching loss is often poorly understood.

(Build 3) Dead time plays a major role in hard switching losses

Discussion Assumptions

A hard-switching buck converter with:

- Synchronous rectifier
- Sufficient deadtime for Sync Rectifier body diode commutation.
- Stray inductance negligible
- $R_{DS(on)}$ negligible

Discussion Assumptions.

We'll be looking at a hard switching buck converter with:

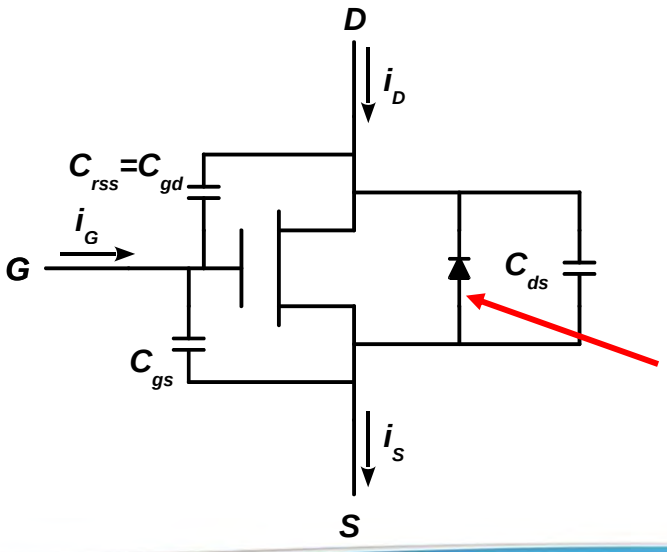
(Build) a synchronous rectifier

(Build) sufficient dead time for Sync Rectifier full body diode commutation

(Build) Negligible stray inductance

(Build) Negligible RDSon Loss.

FET Parasitics (Excluding Inductance)



Capacitance

$C_{iss} = C_{gs} + C_{gd}$

$C_{rss} = C_{gd}$

$C_{oss} = C_{ds} + C_{gd}$

Body diode

$V_{S2,diode}$

Q_{RR}

Let's look at typical FET paracitics.

(Build) The dominant paracitics are capacitance.

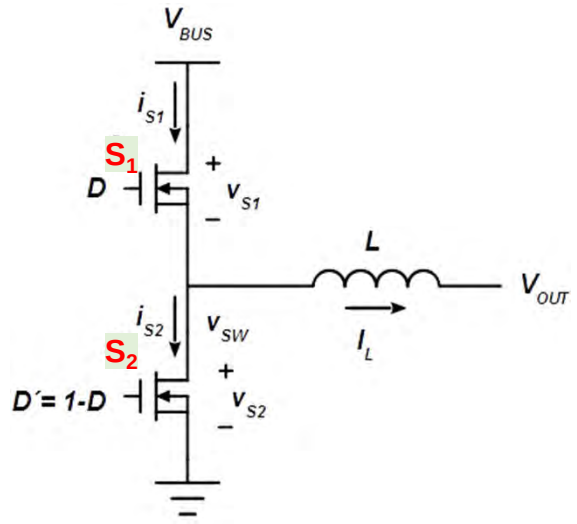
The capacitors are typically identified as Ciss, Crss and Coss.

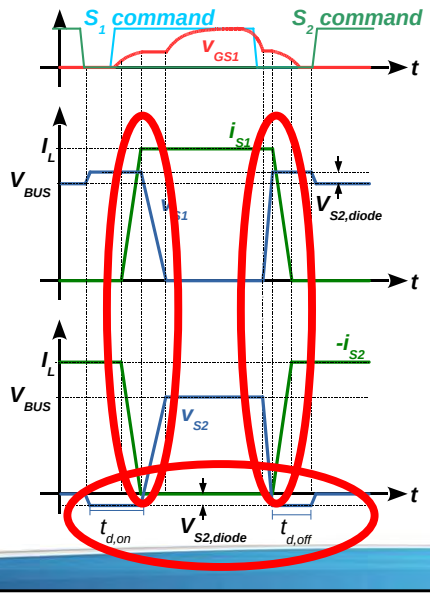
They are often written in terms of the gate to source capacitance, Cgs, gate to drain capacitance, Cgd and the drain to source capacitance Cds.

(Build) We also need to consider the paracitics of the body diode function which has a forward voltage drop VS2.

Silicon MOSFETs have a body diode with minority carriers which creates reverse recovery charge, Qrr

Buck Converter with Sync Rectifier (SR)





Let's look at the operation of a buck convertor with a synchronous rectifier.

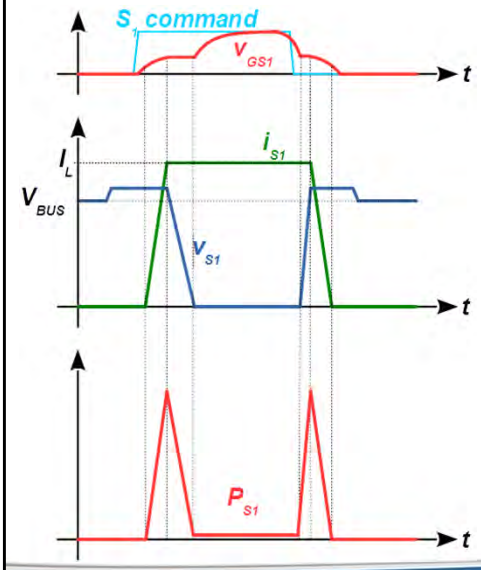
S1 is on the high side and synchronous rectifier S2 on the low side.

S1 is on with a duty cycle feeding an inductor that pulls a constant average current.

(Build 1) This is what we normally consider to be called transition losses or switching losses.

(Build 2) However we're also going to talk about dead time losses highlighted here when the body diode conducts.

Switching Losses: Control FET S_1



Input charge effects

- C_{iss} affects transition speed
- Faster transition = lower switching loss

eGaN FETs (vs. Si MOSFETs)

- **Have very low C_{iss}**
- **Switch faster**
- **Have lower transition loss**

Let's take a look at the switching loss of high side FET S1.

Shown here are typical waveforms.

The Blue S1 command is the Control signal with the resulting Red Vgs Gate Voltage.

(Build 1) Input Charge Effects:

(Build 2) CISS has a direct effect on transition speed.

(Build 3) Faster transition = lower switching losses.

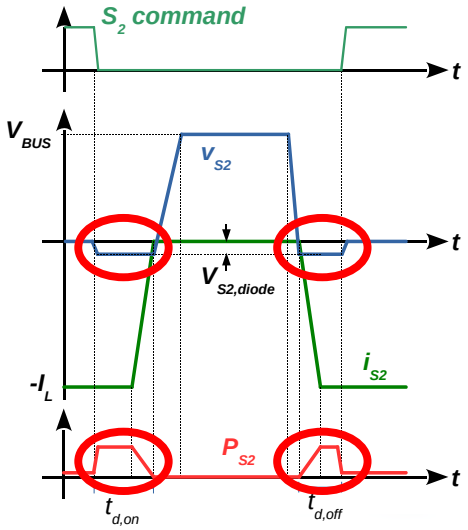
(Build 4) Comparing eGaN FETs with Silicon MOSFETs, eGaN FETs have:

(Build 5) Very low input capacitance CISS.

(Build 6) Switch faster

(Build 7) Have lower transition loss.

Switching Losses: SR FET S_2



Switching Losses

- Ciss has no participation
- No transition overlap = no transition loss

Deadtime losses

$$E_d = V_{S2,diode} I_L (t_{d,on} + t_{d,off})$$

eGaN FETs (vs. Si MOSFETs)

- **eGaN FETs have higher diode drop**
- **= higher deadtime losses**

What about switching loss on the synchronous rectifier FET S2

Shown is the typical waveforms for the synchronous rectifier.

The switch node commutation is driven by the inductor all the way into full body diode conduction. AKA Soft Switch.

(Build 1) Notice sync FETs Ciss does not have any effect in the switching in any way.

(Build 2) The soft switching means there is no hard transition losses.

Allowing enough dead time for body diode conduction prevents shoot between S1 and S2 and maximize efficiency,

(Build 3) However dead time created losses with the equation shown.

S2 Forward body diode conduction results in a negative diode voltage drop in waveform VS2.

Notice the dead time has a multiplying effect on the power loss.

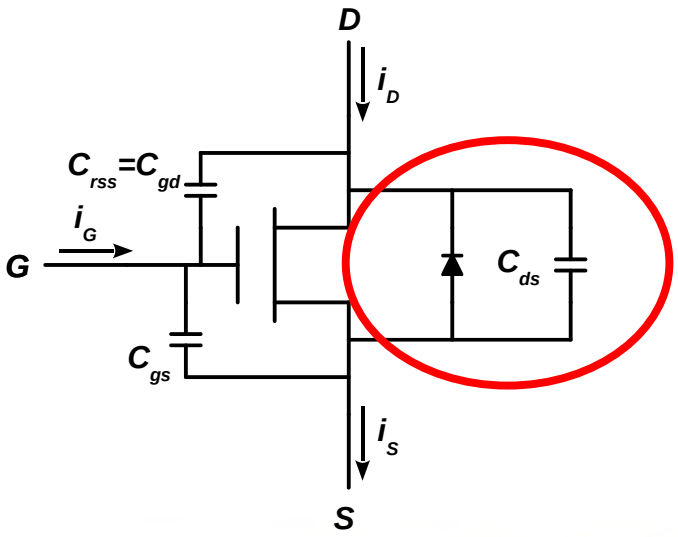
(Build 4) Comparing eGaN FETs with Silicon MOSFETs,

(Build 5) eGaN FETs has higher Forward diode voltage.

(build 6) One would assume this would result in higher power losses than a MOSFET.

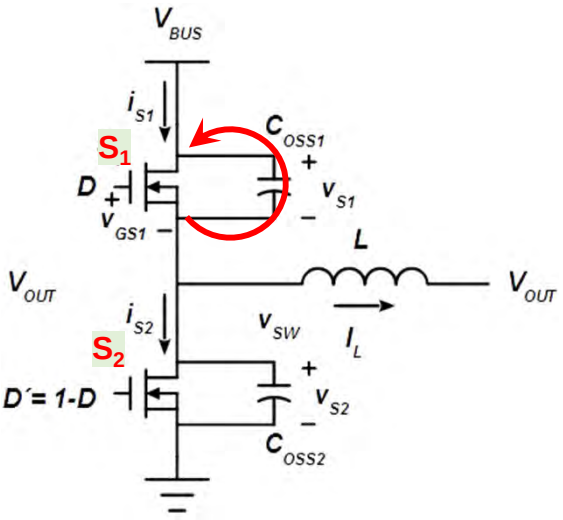
(Build 7) except we find out that in reality this is not true.

Need Closer Look at Output Parasitics



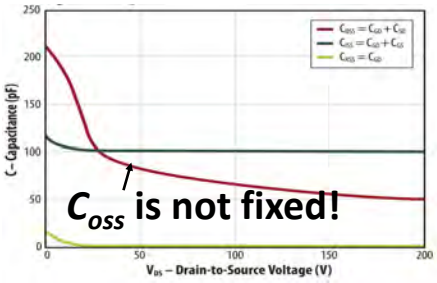
To understand why GaN FET will not necessarily have higher dead time losses than a MOSFET, we need to take a closer look at the output paracitics.

Coss: Output Capacitance Problem



Common approach:

$$E_{oss} = \frac{1}{2} C_{OSS1} V_{BUS}^2$$



C_{oss} is not fixed!

What value of C_{oss1}?
What about C_{oss2}?

First, we will look at output capacitance COSS

(Build 1) When we turn on S1 we discharge the stored charge on Coss1 and that energy is lost.

(Build 2) Shown is the common Eoss energy loss equation used by some engineers.

(Build 3) The problem with using this equation is in reality Coss is not fixed value. It is a function of Vds.

(Build 4) Since Coss is not linear, you left with the question of what Coss1 value do you use?

(Build 5) What about Coss2?

We has stated that switch S2 doesn't have any switching loss.

However, if one puts a large capacitor in parallel with Coss2, it's going to severely disrupt the operation of the converter.

So, it obviously has an effect. So, what do we do with nonlinear capacitance?

Coss: Non-Linear Capacitance

- Capacitors store charge *Q* and energy *E*

$$Q_{oss}(V_{DS}) = \int_0^{V_{DS}} C(v)dv \qquad E_{oss}(V_{DS}) = \int_0^{V_{DS}} vC(v)dv$$

- Accurate values calculated at the desired V_{DS}
- Time-related and energy related equivalent capacitances

$$Q_{oss} = C_{oss,tr}V_{DS} \qquad E_{oss} = \frac{1}{2}C_{oss,er}V_{DS}^2$$

Lets go back to basics.

(Build 1) Capacitor's store charge Q and they store energy E.

These terms can be written in the form of an integral formula where:

(Build 2) QOSS is a function of a capacitance and VDS.

(Build 3) EOSS is a function of a capacitance and VDS.

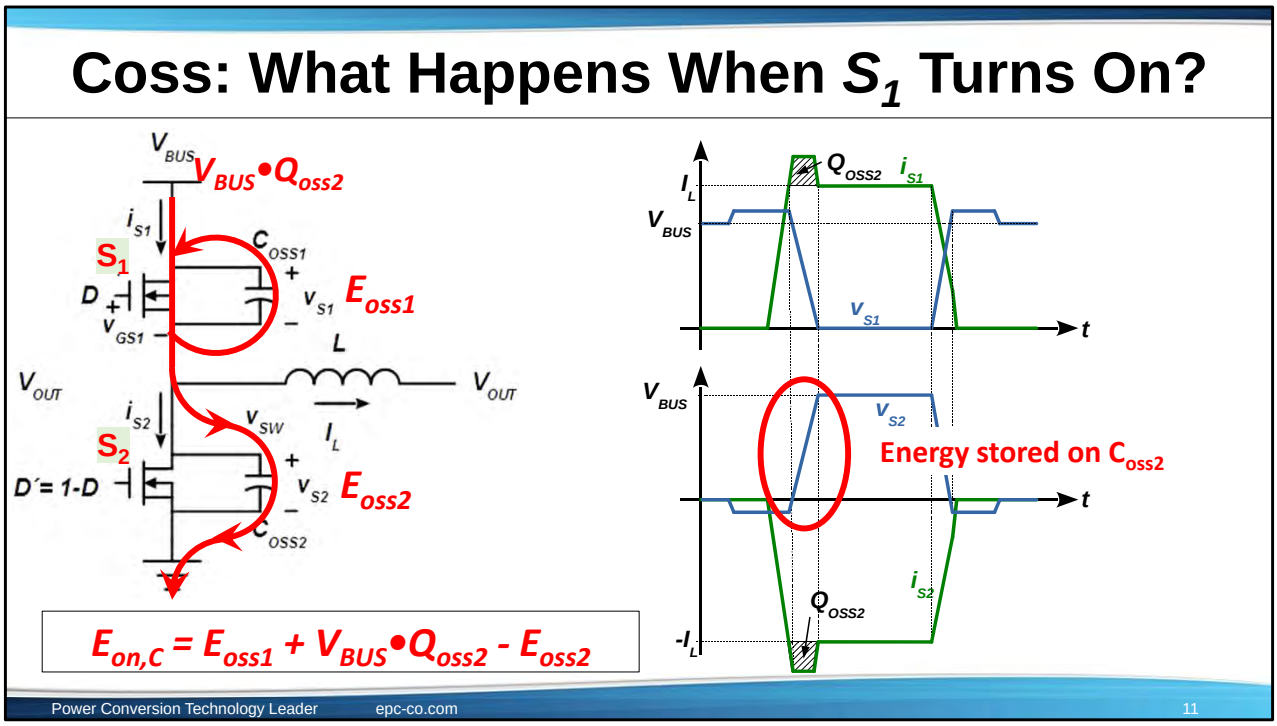
Note the equations are not the same but now accurate values can be calculated.

(Build 4) Now we can compute time related and energy related equivalent capacitances by saying:

(Build 5) What capacitance would I need to get a particular QOSS

(Build 6) What capacitance would I need to get a particular EOSS.

These capacitances values are not identical unless the capacitor is a linear capacitor.



Lets take a look at Coss capacitance when S1 turns on.

The top set of waveforms is for the high side switch S1

The bottom set of waveforms is for the low side switch S2

(Build 1) Let's turn S1 on. We discharge the energy in the top switch, which we'll call Eoss1

(Build 2) But, happening at the same time the switch node voltage is rising charging Coss2,

(Build 3) That charge comes from the bus which is V bus, times Qoss2

(Build 4) At the end of the turn on interval we have energy stored on Coss2 which we'll call Eoss2.

(Build 5) Now we can compute the total energy lost during turn of S1 due to capacitive effects.

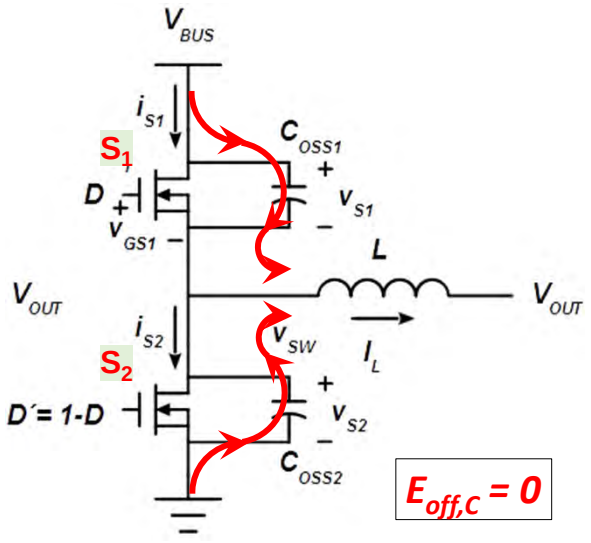
The energy Eon. is equal to:

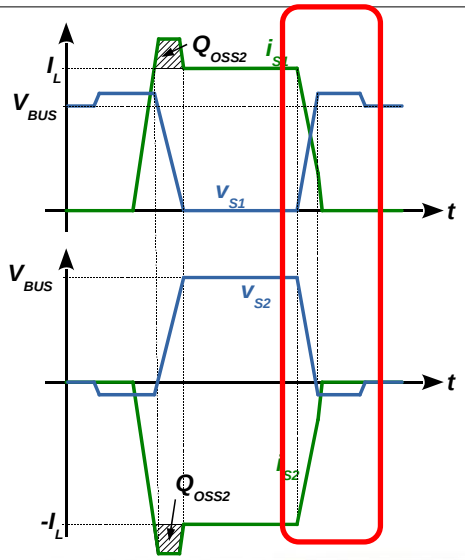
Eoss1, which is lost when we discharge the first capacitor plus

Vbus x Qoss2, which is the energy needed to charge Coss2 during the turn on interval plus

Eoss2, which is the final charge on Coss2 and the end of the turn on interval.

Coss: What Happens When S_1 Turns Off?





Power Conversion Technology Leader epc-co.com 12

Now lets look at the capacitance when we turn S1 off

(Build 1) The inductor wants to pull current from charged Coss2 which is connect to ground discharging Coss2.

At the same time

(Build 2) The inductor also wants to pull current from discharged Coss1 which is connected to Vbus charging Coss1.

(Build 3) Since all of energy is pulled by the inductor, the net turn off energy lost due to capacitance is zero.

Coss Loss Summary

$$E_{on,C} = E_{oss1} + V_{BUS} \bullet Q_{oss2} - E_{oss2}$$

If switches S_1, S_2 are identical, then:

$$E_{on,C} = V_{BUS} \bullet Q_{oss}$$

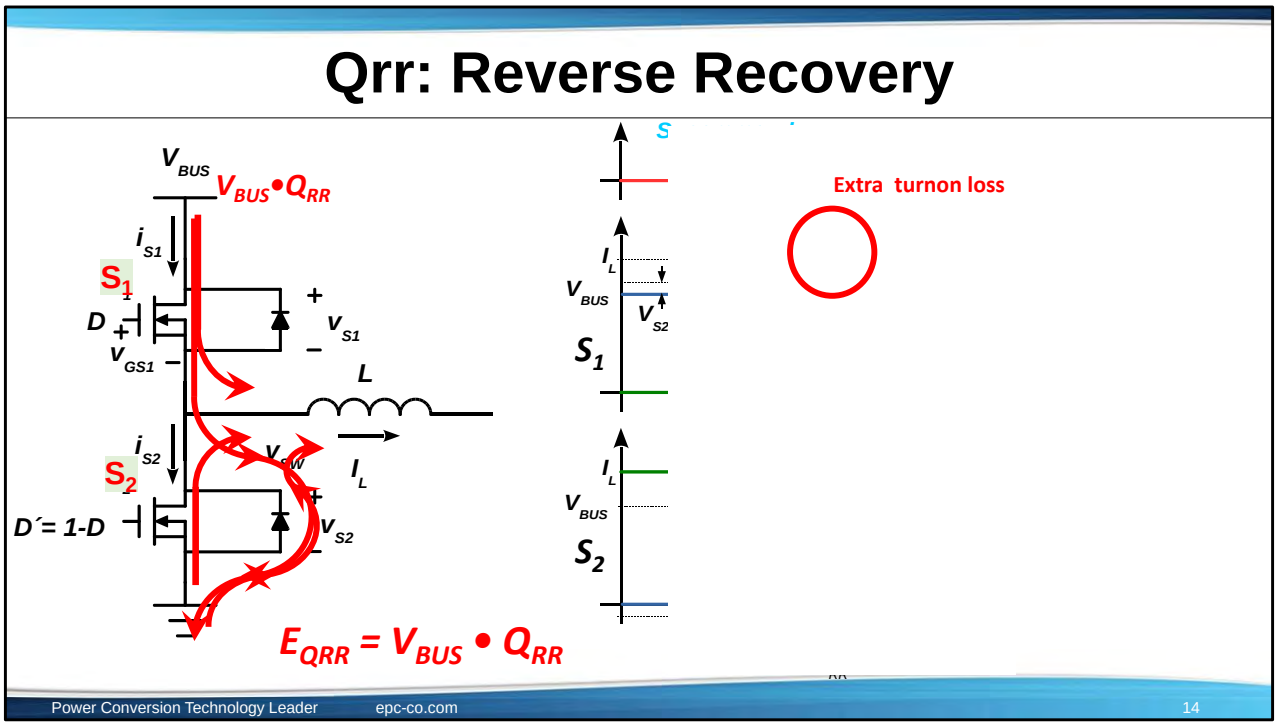
Coss Energy Loss Summary

(Build 1) Coss energy losses per switching cycle is tied to the turn on switching event with the equation shown.

(Build 2) If the FET switches are identical part numbers, then Eoss1 and Eoss2 are identical canceling each other out.

(Build 3) This simplifies the equation leaving Eon equal to Vbus times Qoss.

It should be noted that eGaN FETs typically have lower Coss than a MOSFET allowing it to switch more efficiently.



Let's now look at reverse recovery which occurs when you have a body diode that's a P-N junction

(Build 1) We start with Synchronous rectifier S2 in the on state with inductor current flowing through the device.

(Build 2) Then we turn off S2.

This forces the inductor current to commutate to the body diode of S2 for the duration of the dead time.

(Build 3) Next, we turn on S1.

S1 starts to supply current to the inductor and as S1 current rises the current in S2 falls.

(Build 4) a short time later S1 fully satisfies meeting the entire inductor current.

(Build 5) However at the same time, the current reverses and starts to flow through

the body diode of S2 in the opposite direction it was flowing the moment before.

But wait, this is a diode, and it should have blocked the current flow. This is the conduction phenomenon of reverse recovery.

When the current reverses in the body diode it is due to stored minority carrier charge Qrr within the junction region of the body diode.

This charge cannot instantly or easily be swept out of the diode.

Until the Qrr charge is removed with time, the body diode does not turn off and continues to conduct current.

This diode current can be quite high. Essentially reverse recovery amounts to a shoot through condition.

(Build 6) Eventually the diode recovers.

When the charges all recombine or are swept out the diode turns off stopping the current flow.

However, during the reverse recovery period, we have additional energy loss due to QRR

(Build 7) The loss, EQrr, is equal to Vbus times Qrr.

Qrr: Loss Equation Update

$$E_{Q,output} = E_{oss1} + V_{BUS} \bullet Q_{oss2} - E_{oss2} + V_{BUS} \bullet Q_{RR}$$

$= 0$

If switches S_1, S_2 are identical, then

$$E_{Q,output} = V_{BUS} \bullet (Q_{oss} + Q_{RR})$$

$= 0$

For eGaN FETS

We need to update our capacitive loss equation to show Qrr charge.

Again if the FETs S1 and S2 are identical that simplifies the equation but it still needs to includes Qrr charge loss.

QRR is a strong contributor to output switching loss..

(Build 1) In the case of eGaN FETs, QRR is zero.

Qrr: eGaN FET Versus Silicon MOSFET

- **eGaN FET: Q_{RR} = 0!**
- Si MOSFET: Q_{RR} Reverse recovery only happens within the PN junction body diode
- *MOSFET* Q_{RR} worsens with
  - Higher temperatures
  - Higher currents
  - Faster switching
  - Higher voltage rating
  - **Longer deadtimes**

Let's compare eGaN FETs to silicon MOSFETs

(Build 1) Again, for eGaN FETs, Qrr is equal to zero.

(Build 2) For Silicon MOSFETs, Qrr Reverse recovery only happens with a PN junction body diode.

It is important to consider the QRR is not actually a fixed value.

It is not well characterized in typical datasheets and there is no industry standard on how to measure it.

(Build 3) MOSFETs vendors will give you a number, but in reality QRR worsens:

(Build 4) higher temperatures.

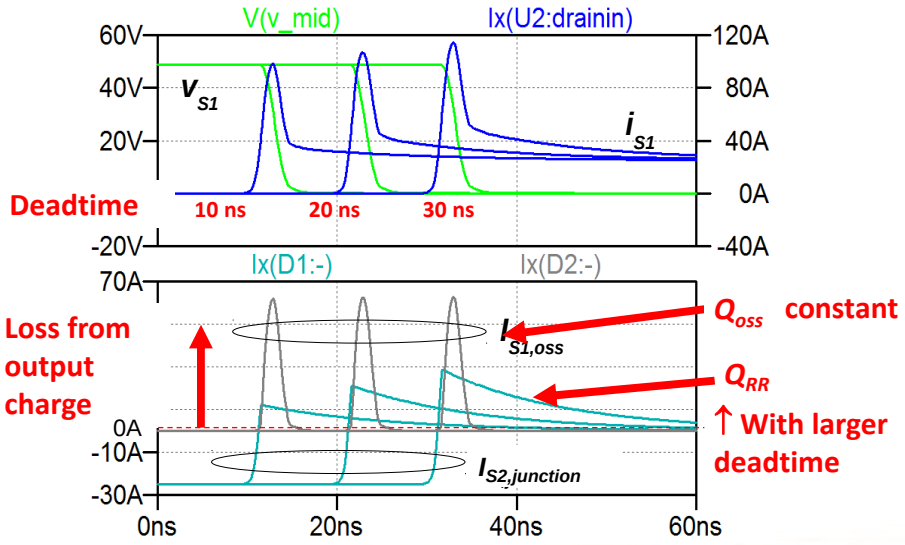
(Build 5) as current goes up

(Build 6) faster switching

(Build 7) higher MOSFET voltage ratings

(Build 8) with longer dead times,

Qrr: Effect of Changing Deadtime



How does changing dead time have an effect on QRR?

Let's take a look at some typical waveforms.

On the top are the high side switch waveforms.

0nS is the time just after the bottom switch turned off and we established current flow through the diode.

Looking at the top waveform, S1 Vds voltage is in green which collapses when we turn S1 on.

The resulting S1 current is in dark blue.

S1 current rises to very large peak value before finally collapsing and returning to the inductor current.

The peak portion of the current is a sum of charging currents both Coss2 and Qrr.

On the bottom waveforms the S1 current has been broken up into two parts:

(Build 1) The gray waveform show Qoss charging current.

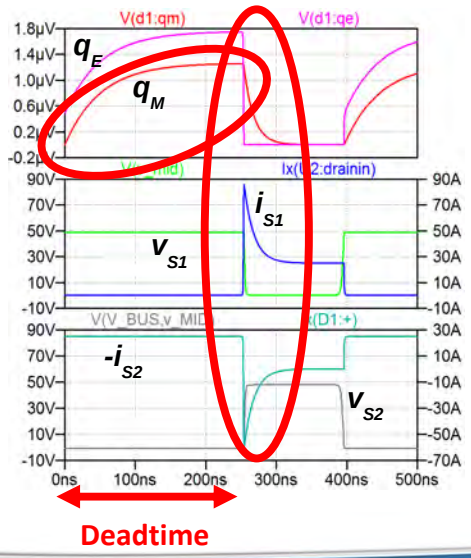
(Build 2) The cyan waveform show S2's body diode's Qrr charging current.

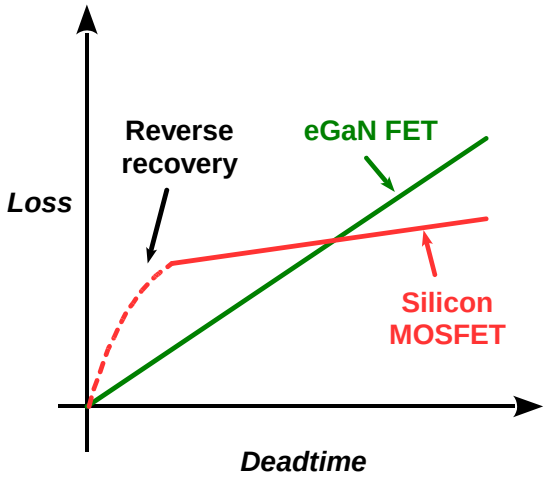
(Build 3) Any positive current above the 0-amp line is loss from total output charge.

Qoss loss is not a function of dead time being pure capacitive.

(Build 4) QRR, on the other hand is getting both higher and longer as the dead time is increased. 10 nanoseconds 20 nanoseconds and 30 nanoseconds.

Qrr vs Dead Time: Why and What





Power Conversion Technology Leader epc-co.com 18

Why is QRR alone a function of dead time loss?

This involves a deeper dive into the diode structure..

The top left graph shows charges within the body diode of the FET.

The middle graft shows the top switch waveforms

The bottom graft shows the bottom switch waveforms.

Returning to the Top graph, we see the two charge waveforms.

QE, is the charge injected into the diode junction region to support normal conduction.

QM represents a surplus minority carrier charge deep in the junction region.

At T= 0nS, we've just turned the rectifier switch off and force inductor current to start flowing into the body diode.

QE builds immediately in order to support the inductor current.

(Build 1) QM follow behind injecting additional charge into the junction region that is stored.

While the diode is conducting, we see both these charges increases exponentially with time,

(Build 2) if we make the dead time very long, eventually QM and QE will flatten out and reach a maximum.

(Build 3) Now we turn S1 on and we see that QE charge drops to zero.

Inductor Current has stopped flowing in the diode.

However, QM is not zero and the charge has to decay exponentially mostly due to recombination.

Meanwhile the diode can conduct reverse current until QM = 0

(Build 4) So how does this affect the loss?

If you look at the eGaN FET, there is no reverse recovery.

Loss is a linearly as a function of dead time because loss is simply due to the reverse voltage drop. The longer the dead time, the more energy is dissipated.

With a PN body diode inside a MOSFET there is a sharp increase in loss due to QRR that tapers off.

Starting at deadtime of 0 nS, we can plot Qrr loss of a MOSFET versus Forward Voltage loss of a GaN FET.

At low dead times, the GaN FET has lower losses.

DeadTime: Experimental Setup for 80 V FETs

- Buck converter using identical PCB Layouts
  - One PCB for each type of FET tested.
- Baseline loss measured at min deadtime (5 ns):

$$P_{baseline}$$

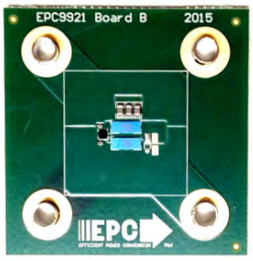
- Total losses measured as function of deadtime:

$$P_{loss}$$

- Loss due to deadtime:

$$P_d = P_{loss} - P_{baseline}$$

- Separate experiments for varying deadtime:
  - Rising edge: $T_{d,on}$ varies, $T_{d,off}$ fixed
  - Falling edge: $T_{d,off}$ varies, $T_{d,on}$ fixed



Test conditions

- **V_{IN} = 48 V**
- **V_{OUT} = 12 V**
- **F_{sw} = 300 kHz**
- **L = 4.7uH**

Proof? We've done some GaN vs MOSFETs experiments using 80V rated parts.

We design a special 50mm x 50mm buck converter board for each FETs tested.

They have identical layout as close as possible subject the limits of FET footprint differences.

Each board was operating at 48 to 12 volts, 300 kilohertz using the same 4.7uH inductor and output capacitors.

Since we could not have a true 0 nS deadtime condition without shoot-through issues, we started with a 5nS and call this P baseline.

We made this loss be our 0 by subtracting it out of all measurements.

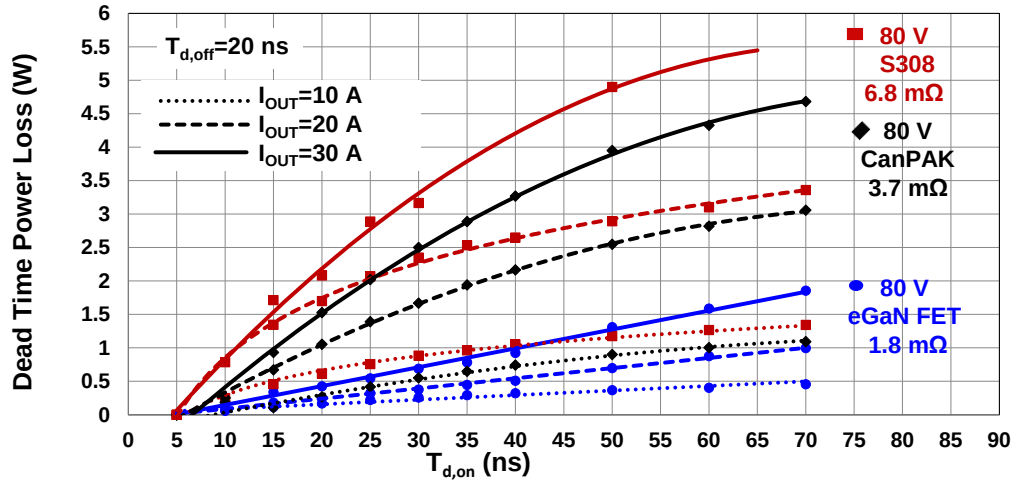
(Build 1) We started adding 5nS to the total dead time and measured total losses.

This is repeated until all dead times have been measured for all FETs.

(Build 2) Dead time loss is then calculated using the equation shown.

(Build 3) Finally we did separate experiments for varying dead times but only varied the rising edge or falling edge keeping the other constant.

Dead Time: Impact of Turn-on



The graph shows S1 Turn-On deadtime results with a fixed Turn-off deadtime of 20 nanoseconds.

We used 3 different 80V FETs. 2 MOSFETs shown in Black and Red with 1 eGaN FET shown in Blue.

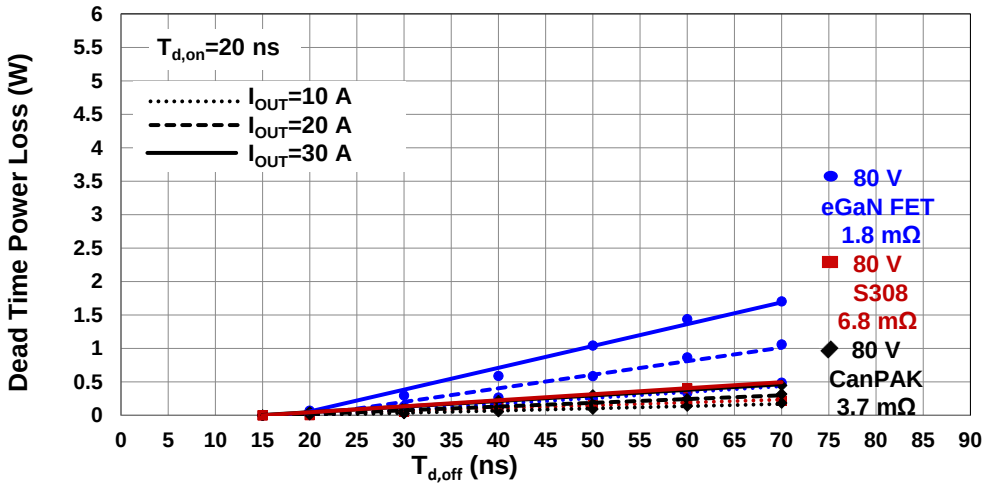
Results were plotted for 10 amps, 20 amps, and 30 amps

Looking at the small dotted lines for a 10A load, the Silicon MOSFETs losses are quite low on the order of a watt. Not to far away from the GaN FET results.

However, at both 20A (dash) and 30A (Solid Line), we see a sharp increase in losses that gets worse and worse as you increase dead time.

Eventually the MOSFET losses start to level off, but the MOSFET losses are now 2 to 3 times than the losses of the GaN FET approaching 6 watts.

Deadtime: Impact of Turn-off



Now, let's look at S1 turn off deadtime with turn on deadtime fixed at 20 nanoseconds.

Same currents, same scales on both the X axis and the Y axis as previous graph.

Notice we don't have any reverse recovery losses. The inductor is driving the switch node.

Silicon MOSFETs do perform better, and that's because they have a lower voltage drop on their body diode than a eGaN FET.

The GaN FET look almost identical to their turn on deadtime loss because the losses in both cases are due to voltage drop only.

If you were to sum both Turn On and Turn Off dead time losses together, the eGaN FET wins with lower dead time losses overall.

DeadTime Summary

- Deadtime losses play a large role in switching losses
- Mechanisms for deadtime switching losses
  - Body diode voltage drop (Si MOSFETs, eGaN FETs)
  - Reverse recovery (Si MOSFETs only)
- **Q_{RR} losses in Si MOSFET can be much higher than high reverse voltage drop in eGaN FETs**
- **Deadtime management critical for Si MOSFETs**

Dead Time Summary.

(Build 1) Deadtime losses play a large role in switching loss.

(Build 2) The mechanisms for dead time switching losses are:

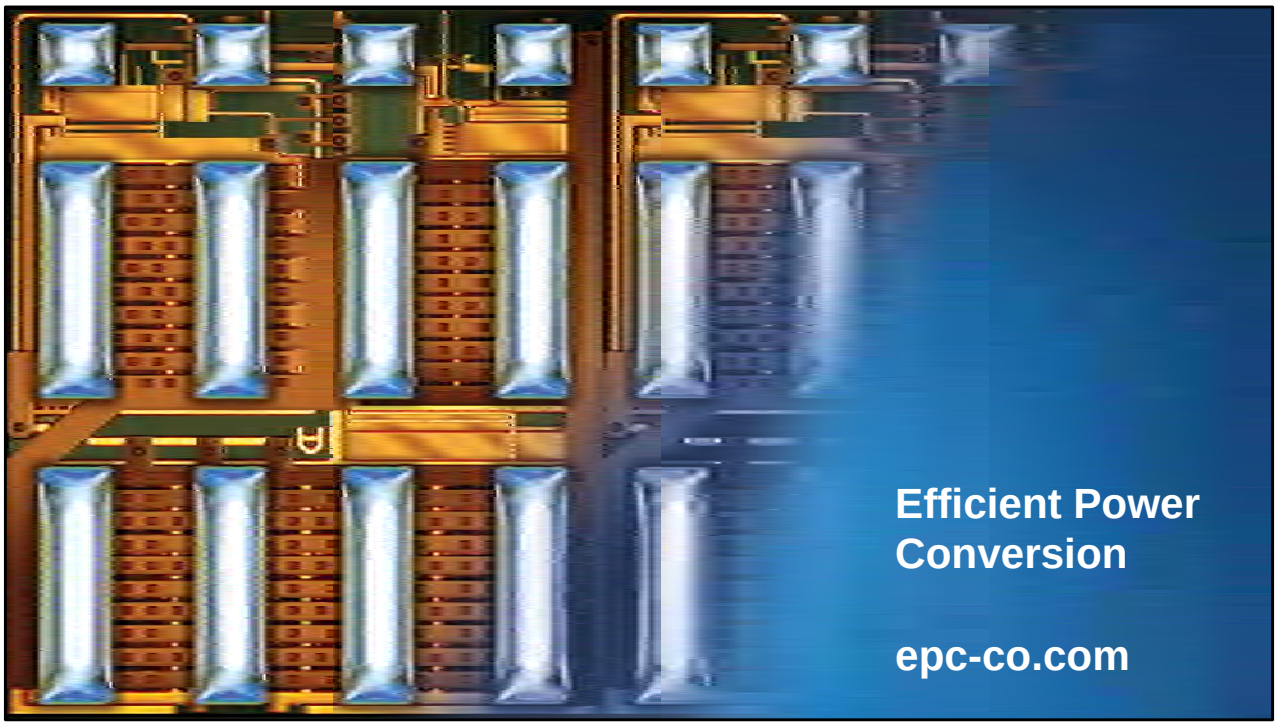
(Build 3) Body diode voltage drop and

(Build 4) Reverse recovery in the case Silicon MOSFETs.

(Build 5) We've shown the MOSFET Qrr losses can be several times higher than the high reverse voltage drop losses of eGaN FETs.

(Build 6) Dead time management is critical for silicon MOSFETs.

It is harder to manage deadtime in silicon MOSFETs than in eGaN FETs


Efficient Power
Conversion
epc-co.com

Next Webinar

Final Session of How2GaN Summer Webinar Series

- August 25, 2021
  Thermal Management of GaN FETs