Technical Note

Calculating Memory System Power for DDR3

Introduction

DDR3 SDRAM provides additional bandwidth over previous DDR and DDR2 SDRAM. In addition to the premium performance, DDR3 has a lower operating voltage range. The result can be a higher bandwidth performing system while consuming equal or less system power. However, it is not always easy to determine the power consumption within a system application from the data sheet specification.

This technical note details how DDR3 SDRAM consumes power and provides the tools that system designers can use to estimate power consumption in any specific system. In addition to offering tools and techniques for calculating system power, Micron's DDR3-1067 "Data Sheet Specifications" on page 20 and a DDR3 Power Spreadsheet Usage Example on page 20 are provided.

Table 1 describes the command abbreviations found in the following sections.

Table 1:   Abbreviation Definitions

Abbreviation	Definition
ACT	ACTIVATE
BL	Burst length
BC	Burst chop
PRE	PRECHARGE
ODT	On-die termination
RD	READ
REF	REFRESH
WR	WRITE

DRAM Operation

To estimate the power consumption of a DDR3 SDRAM, it is necessary to understand the basic functionality of the device (see Figure 1 on page 2). The operation of a DDR3 device is similar to that of a DDR2. For both devices, the master operation of the DRAM is controlled by clock enable (CKE).

If CKE is LOW, the input buffers are turned off. To allow the DRAM to receive commands, CKE must be HIGH, thus enabling the input buffers and propagates the command/ address into the logic/decoders on the DRAM.

During normal operation, the first command sent to the DRAM is typically an ACT command. This command selects a bank and row address. The data, which is stored in the cells of the selected row, is then transferred from the array into the sense amplifiers. The portion of the DRAM consuming power in the ACT command is shown in blue and gold in Figure 1 on page 2.

Eight different array banks exist on the DDR3 SDRAM. Each bank contains its own set of sense amplifiers and can be activated separately with a unique row address. When one or more banks has data stored in the sense amplifiers, the DRAM is in the active state.

The data remains in the sense amplifiers until a PRE command to the same bank restores the data to the cells in the array. Every ACT command must have a PRE command associated with it; that is, ACT and PRE commands occur in pairs unless a PRECHARGE ALL command is used.

Figure 1:   1Gb DDR3 SDRAM Functional Block Diagram
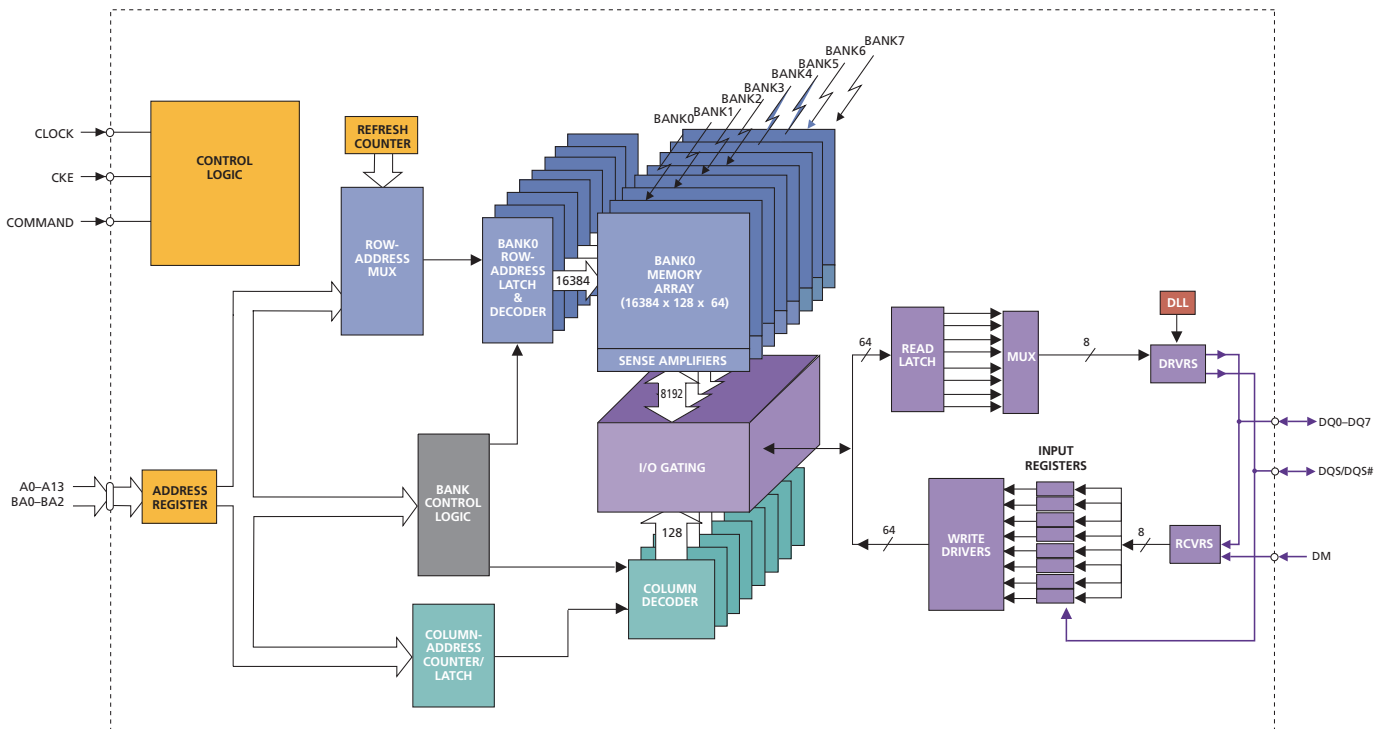
In the active state, the DDR3 device can perform READs and WRITEs. A READ command decodes a specific column address associated with the data that is stored in the sense amplifiers (shown in green in Figure 1). The data from this column is driven through the I/O, gating to the internal READ latch. From there, it is multiplexed onto the output drivers. The circuits used in this function are shown in purple in Figure 1.

The process for a WRITE is similar to the READ except the data propagates in the opposite direction. Data from the DQ pins is latched into the data receivers/registers and is transferred to the internal data drivers. The internal data drivers then transmit the data to the sense amplifiers through the I/O gating and into the decoded column address location.

DDR3, like DDR2, includes ODT on the data I/O pins. This feature is controlled by the ODT pin and consumes additional power when activated. The ODT and the output driver on DDR3 includes additional mode register settings over previous DRAM to increase system flexibility and to optimize signal integrity. This power needs to be included in total power calculations (see "I/O Termination Power" on page 12).

DRAM Power Calculators

The I$_{DD}$ values referenced in this article are taken from Micron's preliminary 1Gb DDR3-1067 data sheet, and they are listed in "Data Sheet Specifications" on page 20. While the values provided in data sheets may differ from between vendors and different devices, the concepts for calculating power are the same. It is important to verify all data sheet parameters before using the information in this article.

Methodology Overview

The following four steps are required to calculate system power:

1. Calculate the power subcomponents from the data sheet specifications. (This calculation is denoted as Pds(XXX), where XXX is the subcomponent power.)
2. Derate the power based on the command scheduling in the system (Psch[XXX]).
3. Derate the power to the system's actual operating V$_{DD}$ and clock frequency (Psys[XXX]).
4. Sum the subcomponents of the system's operating conditions to calculate the total power consumed by the DRAM.

Background Power

As discussed previously, CKE is the master on-off switch for the DRAM. When CKE is LOW, most inputs are disabled. This is the lowest power state in which the device can operate, and if all banks are precharged, it is specified in the data sheet as I$_{DD}$2P. If any bank is open, the current consumed is I$_{DD}$3P. I$_{DD}$2P has two possible conditions, depending on whether mode register bit 12 is set for a slow or fast power-down exit time. The appropriate I$_{DD}$2P value should be used for the power calculations based on how the application sets this mode register.

CKE must be taken HIGH to allow the DRAM to receive ACT, PRE, READ, and WRITE commands. When CKE goes HIGH, commands start propagating through the DRAM command decoders, and the activity increases the power consumption. The current consumed is specified in the data sheet as I$_{DD}$2N if all banks are precharged or I$_{DD}$3N if any bank is active.

Figure 2 on page 4 shows the typical current usage of a DDR3 device when CKE transitions, assuming all banks are precharged. When CKE is HIGH, the device draws a maximum I$_{DD}$2N of 65mA of current; when CKE goes LOW, that figures drops to an I$_{DD}$2P of ~10–25mA, depending on how slow or how fast the power-down exit time is. All of these values assume the DRAM is in the precharged state. Similarly, if the device is in the active state, it consumes I$_{DD}$3P current in power-down (CKE = LOW) and I$_{DD}$3N current in standby (CKE = HIGH).

Figure 2:   Effects of CKE on I_{DD} Consumption
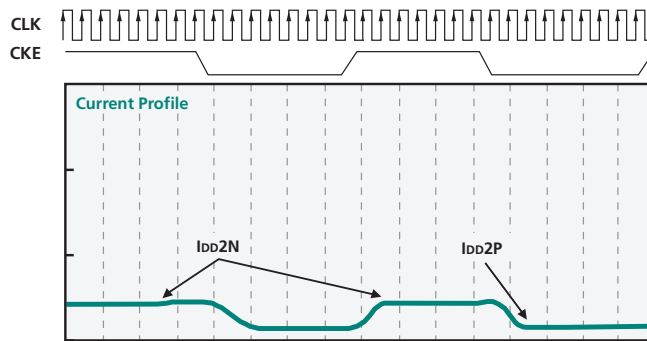
Calculation of the power consumed by a DDR3 device operating in these standby conditions is easily completed by multiplying the I_{DD} and the voltage applied to the device, V_{DD}.

$$Pds(PRE\_PDN) = I_{DD}2P \times V_{DD}$$

(Eq. 1)

$$Pds(PRE\_STBY) = I_{DD}2N \times V_{DD}$$

(Eq. 2)

$$Pds(ACT\_PDN) = I_{DD}3P \times V_{DD}$$

(Eq. 3)

$$Pds(ACT\_STBY) = I_{DD}3N \times V_{DD}$$

(Eq. 4)

The data sheet specification for all I_{DD} values is taken at the worst-case V_{DD}, which is 1.575V for DDR3. The calculations for maximum DDR3 standby powers using the assumptions in "Data Sheet Specifications" are as follows:

$$Pds(PRE\_PDN) = 25mA \times 1.575V$$
$$Pds(PRE\_PDN) = 39mW$$

(Eq. 5)

$$Pds(PRE\_STBY) = 65mA \times 1.575V$$
$$Pds(PRE\_STBY) = 102mW$$

(Eq. 6)

$$Pds(ACT\_PDN) = 45mA \times 1.575V$$
$$Pds(ACT\_PDN) = 71mW$$

(Eq. 7)

$$Pds(ACT\_STBY) = 75mA \times 1.575V$$
$$Pds(ACT\_STBY) = 118mW$$

(Eq. 8)

Note: I_{DD}2P in the above equations assumes MR[12] = 0.

During normal operation, the DRAM always consumes background power. This background power can be in one of the four categories above. Therefore, the total average background power is a ratio of these four individual powers. This ratio is determined by the percentage of time the DRAM is precharged (all of the banks are precharged) or active (one or more banks are open). Additionally, the percent of time that CKE is LOW or HIGH during each of the conditions determines the ratio between the standby and the power-down conditions. To complete these ratios, three parameters are required as shown in Table 2.

Table 2:   **DDR3 Background Power Components**

Component	Description
BNK_PRE%	Percentage of time all banks are precharged
CKE_LO_PRE%	Percentage bank precharge time (BNK_PRE%) when CKE is LOW
CKE_LO_ACT%	Percentage bank active time (100% - BNK_PRE%) when CKE is LOW

Equation 9 is used to ratio the data sheet background powers to the specific system usage conditions based on CKE HIGH/LOW times. Note that these numbers cover 100 percent of the normal device operating time.

$$Psch(PRE\_PDN) = Pds(PRE\_PDN) \times BNK\_PRE\% \times CKE\_LO\_PRE\%$$

$$Psch(PRE\_STBY) = Pds(PRE\_STBY) \times BNK\_PRE\% \times [1 - CKE\_LO\_PRE\%]$$

$$Psch(ACT\_PDN) = Pds(ACT\_PDN) \times [1 - BNK\_PRE\%] \times CKE\_LO\_ACT\%$$

$$Psch(ACT\_STBY) = Pds(ACT\_STBY) \times [1 - BNK\_PRE\%] \times [1 - CKE\_LO\_ACT\%]$$

(Eq. 9)

Activate Power

To allow a DDR3 SDRAM to READ or WRITE data, a bank and row must first be selected using an ACT command. For every ACT command, there is a corresponding PRE command. The ACT command opens a row, and the PRE closes the row.

Figure 3 on page 6 illustrates a typical current profile for $I_{DD}0$. Following an ACT command, the device uses a significant amount of current to decode the command/address and then transfer the data from the DRAM array to the sense amplifiers. When this is complete, the DRAM is maintained in an active state until a PRE command is issued. The PRE command restores the data from the sense amplifiers into the memory array and resets the bank for the next ACT command. This leaves the bank in its precharged state.

Figure 3:   IDD0 Current Profile
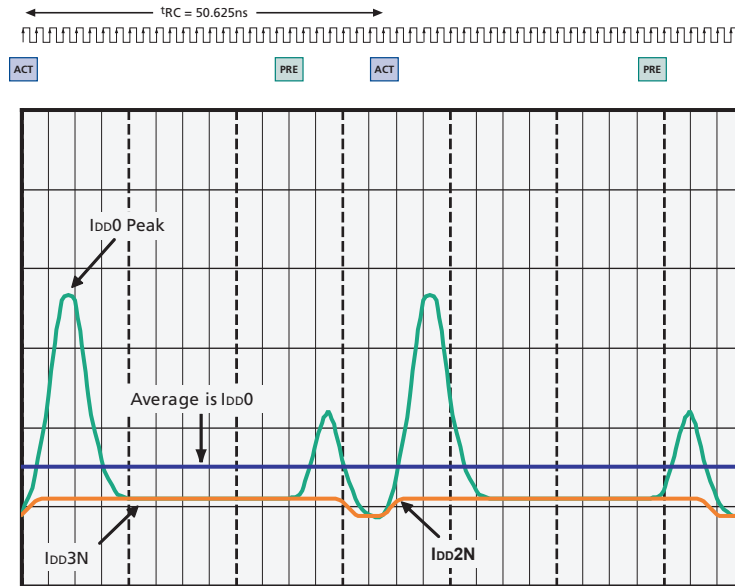
Note: Current profiles are provided for illustrative purposes and are not associated with a specific DDR3 DRAM device.

The data sheet specifies IDD0 averaged over time with the interval between ACT commands being ^tRC. This is represented by the blue line in Figure 3. During this operation, a background current, shown in orange, is always consumed (IDD3N when the row is active and IDD2N when the row is precharged). This background current must be subtracted from IDD0 to identify the power consumed due to the ACT and PRE commands. This is shown in Equation 10, where IDD3N is subtracted from IDD0 during the row active time (^tRAS) and IDD2N is subtracted during the remaining time.

$$Pds(ACT) = \left[IDD0 - \frac{IDD3N \times {}^tRAS + IDD2N \times ({}^tRC - {}^tRAS)}{{}^tRC} \right] \times VDD$$

$$Pds(ACT) = \left[115mA - \frac{[75mA \times 37.5ns] + [65mA \times (50.625ns - 37.5ns)]}{50.625ns} \right] \times 1.575V$$

Pds(ACT) = 63mW

(Eq. 10)

Equation 10 provides the maximum power consumed only if the DRAM is used at MIN ^tRC cycle time as specified in the data sheet. This is noted as Pds(ACT), meaning "power under data sheet conditions." However, most systems do not operate in this manner. Fortunately, it is easy to scale the ACT power for other modes of operation. The scaling factor is represented as $^tRRDscheduled$ (^tRRDsch), which is the average scheduled row-to-row activate timing. Two examples of scaling activate power with different command spacings are shown. One example is when $^tRRDsch > {}^tRC$, and a second when the device is in bank interleave mode.

Figure 4: ACT-ACT Current with ^{t}RRDsch = 65.625ns
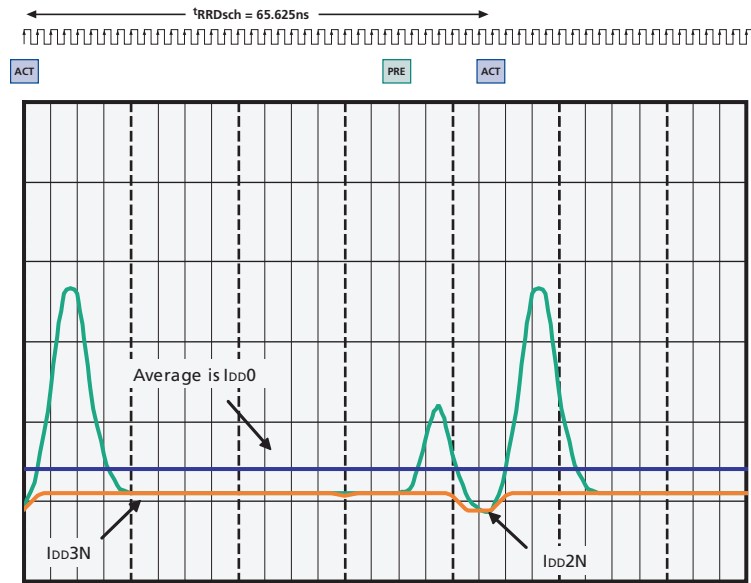
In Figure 4, the average ACT-ACT cycle time is greater than the specified ^{t}RC = 50.625ns. ^{t}RRDsch is stretched to 35 clock cycles, which is 65.625ns for a 533 MHz clock.

The active power can easily be scaled as the ratio of the actual ^{t}RRDsch value to the data sheet ^{t}RC condition. The calculation is as follows:

$$\text{Psch(ACT)} = \text{Pds(ACT)} \times \frac{^t\text{RC}}{^t\text{RRDsch}}$$

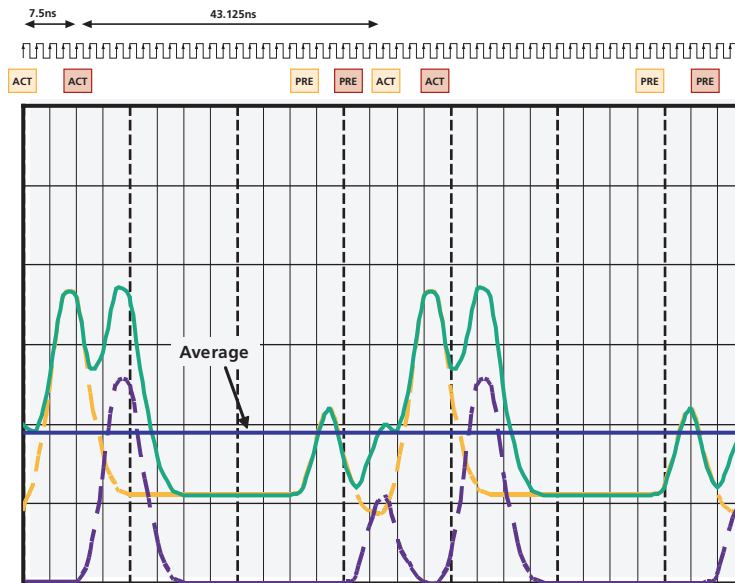$$\text{Psch(ACT)} = 63\text{mW} \times \frac{50.625\text{ns}}{65.625\text{ns}}$$

Psch(ACT) = 49mW

(Eq. 11)

Therefore, by changing the ACT-ACT time from 50.625ns to 65.625ns, the maximum activation power, Psch(ACT), drops from 63mW to 49mW. Note that this power is only the activation power and does not include the background power contributed by $I_{DD}2N$ and $I_{DD}3N$.

Because a DDR3 device has multiple banks, it is possible to have several open rows at one time. Therefore, it is also possible to have ACT commands closer together than ^{t}RC. Figure 5 on page 8 shows an example in which two banks are interleaved within 50.625ns, making the average ^{t}RRDsch = 25.3ns. Because ^{t}RRDsch is an average, it does not matter that some commands are spaced 7.5ns apart while others are 43.125ns apart (see Figure 5). The yellow current profile represents the first bank activated and includes the $I_{DD}3N$ component. This is only included in one instance on the device, even if other banks are open. The purple current profile, which represents the second bank activated, shows only the additional current introduced due to the second bank activated. The green curve represents the sum of the two banks.

Figure 5:   ACT-ACT Current for ^{t}RRDsch = 25.3ns

The calculation to determine the power consumption for the activation power is the same as before:

$$\text{Psch(ACT)} = 63\text{mW} \times \frac{50.625\text{ns}}{25.3\text{ns}}$$

Psch(ACT) = 126mW

(Eq. 12)

The maximum Psch(ACT) for two interleaved banks increases from 63mW to 126mW because twice the amount of ACT and PRE power is consumed when operating two banks compared to one.

With this basic equation, the ACT-PRE power can be calculated for any usage condition, from eight interleaved banks to one bank that is seldom opened.

Write Power

After a bank is open, data can be either read from or written to the DDR3 SDRAM. The two cases are similar. Figure 6 on page 9 illustrates an example of two WRITE commands utilizing BL = 8 operation.

Figure 6:   Current Profile – WRITEs
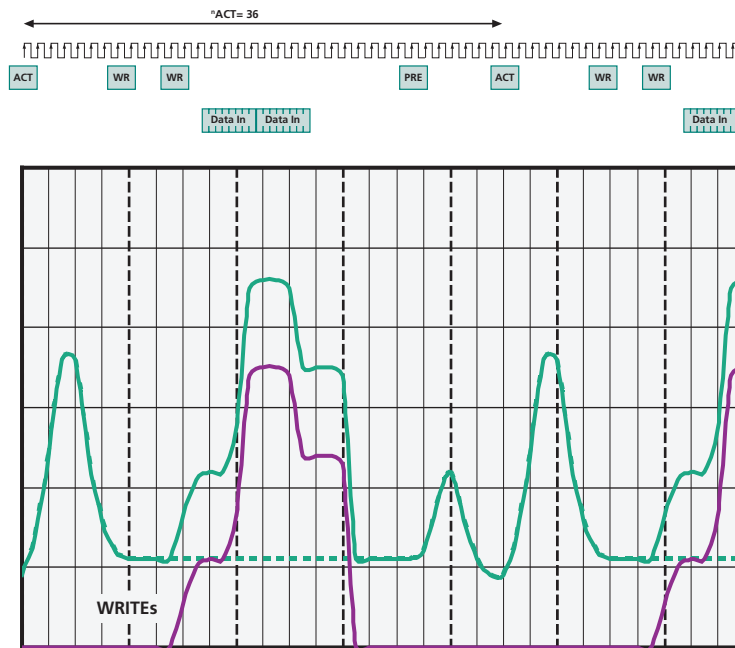
When several WRITEs are added between ACT commands, the consumption of current associated with the WRITE is IDD4W. To identify the power associated with only the WRITEs and not the standby current, IDD3N must be subtracted. The calculation for the data sheet write component of power, Pds(WR), is shown in Equation 13.

$Pds(WR) = (I_{DD}4W - I_{DD}3N) \times V_{DD}$

$Pds(WR) = (240mA - 75mA) \times 1.575V$

Pds(WR) = 260mW

(Eq. 13)

To scale the data sheet power to actual power based on command scheduling, it must be calculated as a ratio of the write bandwidth. This is noted as WRsch%, which is the total number of clock cycles that write data is on the bus (not WRITE commands) versus the total number of clock cycles. The WRsch% calculation for the example show in Figure 6 is shown in Equation 14.

$$WRsch\% = \frac{num\_of\_WR\_cycles}{n_{ACT}}$$

$$WRsch\% = \frac{8 \text{ cycles}}{36^{t}CK}$$

WRsch% = 22%

(Eq. 14)

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When the ratio of WRITEs is known, the power associated with the scheduled WRITEs, Psch(WR), can be easily calculated from the data sheet write power, as shown in Equation 15.

The data sheet conditions specify I$_{DD}$4W with a BL = 8. DDR3 devices may also operate with a BC = 4. However, internally the DDR3 DRAM continues operate as if it were doing BL = 8 WRITEs and masks off the last four data bits. Therefore, if a WRITE using BC = 4 is completed, it will require approximately the same amount of power as a WRITE with BL = 8 (four clock cycles). The multiplication of the (8/BL) at the end of the equation adjusts for this difference in burst length.

$$Psch(WR) = Pds(WR) \times WRsch\%$$

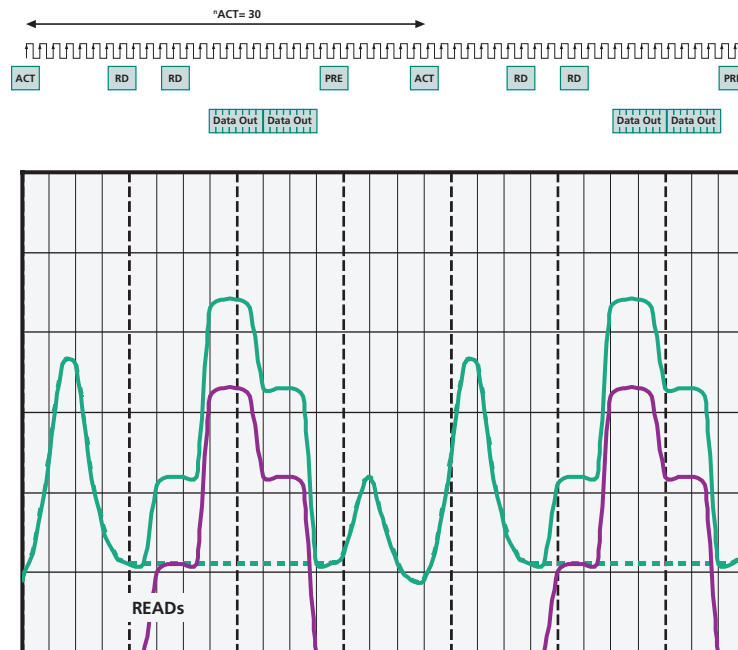$$Psch(WR) = 260mW \times 22\%$$

Psch(WR) = 57mW

<div align="right">(Eq. 15)</div>

Read Power

The power required to read data is similar to that needed to write data, as shown in Figure 7. A row is opened with an ACT command, and then a set of two BL = 8 READs is completed from columns in that row. After the READs are complete, the row is closed with a PRE command and the sequence is restarted.

Figure 7:   Current Profile – READs

The read current profile looks very similar to the write current profile. The average current is calculated exactly the same as in the write case, except I_{DD4R} is substituted for I_{DD4W}.

$Pds(RD) = (I_{DD4R} - I_{DD3N}) \times V_{DD}$

$Pds(RD) = (220mW - 75mA) \times 1.575V$

Pds(RD) = 228mW

<div align="right">(Eq. 16)</div>

To scale the data sheet power to actual power based on command scheduling, it must be calculated as a ratio of the read bandwidth. This is denoted as RDsch%, which is the total number clock cycles containing read data (not READ commands) that are on the data bus versus the total number of clock cycles. The RDsch% calculation is shown in Equation 15.

$$RDsch\% = \frac{num\_of\_RD\_cycles}{n_{ACT}}$$
$$RDsch\% = \frac{8 \text{ cycles}}{32^{t}CK}$$

RDsch% = 25%

<div align="right">(Eq. 17)</div>

After the ratio of READs is known, the power associated with the scheduled READs, Psch(RD), can be easily calculated from the data sheet read power in Equation 18.

$Psch(RD) = Pds(RD) \times RDsch\%$

$Psch(RD) = 228mW \times 25\%$

Psch(RD) = 57mW

<div align="right">(Eq. 18)</div>

I/O Termination Power

Psch(RD) and Psch(WR) are only part of the total power for read and write sequences. Data sheet specifications do not include output driver power or ODT power. These powers are system-dependent and must be calculated for each system.

DDR3 systems can vary greatly depending on the application's density and form factor requirements. A typical small density system is shown in Figure 8. The data bus connects the controller to two DDR3 DRAM. Additionally, the controller and the DRAM utilize ODT for the data lines so no external passive components are required for this example system.

Figure 8: Typical System DQ Termination
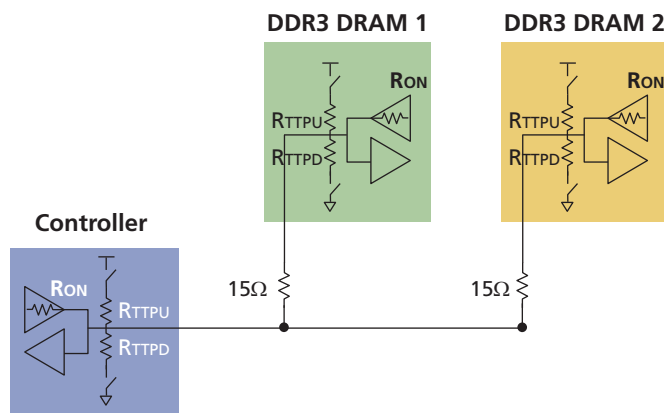
The drivers in the system have an impedance of R_{ON} which pulls the bus towards V_{DDQ} for a "1" or V_{SSQ} for a "0". The termination on the die is functionally a pull-up resistor and a pull-down resistor where $R_{TTPU} = R_{TTPD} = 2 \times R_{TT}$. R_{TT} is the selected Thevenin equivalent termination value selected for the device.

A simple termination scheme for the example system is shown in Table 3 on page 12. Because this is a point-to-two-point system, all output drivers are set to 34Ω and terminations are set.

Table 3: Termination Configuration

	Controller		DRAM 1		DRAM 2	
	R_{ON}	R_{TT}	R_{ON}	R_{TT}	R_{ON}	R_{TT}
WRITEs to DRAM 1	34Ω	Off	Off	120Ω	Off	30Ω
READs from DRAM 1	Off	75Ω	34Ω	Off	Off	30Ω
WRITEs to DRAM 2	34Ω	Off	Off	30Ω	Off	120Ω
READs from DRAM 2	Off	75Ω	Off	Off	34Ω	Off

Two methods can be used to calculate the power consumed by the output driver and ODT. One is to simulate the system data bus using SPICE models of the components and then average the power consumed over a sufficiently long pattern of pseudo-random data. A simpler method, however, is to calculate the DC power of the output driver against the termination. This is usually not worst-case, but it provides a first-order approximation of the output power.

The I/O powers that must be calculated are:

- **PdqRD:** The output driver power when driving the bus
- **PdqWR:** The termination power when terminating a WRITE to the DRAM
- **PdqRDoth:** The termination power when terminating a READ from another DRAM
- **PdqWRoth:** The termination power when terminating write data to another DRAM

The nominal DRAM I/O termination DC power for the memory system can be calculated using Thevenin equivalent circuits (see Figure 9 and Figure 10). The resultant I/O termination DC power values for the DRAM, per I/O pin, are listed in Table 4 on page 14. The controller and board series termination powers are not accounted for in the DRAM I/O termination power values even though they are shown for reference.
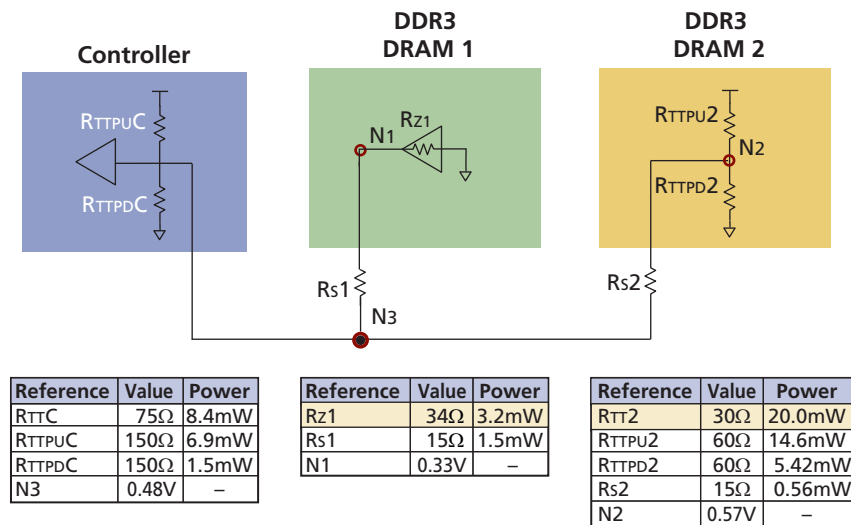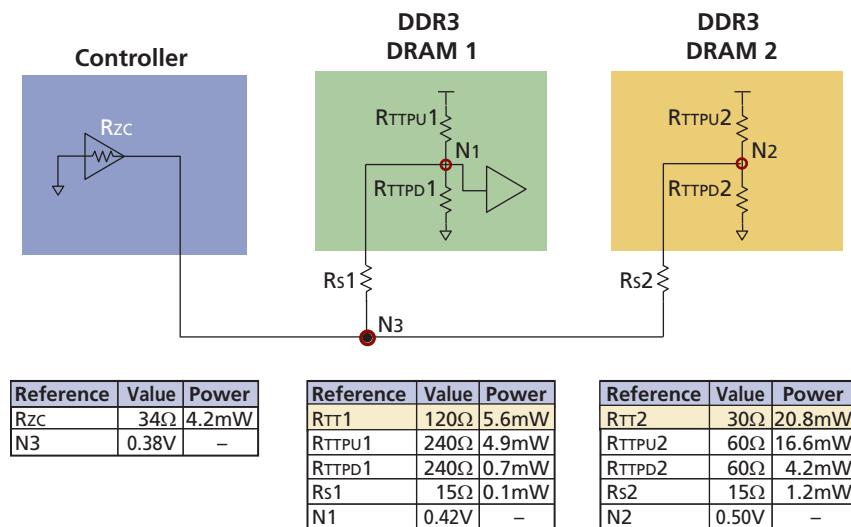
Figure 9:   DRAM READ

Reference	Value	Power
R$_{TT}$C	75Ω	8.4mW
R$_{TTPU}$C	150Ω	6.9mW
R$_{TTPD}$C	150Ω	1.5mW
N3	0.48V	–

Reference	Value	Power
R$_{Z1}$	34Ω	3.2mW
R$_{S1}$	15Ω	1.5mW
N1	0.33V	–

Reference	Value	Power
R$_{TT}$2	30Ω	20.0mW
R$_{TTPU}$2	60Ω	14.6mW
R$_{TTPD}$2	60Ω	5.42mW
R$_{S2}$	15Ω	0.56mW
N2	0.57V	–

Figure 10:   DRAM WRITE

Reference	Value	Power
R$_{ZC}$	34Ω	4.2mW
N3	0.38V	–

Reference	Value	Power
R$_{TT}$1	120Ω	5.6mW
R$_{TTPU}$1	240Ω	4.9mW
R$_{TTPD}$1	240Ω	0.7mW
R$_{S1}$	15Ω	0.1mW
N1	0.42V	–

Reference	Value	Power
R$_{TT}$2	30Ω	20.8mW
R$_{TTPU}$2	60Ω	16.6mW
R$_{TTPD}$2	60Ω	4.2mW
R$_{S2}$	15Ω	1.2mW
N2	0.50V	–

Table 4:   Nominal I/O Termination Power Consumption

	DC Power	
	DRAM 1	**DRAM 2**
DRAM READ	pdqRD = 3.2mW/DQ	pdqRDoth = 24.9mW/DQ
DRAM WRITE	pdqWR = 5.6mW/DQ	pdqWRoth = 20.8mW/DQ

To calculate the power for output or termination on the DRAM, the power per DQ must be multiplied by the number of DQ and strobes on the device (num_DQR). For write termination, data masks must also be included in the sum of the total number of write signals that must be terminated (num_DQW). This will vary depending on data width of the DRAM.

Equation 19 on page 14 calculates the DRAM power for the following four I/O buffer operations:

- **Pds(DQ):** DRAM output driver power when driving the bus
- **Pds(termW):** DRAM termination power when terminating a WRITE to the DRAM
- **Pds(termRoth):** DRAM termination power when terminating a READ from another DRAM
- **PPds(termWoth):** DRAM termination power when terminating write data to another DRAM

$$Pds(DQ) = Pdq(RD) \times num\_DQR$$
$$Pds(termW) = Pdq(WR) \times num\_DQW$$
$$Pds(termRoth) = Pdq(RDoth) \times num\_DQR$$
$$Pds(termWoth) = Pdq(WRoth) \times num\_DQW$$

(Eq. 19)

To illustrate how the power is calculated, an assumption using a x8 device is shown. For this example, num_DQR includes eight DQ and two DQS signals for a total of ten, whereas num_DQW totals 11 to account for the addition of the data mask. The DC power values from Table 4 on page 14 are also used, and the results are presented in Equation 20.

$$Pds(DQ) = 5.3mW \times 10 = 53mW$$
$$Pds(termW) = 0mW \times 11 = 0mW$$
$$Pds(termRoth) = 0mW \times 10 = 131mW$$
$$Pds(termWoth) = 13.2mW \times 11 = 145mW$$

(Eq. 20)

To complete the I/O and termination power calculation, the 100 percent usage data sheet specification must be derated based on the data bus utilization. The read and write utilization has already been provided as RDschd% and WRschd%. Two additional terms are required to cover the termination case for data to/from another DRAM. These are termRDsch% (terminating read data from another DRAM) and termWRsch% (terminating write data to another DRAM). The power based on command scheduling is then calculated as:

$$Psch(DQ) = Pds(DQ) \times RDsch\%$$

$$Psch(termW) = Pds(termW) \times WRsch\%$$

$$Psch(termRoth) = Pds(termRoth) \times termRDsch$$

$$Psch(termWoth) = Pds(termWoth) \times termWRsch$$

(Eq. 21)

Sample calculations showing how to determine the output and termination percentages are provided in "DDR3 Power Spreadsheet Usage Example" on page 20.

Refresh Power

Refresh is the final power component that must be calculated for the device to retain data integrity. DDR3 memory cells store data information in small capacitors that lose their charge over time and must be recharged. The process of recharging these cells is called refresh.

The specification for refresh in the DDR3 data sheet is $I_{DD}5$. $I_{DD}5$ assumes the DRAM is operating continuously at minimum REFRESH-to-REFRESH command spacing, ^tRFC (MIN). During this operation, the DRAM is also consuming $I_{DD}3N$ standby current. Thus, to calculate only the power due to refresh, $I_{DD}3N$ must be subtracted, as shown in Equation 22.

$$Pds(REF) = (I_{DD}5 - I_{DD}3N) \times V_{DD}$$

$$Pds(REF) = (255mA - 75mA) \times 1.575V$$

Pds(REF) = 284mW

(Eq. 22)

However, REFRESH operations are typically distributed evenly over time at a refresh interval of ^tREFI. Thus, the scheduled refresh power, Psch(REF), is the ratio of ^tRFC (MIN) to ^tREFI, multiplied by Pds(REF), as shown in Equation 23.

$$Psch(REF) = Pds(REF) \times \frac{^tRFC\ (MIN)}{^tREFI}$$

$$Psch(REF) = 284mW \times \frac{110ns}{7.8us}$$

Psch(REF) = 4mW

(Eq. 23)

Power Derating

Thus far, the power calculations have assumed a system operating at worst-case V_{DD}. They have also assumed the clock frequency in the system is the same as the frequency defined in the data sheet. The resulting power is denoted as Psch(XXX). Most systems, however, operate at different voltages or clock frequencies than the ones defined in the data sheet. Each of the power components must be derated to the actual system conditions, with the resulting power denoted as Psys(XXX).

The following section explains how to derate each of the power components to an actual system.

Voltage Supply Scaling

Most applications operate near the nominal V_{DD}, not at the absolute maximum V_{DD}. The only power parameters that do not scale with V_{DD} are the data I/O and termination power because the system V_{DD} is already assumed when the initial power is calculated.

On DRAM, power is typically related to the square of the voltage. This is because most of the power is dissipated by capacitance, with $P = CV^2f$ where C = internal capacitance, V = supply voltage, and f = frequency of the clock or command (see "Frequency Scaling" on page 16). Thus, to scale power to a different supply voltage:

$$Psys(XXX) = Psch(XXX) \times \left(\frac{V_{DD}\ used}{MAX\ spec\ V_{DD}} \right)^2$$

(Eq. 24)

Frequency Scaling

Many power components, such as Psch(ACT_PDN), Psch(ACT_STBY), Psch(PRE_STBY), Psch(WR), and Psch(RD), are dependent on the clock frequency at which a device operates. Psch(PRE_PDN) is dependent on a slow or fast exit time. If a fast exit time is selected, the power will scale with frequency. However, if a slow exit time is selected, there is no scaling because the clock is disabled during power-down mode.

Similarly, Psch(REF) does not scale with clock frequency, and Psch(ACT) is dependent on the interval between ACT commands, rather than clock frequency.

The power for components dependent on an operating frequency can be scaled for actual operating frequency:

$$Psys(XXX) = Psch(XXX) \times \frac{freq\_used}{spec\_freq}$$

(Eq. 25)

The freq_used is the actual clock frequency at which a device operates in the system. The spec_freq is the clock frequency at which the device was tested during the I_{DD} tests. This information is provided in the test condition notes in a data sheet. The test condition notes also describe tests at the minimum clock rate for a specific CAS latency, and that value is specified under the ^tCK parameter.

The combination of all V_{DD} and clock frequency scaling is presented in Equation 26.

$$Psys(PRE\_PDN) = Psch(PRE\_PDN) \times \left[\frac{V_{DD}\ used}{MAX\ spec\ V_{DD}} \right]^2 \qquad if\ MRS12 = 0$$

$$= Psch(PRE\_PDN) \times \left[\frac{freq\_used}{spec\_freq} \right] \times \left[\frac{V_{DD}\ used}{MAX\ spec\ V_{DD}} \right]^2 \qquad if\ MRS12 = 1$$

$$Psys(ACT\_PDN) = Psch(ACT\_PDN) \times \left[\frac{freq\_used}{spec\_freq} \right] \times \left[\frac{V_{DD}\ used}{MAX\ spec\ V_{DD}} \right]^2$$

$$Psys(PRE\_STBY) = Psch(PRE\_STBY) \times \left[\frac{freq\_used}{spec\_freq} \right] \times \left[\frac{V_{DD}\ used}{MAX\ spec\ V_{DD}} \right]^2$$

$$Psys(ACT\_STBY) = Psch(ACT\_STBY) \times \left[\frac{freq\_used}{spec\_freq} \right] \times \left[\frac{V_{DD}\ used}{MAX\ spec\ V_{DD}} \right]^2$$

$$Psys(ACT) = Psch(ACT) \times \left[\frac{V_{DD}\ used}{MAX\ spec\ V_{DD}} \right]^2$$

$$Psys(WR) = Psch(WR) \times \left[\frac{freq\_used}{spec\_freq} \right] \times \left[\frac{V_{DD}\ used}{MAX\ spec\ V_{DD}} \right]^2$$

$$Psys(RD) = Psch(RD) \times \left[\frac{freq\_used}{spec\_freq} \right] \times \left[\frac{V_{DD}\ used}{MAX\ spec\ V_{DD}} \right]^2$$

$$Psys(REF) = Psch(REF) \times \left[\frac{V_{DD}\ used}{MAX\ spec\ V_{DD}} \right]^2$$

(Eq. 26)

Calculating Total DRAM Power

The tools are now in place to calculate the system power for any usage condition. The last task is to put them together. The various system power subcomponents are summed together, as shown in Equation 27.

$$\begin{aligned} Psys(TOT) = \ & Psys(PRE\_PDN) + Psys(PRE\_STBY) \\ & + Psys(ACT\_PDN) + Psys(ACT\_STBY) + Psys(WR) \\ & + Psys(RD) + Psys(REF) + Psys(DQ) \\ & + Psys(termW) + Psys(termRoth) + Psys(termWoth) \end{aligned}$$

(Eq. 27)

Having compensated for all primary variables that can affect device power, the total power dissipation of a DDR3 device operating under specific system usage conditions has now been calculated.

DDR3 Power Spreadsheet

Calculating all of these equations by hand can be tedious. For this reason, Micron has published an online worksheet to simplify the process. Micron's DDR3 SDRAM System-Power Calculator, as well as detailed instructions for its use, are available on Micron's Web site at www.micron.com/systemcalc. An example of using the system-power calculator is provided in "DDR3 Power Spreadsheet Usage Example" on page 20.

To utilize the online spreadsheet, enter the device data sheet conditions on the "DDR3 Spec" tab. Starting values are provided, but it is important to verify all data sheet parameters prior to using the spreadsheet. Note that multiple speed bins and DRAM densities are included and that correct inputs are required for each column utilized.

After the data sheet values are entered, the actual DRAM configuration to be used for the power calculations is selected on the "DDR3 Config" tab, as shown in Figure 11. The density, I/O configuration, and speed grade are selected with pull-down menus. In addition, the mode register configuration is selected for the differential strobe, TDQS, and PD exit mode. These inputs correctly configure the calculator for a specific DRAM based on the data input on the "DDR3 Spec" worksheet.

Figure 11:   Spreadsheet – DRAM Configuration Tab

DRAM Density	1Gb ▼
Number of DQs per DRAM	x8 ▼
Speed Grade	-187E ▼
Mode Register Bit 12: PD Exit Mode	1:Fast ▼

After the DRAM configuration has been selected, the system operating conditions are input on the "System Config" tab, as shown in Figure 12 on page 19. The actual system operating V_{DD} and clock frequency are entered. Output power consumption and bus utilization are also entered, along with CKE conditions.

Figure 12:   Spreadsheet – System Configuration Tab

	System V$_{DD}$	1.5	V	
	System CK frequency	533	MHz	
	Burst length	8		Must be either 4 or 8.
PdqRD	DDR3 SDRAM output power per individual DQ on this DRAM	5.3	mW	This value is the output driver power per DQ on the DRAM. It is specific to each system design and must be calculated based on the termination scheme.
PdqWR	DDR3 SDRAM termination power per individual DQ during WRITEs to this DRAM	0	mW	This value is the output driver power per DQ on the DRAM. It is specific to each system design and must be calculated based on the termination scheme.
PdqRDoth	DDR3 SDRAM termination power per individual DQ during READs from other DRAM	0	mW	This value is the output driver power per DQ on the DRAM. It is specific to each system design and must be calculated based on the termination scheme.
PdqWRoth	DDR3 SDRAM termination power per individual DQ during WRITEs to other DRAM	13.2	mW	This value is the output driver power per DQ on the DRAM. It is specific to each system design and must be calculated based on the termination scheme.
BNK_PRE%	The percentage of time that all banks on the DRAM are in a precharged state	20%		
CKE_LO_PRE%	Percentage of the all bank precharge time for which CKE is held LOW	0%		
CKE_LO_ACT%	Percentage of the at least one bank active time for which CKE is held LOW	0%		
PH%	Page hit rate	0%		
RDsch%	The percentage of clock cycles which are outputting read data from the DRAM	15%		
WRsch%	The percentage of clock cycles which are inputting write data to the DRAM	5%		
termRDsch%	The percentage of clock cycles which are terminating read data to another DRAM	0		Must be 0% for a 1-rank system.
termWRsch%	The percentage of clock cycles which are terminating write data to another DRAM	5%		Must be 0% for a 1-rank system.
^{t}RRDsch	The average time between ACT commands to this DRAM (includes ACT to same or different banks in the same DRAM device)	37.5	ns	This is calculated from page hit rate read/write bus utilization.
No entry is necessary.

To assist calculating ^{t}RRDsch, one new parameter is added to this table which has not been previously discussed. This parameter is the PageHit% rate. The PageHit% is the percentage of READ and WRITE commands executed to an open row that has already been read from or written to previously divided by the total number of READ and WRITE commands. The PageHit% is application/system dependent. Desktop and notebook applications tend to have a high PageHit% while server and networking applications tend to have a very low PageHit%.

The PageHit% is used to calculated ^{t}RRDsch, as shown in Equation 28.

$$^{t}RRDsch = \left[\frac{BL / 2}{(RDsch\% + WRsch\%) \times f_{CLOCK}} \right] / (1 - PageHit\%)$$

(Eq. 28)

After all the inputs are entered, the actual DRAM device power derated to the system conditions can be found on the "Summary" tab. Note that the interim power calculations for data sheet power and scheduled power can also be found on the "Power Calcs" worksheet.

Data Sheet Specifications

Table 5:   Data Sheet Assumptions for Micron's 1Gb DDR3-1067

Parameter/Condition		Symbol	-187E x8	-187E x16	Units
Operating current: One bank active-precharge		I_{DD}0	115	140	mA
Precharge power-down current	Fast PDN Exit; MRS[12] = 0	I_{DD}2P	25	25	mA
	Slow PDN Exit; MRS[12] = 1		10	10	
Precharge standby current		I_{DD}2N	65	65	mA
Active power-down current		I_{DD}3P	45	45	mA
Active standby current		I_{DD}3N	75	80	mA
Operating burst read current		I_{DD}4R	220	280	mA
Operating burst write current		I_{DD}4W	240	350	mA
Burst refresh current		I_{DD}5	255	255	mA

Notes: 1. I_{DD} is dependent on output loading, cycle rates, I_{OUT} = 0mA; ODT disabled.
          2. Refer to the data sheet for the most current information and test conditions.

DDR3 Power Spreadsheet Usage Example

An example for calculating DDR3 power in a system environment is shown below. The system assumptions are for a two-rank system with a 32-bit data bus as shown in Figure 13. This system is populated with 1Gb DDR3-1067 DRAM. The controller (shown in purple) drives a common command/address bus to all four DRAM. The DRAM are divided into two ranks with one rank shown in green and the second rank shown in orange. Each rank is driven by a unique chip select. DRAM are selected in a x16 I/O configuration to support the 32-bit controller data bus.

Total data bus for this example is 80 percent with read data utilizing 50 percent of the bandwidth and write data utilizing 30 percent of bandwidth. All data bus terminations follow the guidelines shown previously in Table 3 on page 12. Because there are two ranks, it is assumed that each DRAM is accessed uniformly.

To support this bandwidth, a burst length of eight is assumed with a page hit rate of 50 percent. Based on the high bus utilization, no CKE power management is assumed, and all banks precharged occurs only 20 percent of the time.

Figure 13: Mobile/Desktop System
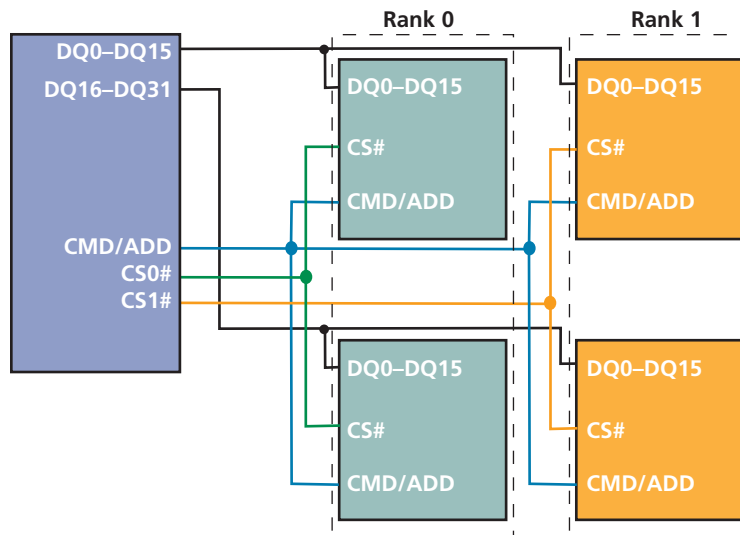
Note: Total data bus utilization = 80 percent (50 percent read data/30 percent write data).

To utilize the DDR3 Power Calculator spreadsheet, the IDD data sheet values must be loaded into the "DDR3 Spec" tab. After these values are verified, the DRAM utilized in the system is selected using the pull-down menus on the "DRAM Config" tab as shown in Figure 14 on page 21.

Figure 14: DRAM Configuration

DRAM Density	1Gb
Number of DQs per DRAM	x16
Speed Grade	-187E
Mode Register Bit 12: PD Exit Mode	1:Fast

After the DRAM is configured, the system implementation of the DRAM must be set using the "System Config" tab as shown in Figure 15. The I/O and termination powers are system dependent. This example aligns to those calculated in Table 4 on page 14. Because this example system contains two ranks of memory, each DRAM rank is assumed to consume half the total data bandwidth. Thus, each DRAM has a READ utilization of 25 percent and a WRITE utilization of 15 percent. The termination scheme also requires each DRAM to terminate the other DRAM's WRITE data bandwidth which is also 15 percent.

With this information and the PageHit%, the spreadsheet calculates the average time between ACT commands of ^{t}RRDsch = 37.5ns.

Figure 15: System Configuration

System V$_{DD}$	1.5	V
System CK frequency	533	MHz
Burst length	8	
PdqRD	5.3	mW
PdqWR	0	mW
PdqRDoth	0	mW
PdqWRoth	13.2	mW
BNK_PRE%	20%	
CKE_LO_PRE%		
CKE_LO_ACT%	0%	
PH%	50%	
RDsch%	25%	
WRsch%	15%	
termRDsch%	0%	
termWRsch%	15%	
^{t}RRDsch	37.5	ns

After all the assumptions are entered into the spreadsheet, it calculates each subcomponent of power and derates it to the system use condition. The results are shown on the "Summary" tab as shown in Figure 16. During the system conditions, each DDR3 DRAM utilizes 114mW of power for background operations, 123mW of power for activating rows, and 199mW of power for reading and writing data.

Therefore, each DRAM will consume approximately 436mW of total power. Because the calculations are completed on a per-DRAM basis, and the data was assumed to be uniformly distributed amongst all of the DRAM in the system, the total memory subsystem power can be approximated as four times 436mW, or 1.7W.

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Figure 16:   Power Consumption Summary

Psys(PRE_PDN)	0.0	mW
Psys(PRE_STBY)	18.6	mW
Psys(ACT_PDN)	0.0	mW
Psys(ACT_STBY)	91.4	mW
Psys(REF)	3.5	mW
Total Background Power	**113.5**	**mW**
Psys(ACT)	123.2	mW
Total Activate Power	**123.2**	**mW**
Psys(WR)	57.8	mW
Psys(RD)	71.4	mW
Psys(DQ)	26.5	mW
Psys(TERM)	43.6	mW
Total RD/WR/Term Power	**199.3**	**mW**
Total DDR3 SDRAM Power	**435.9 mW**	

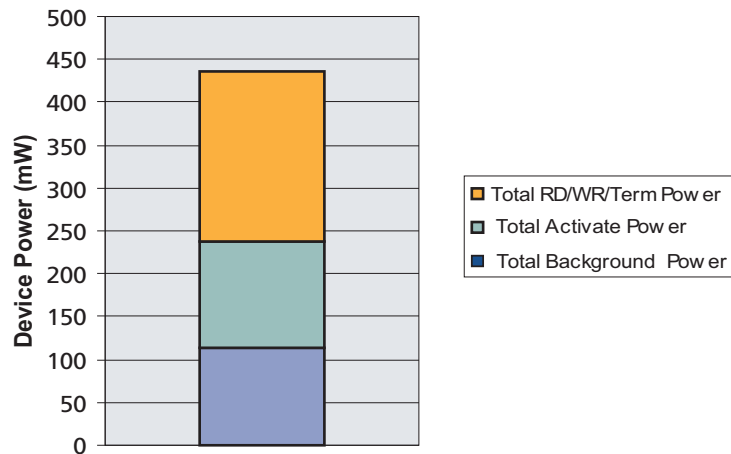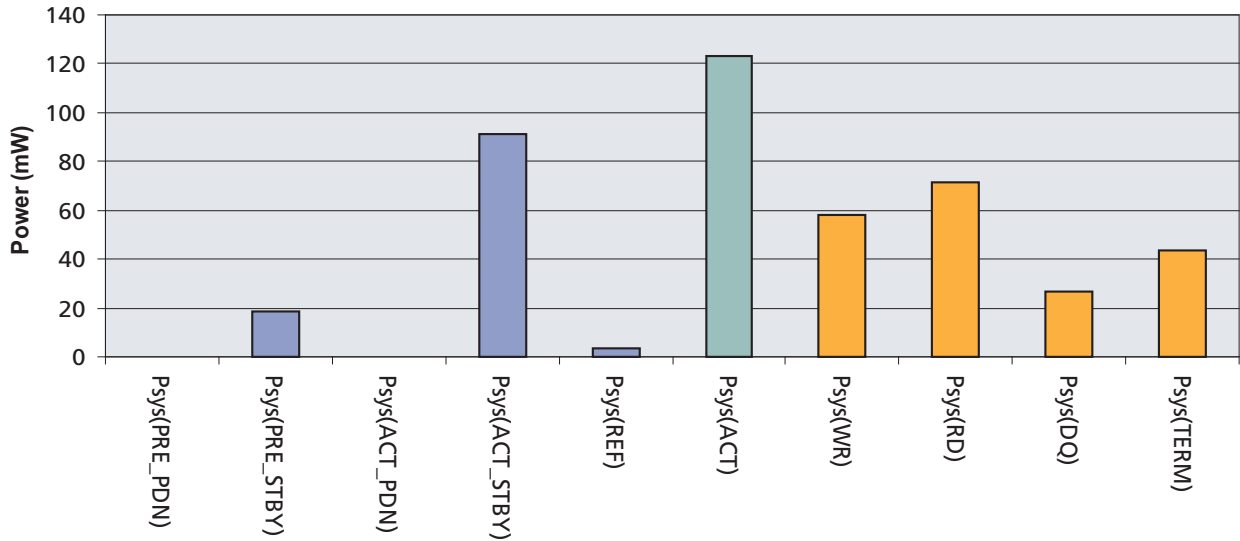**Figure 17:   Power Consumption per Device**

Figure 18: Power Consumption Breakout

Summary

When relying on a data sheet alone, it can be difficult to determine how much power a DDR3 device will consume in a system environment. However, by understanding the data sheet and how a DDR3 device consumes power, it is possible to create a power model based on system usage conditions. Such a model can enable system designers to experiment with various memory access schemes to determine the impact on power consumption—that is, more aggressive use of power-down (CKE = LOW) or changes to data access patterns (page hit percentages). In short, system designers can use this tool to estimate realistic power requirements for DDR3 devices and adjust a system's power delivery and thermal budget accordingly, optimizing system performance.