Prasad Venugopal, Systems Design Manager, PLX Technology

Overview

This white paper describes the need for receiver equalization in printed circuit board environments. The focus is on receiver equalization for serial links used on printed circuit boards for PCI Express Gen 2 signaling and PCI Express switches from PLX Technology.

Problem

PCI Express Gen 2 serial links carry data signals at 5 Gb/s in a differential format. A clock and data recovery (CDR) circuit recovers a clock from this data and uses this clock to sample the data at the receiver. In order for the CDR to recover the data correctly, every bit should have sufficient margin around the sampling point in terms of signal level and time (set-up and hold with respect to the CDR clock edge). This margin is measured by looking at the eye-diagram of the data at the receiver.

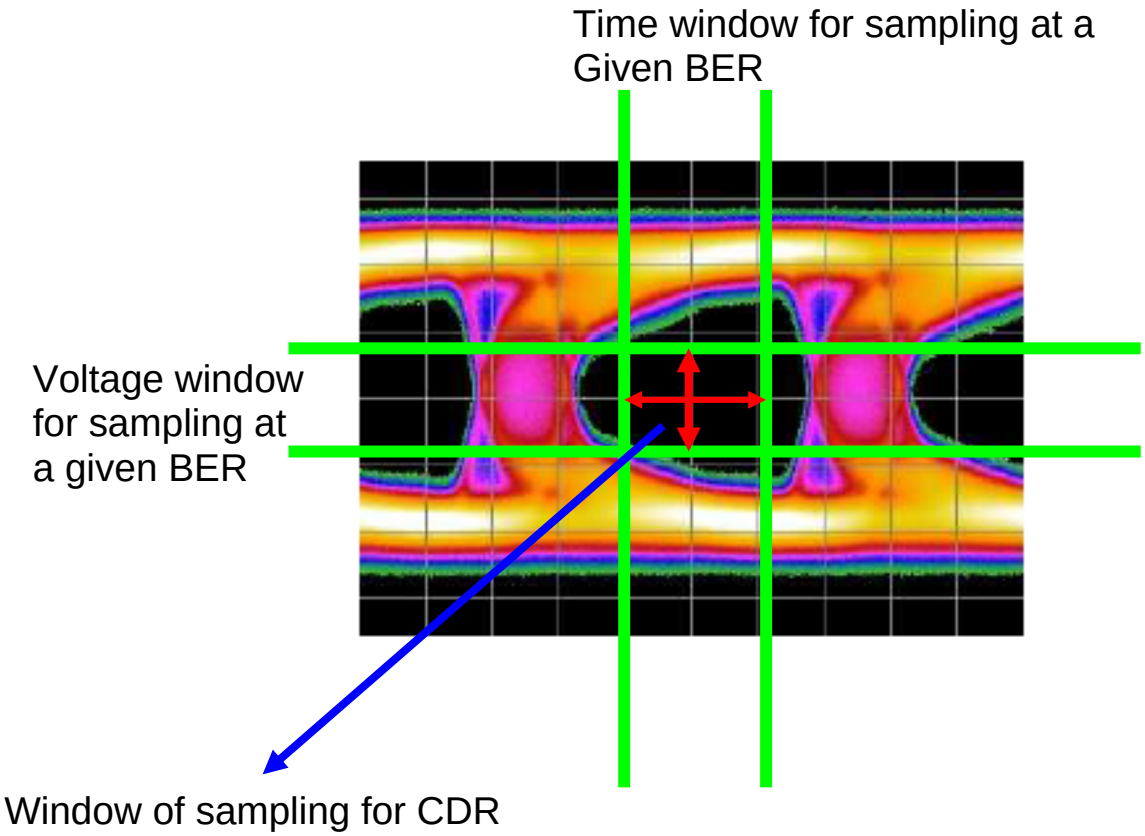

Figure 1. Eye Diagram

As shown in Figure 1 above, the eye diagram indicates the margin available for the CDR to sample data. The width (time margin) and height (voltage margin) can be related to the BER. The larger the margins, the smaller the bit error rate. Insufficient margins as indicated by poor eye quality indicate that the sampling will not be optimal and will lead to bit errors.

In PCI Express Gen 2 signaling, the data being transmitted is 8B/10B encoded and signaling is non-return-to-zero (NRZ). The run-length limitation of 8B/10B encoding guarantees a low-frequency of 500 MHz for data signals. The NRZ signaling guarantees the fundamental frequency of data signals will be 2.5 GHz. The rise times and fall times of these signals are approximately 20% of the bit period. These rise and fall times lead to higher frequency content than the fundamental data rate. In order to maintain the signal integrity of these broadband signals, from the transmitter through the channel and into the receiver, the highest frequency of interest the channel will need to pass with minimum attenuation will be about 3x (7.5 GHz) the fundamental frequency.

The channels are typically made of stripline and/or microstrip transmission lines, constructed out of 0.5 oz. copper, 5-8 mils wide, etched on substrates like FR-4 and Nelco 4000. The frequency range of interest, as mentioned above, is between 250 MHz – 7.5 GHz and the loss characteristic of the channel in this range is what determines the quality of the signal at the receiver.

Losses at these signaling rates are due to skin-effect losses, dielectric losses, reflection losses, radiation losses, proximity effect current redistribution losses and surface roughness losses. This paper will focus on skin effect losses and dielectric losses.

Skin effect losses and dielectric losses combine to create a frequency response of the channel that tends to attenuate the high frequency components more in comparison to lower frequency components. The lower frequency components therefore pass through the channel with lower attenuation. The skin effect losses are proportional to the square root of the frequency and the dielectric losses are proportional to the frequency.

Due to these losses, the transmitted signal loses its sharp edges that correspond to high frequency components. Longer run-lengths in the data (lower frequency) lose less amplitude compared to the lower run-lengths (higher frequency) and therefore the zero crossings of the signal are different for different run-lengths. Hence, this leads to jitter, making the signal at the receiver have a smaller eye than what was transmitted. In some cases, there is no eye at all because the differential signals do not cross due to frequency dependent losses. Eye closure due to Data Dependant Jitter, DDJ, caused by the channel losses attenuating high frequency components more than low frequency components as mentioned above, can be reduced by receiver equalization. A reduction in the data eye reduces the sampling aperture available to the receiver data recovery circuit. Figure 2 (below) shows a signal at the transmitter and Figure 3 (below) shows a signal at the end of a lossy transmission line. The two traces shown are differential signals.

Since the differential signals do not cross, a receiver will not be able to recover bits as is. With the PLX receiver equalization enabled, the receiver compensates for this distortion and recovers bits correctly. Receiver equalization can overcome the deleterious effects due to the aforementioned frequency dependent losses and provide the receiver with an open eye.

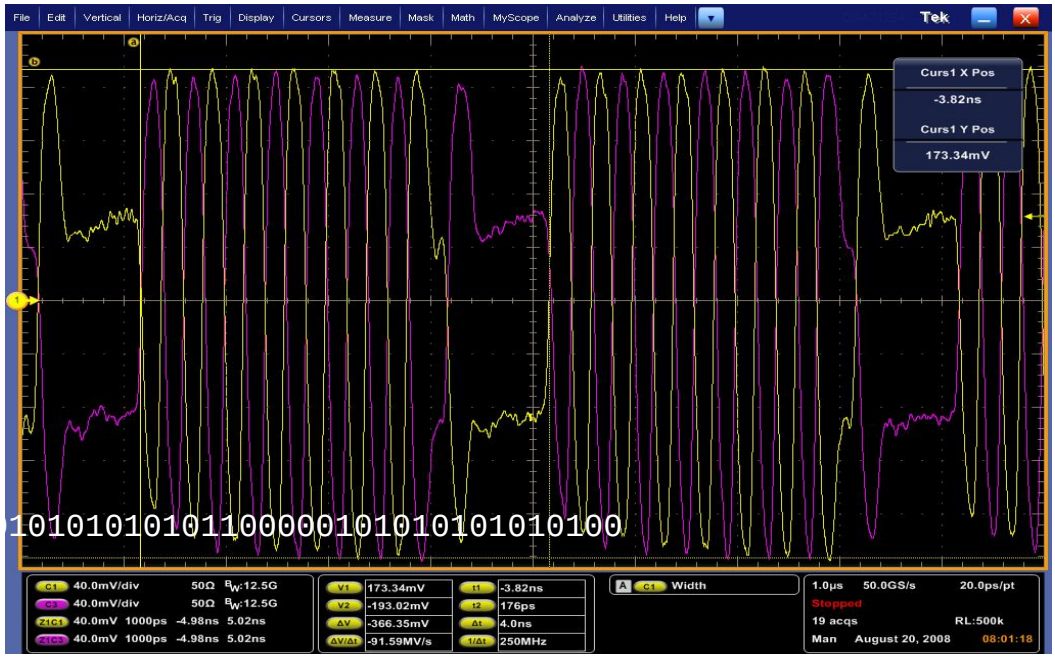

Figure 2. Transmitted signal at the input to a lossy transmission line

Figure 3. Received signal at the input to receiver at the end of a lossy transmission line

Equalization Curves

PLX switches have receiver equalization and the response of the equalizer is shown in Figure 4 below. At higher settings, the equalizer provides lower gain for lower frequencies and higher gain for higher frequencies. This counteracts the transmission medium behavior that has the opposite behavior – the transmission medium has higher gain (lower losses) for lower frequencies and lower gain (higher losses) for higher frequencies. This "equalization" of gains tends to create an eye at the receiver that is open and with low jitter. Please refer to the White Paper, "PLX PCI Express over 30" of Legacy Backplane", for details on an actual simulation with a backplane and the results of different settings for the receiver equalizer.

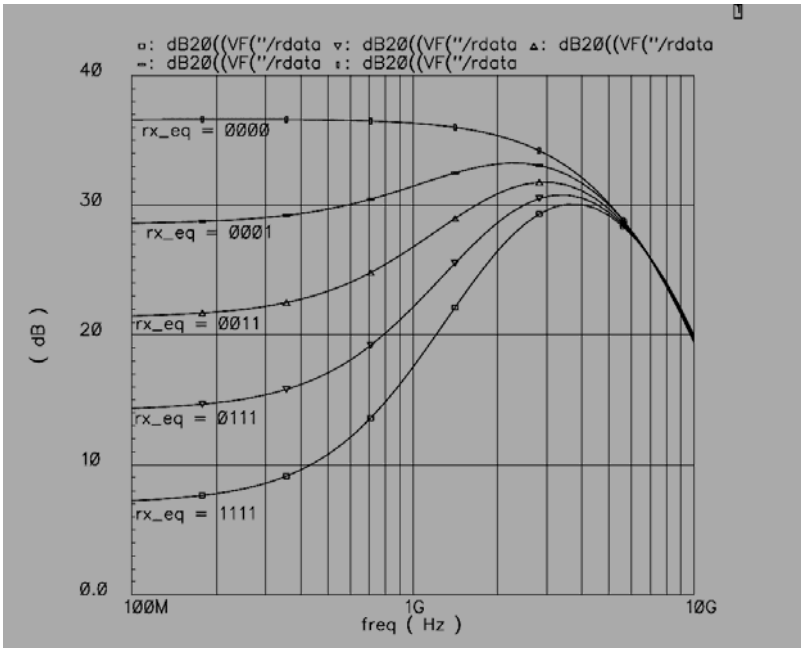

Figure 4. Receiver equalization curves

Considerations

Receiver equalization, while useful in lossy environments as described above, can overcompensate in low loss environments and result in receiver eye margins being adversely affected. Since receiver equalization is a band-pass filter and it provides gain in the frequency ranges that have the most attenuation, it can also amplify noise within the same range. In noisy environments, transmit pre-emphasis and receiver equalization may be the ideal combination. In Figure 2 above, the transmit pre-emphasis can be seen in the waveform.

How to use equalization for PLX switches

PLX provides a model for its switch transmit and receive buffers that correctly model the transmit and receive equalization. A user supplied channel model is inserted between the transmitter and receiver and simulations can be performed to determine the optimum settings. The output of the receiver at the internal node to the clock and data recovery circuit can be observed in simulation.