Introduction
to
SMPS Control
Techniques

Welcome to the Introduction to SMPS Control Techniques Web seminar.

The following slides will introduce you to some of the basic control methods that have been developed for use in SMPS applications.

SMPS designs have traditionally been implemented with analog pwm controllers. These controllers were built with comparators and op-amps and within their circuitry the control algorithms were implemented; either Voltage mode or Current mode.

Session Agenda

- **Voltage versus Current Mode Control**
- **P.I.D Control**
- **Feed-Forward techniques**
- **Digital SMPS Control Techniques**
- **Switching Methodology**
- **Control Loop Stability**

This is the agenda for this course. We will discuss the differences between voltage and current mode control.

Then we will cover the PID control algorithm.

Feed-Forward techniques and their application to digital control systems are discussed.

The method and timing of the transistor switching and the associated effect on SMPS design is detailed.

We conclude this presentation by covering some major issues that relate to insuring stable control loops.

Classic Analog SMPS Control Techniques

- **Voltage Mode Control: The difference between the desired and actual output voltages (error) controls the <u>voltage</u> applied across the inductor.**

- **Current Mode Control: The difference between the desired and actual output voltages (error) controls the peak inductor <u>Current</u>.**

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The first approach developed to control SMPS applications is called "Voltage Mode". Voltage mode is intuitive, the actual output voltage is compared to the desired output voltage and the difference (error) is used to adjust the pwm duty cycle to control the voltage across the inductor.

Later, Current-Mode control was developed to correct some issues known with voltage mode. Current-mode uses the error between the desired and actual output voltages to control the peak current through the inductor.

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Voltage Mode Advantages

- **Voltage sensing is easier then current sensing: Less noise, Less power loss, Less cost, More resolution.**
- **Single feedback path is easier to design.**

Voltage mode control, where the output voltage is the control endpoint, is conceptually easier to understand than current mode control.

Sensing voltages is easy. Typically a resistor divider scales the output voltage to a value that is read by an ADC (Analog to Digital Converter), or is presented to an analog comparator. The measured voltage levels are usually in the one to five volt range, so signal to noise ratios and resolution are not an issue.

The voltage mode control only needs to monitor the output voltage so only one feedback path is required, thus simplifying the design of the converter.

Current Mode Advantages

- **Faster response due to single "Pole" system. Output capacitor is removed from feedback path.**

- **Responds immediately to input voltage changes.**

- **Inherent cycle by cycle current limiting.**

Current mode (historically) has faster output response than voltage mode because the current in the inductor is controlled instead of the output voltage which is measured on the output capacitor. Voltage mode is a two pole feedback loop while current mode is a one pole feedback loop. The single pole of a current mode control loop requires less high frequency roll-off to maintain loop stability.

Inductor current responds directly with changes in input and output voltages. Current mode control provides better response to input and output voltage variations because the current changes are sensed directly.

Current mode control provides inherent current limiting on a cycle by cycle basis. Current limiting improves system reliability in response to current transients.

Voltage Mode Disadvantages

- **Control of Flux Imbalance is difficult.**
- **Fast response to load changes is difficult.**
- **Slow response to input voltage changes.**

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Voltage mode control does not provide cycle by cycle control of current thru the transistors, this lack makes transformer flux balancing more difficult (often requiring added components).

The output voltage is measured on the output capacitor which makes quick detection of input voltage or output load changes difficult.

The two pole filter roll off in the feedback path further slows the system response to changes.

**Current Mode
Disadvantages**

- **Control stability is more difficult with dutycycles > 50%. Requires "slope compensation" to prevent "Sub-cycle oscillations."**
- **Wide input voltage variation is difficult to support.**
- **Low current loads difficult to control.**

Current mode control requires two feedback paths, increasing the system complexity and cost.

Duty cycles greater than 50% have problems with sub-cycle oscillations. To stop these oscillations requires the addition of "Slope compensation". Slope compensation decreases the peak current limit as the duty cycle increases. The reduction in peak currents is designed to maintain the same average currents with increasing duty cycles.

The accurate sensing of current is difficult to achieve with high accuracy. Typically, low ohmage resistors are inserted in the current path and the voltage drop across the resistor is an indication of the current. To minimize heat dissipation and voltage drops, the current sensing resistors are typically in the tens of milliohms range. The resultant voltage drops are in the millivolt range. Amplifying small signals in the presence of huge switching currents is a daunting task.

Wide input voltage range creates design issues because large variations in pwm duty cycle ratios are required, and exceeding 50% duty cycle introduces issues with slope compensation.

Output current loads that vary over large ranges are also difficult for current mode control to handle because the light load results in very small current measurement signals. The current measurement signals become buried in the noise.

Classic Digital SMPS Control Algorithm

P.I.D.

The Proportional error, the Integral error, and the Derivative error of the actual output versus the desired output voltage are summed to control the PWM dutycycle.

PID technique may be used in "Voltage Mode" and "Current Mode" control loops.

The PID (Proportional Integral Derivative) control algorithm was developed in 1942 by John G. Ziegler and Nathaniel B. Nichols. The PID loop is the dominant control method for motor control, industrial process control, and plant control.

PID controllers have been implemented in mechanical, pneumatic, and hydraulic systems, as well as in electronic form. While digital implementation of PID controllers have been used for decades to control motors, the digital implementation of PID control for SMPS applications is relatively new phenomenon.

The PID algorithm is an easy to understand (intuitive) algorithm.

The proportional term is the error between the desired output state and the actual output state (example: Desired output voltage – Actual output voltage). The proportional error provides the "Bulk" of the control loop command output.

The derivative term is the change in the proportional error over time. (example: New proportional error – previous proportional error). If the derivative error is non zero then it indicates that the system's conditions are changing rapidly. The derivative error acts to "dampen" transient conditions, providing the high frequency gain for the control loop.

The integral error is the slow accumulation of the proportional errors. In a system without an integral error term, the proportional error's affect on reaching the desired output state is less as the error is reduced. The integral error will drive the control system to the final end point.

Feed-Forward New Digital SMPS Control Techniques

- **P.I.D. technique is augmented with calculations including input voltage, components, and desired behavior.**

- **Classic PID requires an "Error" to create an output.**

- **Feed-Forward computes the expected pwm duty cycle based on input / output voltages, currents, and circuit topology.**

With the advent of modern DSPs and microprocessors, the PID algorithm is being "improved". The classic PID control method requires that an error be generated to create an output command to reach the desired system state.

With a computer, knowledge of the application system can be used to add more terms to the PID equation so the control loop does not have to be purely "Reactive" to an output state. Given the input voltage, system component values, and the desired output voltage, an ideal control loop command output can be calculated. This calculated ideal command is called the "Feed-Forward" term. The feed-forward term is added to the standard PID error terms. Other system aspects, such as anticipated load current changes, may also be added to the feed-forward calculations. For example: If a processor is in sleep mode, and it is about to enter active operation, it can provide a signal to the power supply to begin increasing the current supply.

Feed-forward terms can anticipate system changes before they are reflected in the output state of the power supply.

Feed-forward terms are inherently stable and "Pro-Active".

Benefits of Digital SMPS Control Techniques

- **Feed-Forward techniques are inherently stable, providing improved response to input changes.**

- **Classical definitions of Voltage Mode or Current Mode are blurred and now almost irrelevant.**

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Classic control theory has always been reactionary. They always look at where they were.   Imagine driving your car by only looking through the rear-view mirror !

Feed-forward terms combined with PID control loops are proactive. They are looking forward to the future. That is why most of us drive looking through the front windshield !

Most modern PID control systems incorporate multiple control loops that regulate and control system behaviors at different levels of the system hierarchy.

For example: Modern PID control loops can monitor and control both inductor current and voltage outputs.

So is it Voltage or Current mode ? Maybe it no longer matters.

Advanced Digital SMPS Control Techniques

- **Classic Linear Control Methods are "Reactive".**

- **Advanced Digital Control Methods can be "Proactive". Combine ability to model system with knowledge of application.**

- **"Think outside the Box"**

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As more information can be integrated into the feed-forward terms, the output errors become smaller, and fewer unexpected transients will be encountered.

With modern DSPs, the circuit equations for an SMPS system can be directly solved yielding voltage and current values without directly measuring them. This capability can circumvent stability issues created by system component induced measurement delays that plague traditional control techniques.

Benefits of dsPIC® SMPS Digital Control

- **Infinite flexibility in Control system design.**

- **Create new Topologies not supported by analog SMPS controllers to fit your application.**

- **Change converter characteristics by changing Flash program instead of circuit components.**

With classic analog SMPS PWM controllers, the control mode and the circuit topology are defined by the circuitry in the analog controller device.

Manufacturers of these controllers developed devices to support SMPS topologies that had enough "sockets" to justify the development costs for each pwm controller device.

The development of new SMPS topologies and the required pwm controller became a "Chicken and the Egg" issue. New controllers are unlikely to be built until there is a market for them, but the market won't develop until there is a controller available.

The SMPS dsPIC devices enable you to develop new circuit topologies and control methods to meet your system requirements !

Revising the control behavior no longer requires circuit board or component changes, instead just update the control program in Flash !

Switching Methodology

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Switching Methodology describes the voltage and current conditions that are applied to the power transistor in a switch mode converter at the time the transistor switches between conducting and non conducting states.

Switching Methodology

- **Hard-switching:** Classic SMPS switching method where the voltage and current are in phase. Large switching losses.

- **Soft-switching:** Complex circuit and control method insures either current or voltage is zero during switching. Near zero switching losses.

Most existing switch mode power supplies currently use "Hard-switching". Hard switching has the transistor switch on and off without regard to the phase of the currents and voltages applied to the transistor.

Historically, SMPS systems were considered so efficient relative to the older linear power supplies, that nobody complained about switching losses. Now as the switching frequency of SMPS systems moves from 20 KHz to 500 KHz, the issue of switching losses is becoming more urgent.

In hard switching converters, the voltages and currents are in-phase, so switching power dissipation is directly proportional to switching frequency and switching time. Switching times are now probably as small as practically feasible.

To further reduce switching losses, SMPS topologies and control schemes are being developed to shift the phase of the transistor voltage relative to the transistor current during the switching process.

If either the voltage or current is zero during the switching process, then the switching power dissipation is zero.

Hard Switching

- **Fixed Frequency**
- **Fewer components**
- **Simpler Control**

Hard switching is still the most common switching method. Hard switching converters are simpler, lower cost, and usually have a fixed switching frequency.

Fixed switching frequency makes the design of the magnetic components easier to optimize, and it simplifies control system design.

Fixed frequency switching may be required in larger systems so that the generated EMI falls into known frequencies, to avoid interference with other system circuitry.

Soft Switching Topologies

- **Resonant Mode** (variable frequency)
  - **SRC – Series Resonant**
  - **PRC – Parallel Resonant**
- **Quasi-Resonant Mode** (variable frequency)
  - **ZVS – Zero Voltage Switching**
  - **ZCS – Zero Current Switching**
- **Zero Transition** (Fixed Frequency)
  - **ZVT – Zero Voltage Transition**
  - **ZCT – Zero Current Transition**

Resonant mode power conversion uses tuned LC tank circuit(s) to transfer power from the input to the output. The power flow is controlled not by varying the duty cycle of the pwm, but by varying the frequency. Maximum power transfer occurs when the switching frequency matches the resonant frequency of the LC circuit. Minimum power transfer occurs as the switching frequency moves away from the resonant frequency. Resonant mode converters convert DC to high frequency sinusoidal AC and then back to DC. Resonant mode converters suffer from large circulating currents in the LC network.

Quasi-Resonant mode conversion attempts to simplify the complexity of resonant mode, the tuned LC circuits are used for "commutation" of the voltage and currents at the transistors rather than actually participating in the transfer of power. Quasi-Resonant mode is a variable frequency switching technique.

Zero Voltage Transition and Zero Current Transition uses shunt resonant circuits across the transistors to phase shift the current or voltage just during the transistor switching periods. ZVT and ZCT use a fixed pwm frequency to simplify system design.

ZVT and ZCT methods attempt to combine the best features of Hard and Soft switching techniques.

dsPIC® SMPS

Control Loop
Stability

Introduction to SMPS Control Techniques

The following slides will discuss issues that affect power supply control stability.

Basic Control System with Feedback
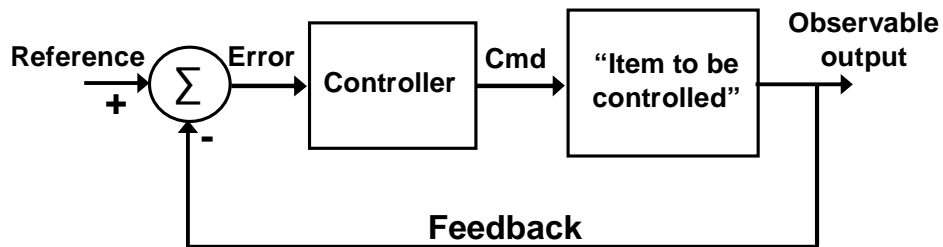
This slide shows a block diagram of a basic control system with feedback. The feedback provides information to the controller on the state of the "Item to be controlled" needed to correct any observed "misbehavior".

This control diagram is called a "Control Loop" because the feedback path creates a loop from the controller, to the "item to be controlled", and then back to the controller.

This control system features "Negative Feedback", the observable output signal is subtracted from the reference signal (desired behavior) to create an "Error" signal.

The error signal is the input to controller. The controller processes the error signal to create a command signal. The command signal provides the "force" needed to "push" the "Item to be controlled" to the desired state.

This simple control loop representation does not represent real world conditions.
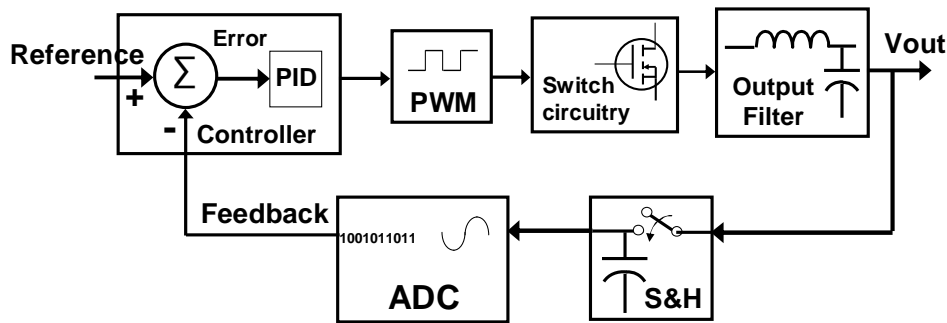
This slide shows a typical SMPS control system. The most important fact is that there are delays associated with each block in this diagram. The sample and hold circuit is typically sampling every 2 to 10 microseconds.

The ADC requires about 500 nanseconds to convert the analog feedback signal to a digital value.

The PID controller is a program running on a microprocessor (DSP) with a computation delay of about 1 to 2 microseconds.

The controller output is converted to a PWM signal which drives the switching circuitry. The pwm generator can introduce significant delays if it can not immediately update its output when given a new duty cycle.

The transistor drivers and the associated transistors also introduce delays from 50 nanseconds to about 1 microsecond depending on devices used and circuit design.

A very large source of delays is the output filter which is typically implemented with an inductor and capacitor (LC) circuit.

Control System with Delays
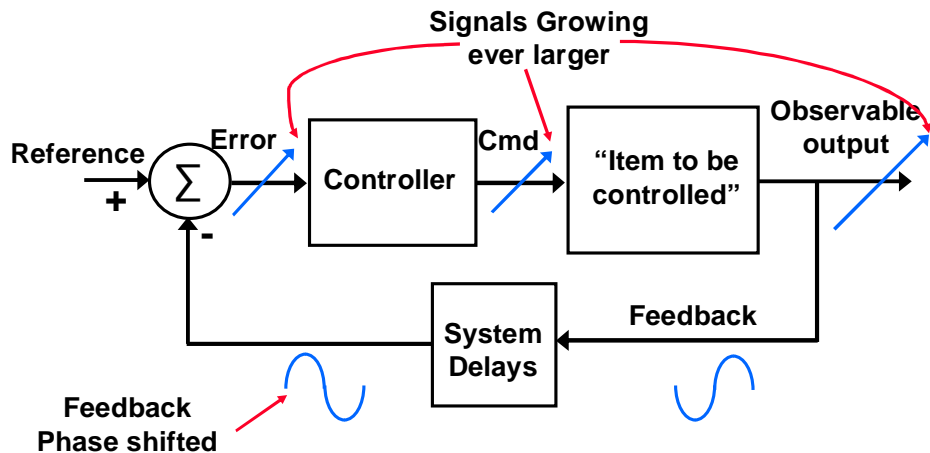
This slide shows a block diagram of a basic control system with delays. The delays are shown lumped together in a single block for clarity. Control systems assume "Negative Feedback". The error signal is supposed to be the reference signal MINUS the feedback signal.

If there are enough delays in a system where the feedback signal is phased shifted (delayed) by 180 degrees, then the subtraction operation becomes an addition (Reference + Feedback). In this situation, the error term grows in an uncontrolled fashion.

In a real system, there are limits to signals and system capabilities and the system will "Saturate".

As the system saturates, the outputs will become stable because they can not go any further. Eventually, the delayed feedback signal will "catch up" to the saturated system state.

Now the error term (Reference – Feedback) will become a large negative value, and the system will move rapidly to the negative saturated limit. This process will repeat with the system swinging between the positive and negative limits. The system is oscillating.

The system will oscillate at a frequency determined by the system's delays.

Minimum Control System Stability Requirements

- **At the frequency where the system delays introduce a 180 degree phase shift, the system gain MUST be less than 1.**

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To be stable, a control system must insure that for all possible frequencies of signals in a system where the phase shift of the feedback is greater than or equal to 180 degrees relative to the controller output, the gain around the control loop must be less than one.

Typical Control System Stability Requirements

- **Phase Margin ≥ 45°**
- **Gain Margin ≥ 2**

Phase margin is the amount of additional phase lag that a system can add before the critical 180 degree phase lag is reached. Systems with less than 45 degrees of phase margin experience "ringing" or overshoot in response to transient conditions.

The gain margin is the factor by which the closed loop system gain is less than 1.0 at the critical 180 degree phase lag frequency. A gain margin of 2 means that the loop gain is 0.5 at 180 degrees.

In large transient situations, system non-linearities can reduce the system's loop gain and cause instability problems. Having additional phase and gain margin helps prevent situations where a system is conditionally stable.

Digital Control Loops and Stability

- **Digital Sampling rate must be greater than Nyquist rate. 6 – 10x**

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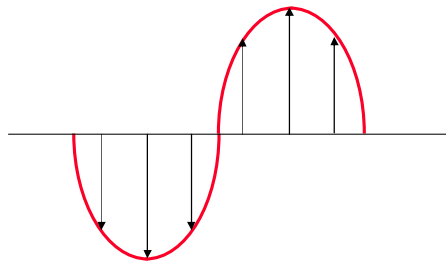
While Nyquist requires a 2X sampling rate to reconstruct a signal, digital control loops need to sample at a 6x to 10x rate.

The reason is pretty obvious: With only a 2x sampling rate, the phase lag is 180 degrees. With 2x sampling rate, we have already used up our "budget" of 180 degrees for phase lag without considering any other delays in the system.

A system with 8x sampling introduces 45 degrees of phase lag just from the sampling process. This is a better sampling rate

To maximize phase margin many digital control systems oversample the analog signals by 10x or more.
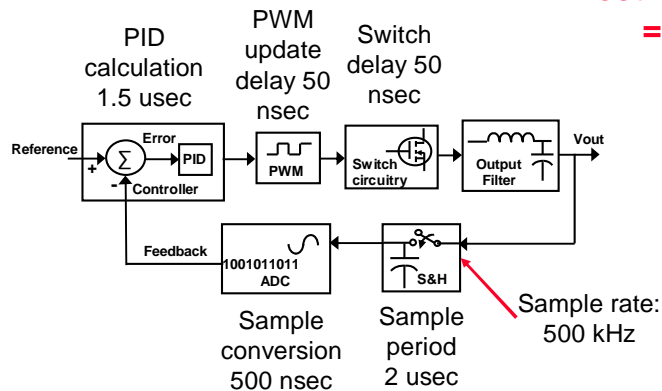
All of the delays associated with the conversion of the analog feedback signal, to the digital calculations by the processor, and the output delays of the pwm to the power transistors are added to the sampling rate delays. The effective sampling frequency is the inverse of the controller and sampling delays.

The controller bandwidth is the effective controller sample rate divided by the oversampling ratio. In this slide, we assume we can assume 6x over sampling.

The estimated controller bandwidth is 40 KHz.

Adding Feed-Forward terms to the control algorithm can increase the performance of the controller beyond the capabilities of a traditional PID controller with a 40 KHz bandwidth.

Output Filter Corner Frequency Requirements

Filter Corner Frequency should be less than or equal to one third of Control Bandwidth.
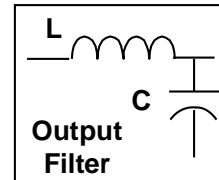
Output Filter

Example:

Bandwidth = 40 kHz

C = 19.5 uF

L = 12.12 uh

Filter Corner Frequency:

$$FCF = 1/(2\pi \sqrt{LC}) = 10.35 \text{ kHz}$$

10.35 KHz < (40 kHz / 3)

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The SMPS output filter's corner frequency should be significantly less than the controller's bandwidth to insure that the output filter's resonance behavior lies within the controller's bandwidth.

A reasonable guideline is that the output filter's resonant frequency should be two to three times lower than the controller's bandwidth.

Controller and PWM Frequency Requirements

The controller's bandwidth should be less than or equal to one fourth of PWM frequency.

Example:

Bandwidth = 40 kHz
PWM Frequency = 400 kHz
40 kHz << 400 kHz

To prevent the PWM ripple from affecting the controller, the PWM frequency should be at least 4 or 5 times higher than the controller's bandwidth.

In this example, the ratio is ten to one.

Key Support Documents

Device Selection Reference	Document #
General Purpose and Sensor Family Data Sheet	DS70083
Motor Control and Power Conv. Data Sheet	DS70082
dsPIC30F Family Overview	DS70043

Base Design Reference	Document #
dsPIC30F Family Reference Manual	DS70046
dsPIC30F Programmer's Reference Manual	DS70030
MPLAB® C30 C Compiler User's Guide	DS51284
MPLAB ASM30, LINK30 & Utilities User	DS51317
dsPIC® Language Tools Libraries	DS51456

For more information, here are references to some important documents that contain a lot of information about the dsPIC30F family of devices.

The Family Reference Manual contains detailed information about the architecture and peripherals, whereas the Programmer's Reference Manual contains a thorough description of the instruction set.

Key Support Documents

Microchip Web Sites: **www.microchip.com/smps**

www.microchip.com/16-bit

For device data sheets, Family Reference Manuals, and other related documents please visit the following Microchip websites.

Thank You

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Thank you for attending this Webinar