4

Analyzing the Fundamental SMPS Model

Chapter 3 developed the basic switch mode power converter circuit-averaged models that could easily be adapted for use in a switch mode power supply (SMPS) computer simulation circuit analysis. These models provide the capability of analyzing the large signal (DC and transient) and small signal (AC) properties of a particular power converter. At the next higher level, these converter models can be enfolded into a total SMPS model and an analysis of the total power supply performance can make. In this chapter, only the most basic or first-order aspects of the SMPS will be considered by analyzing some of its fundamental DC and AC characteristics. Chapter 6 will continue with the general theme of this chapter and provide the more advanced or comprehensive detailed analysis methods necessary when a higher level of complexity is involved.

4.1 Buck Converter SMPS Analysis (Voltage Mode)

Consider the switching regulator (SMPS) depicted in Figure 4.1. This is a very elementary voltage regulator with a single output voltage and no transformer isolation separating the input from the output. Despite its simplicity, many fundamental analysis concepts with a broad range of applications can be learned by conducting a thorough first-order analysis on such a regulator. A first-order computer model will be set up for the voltage mode switching regulator and some of its most basic properties will be observed as it is analyzed.

4.1.1 Voltage Mode Converter Model Setup

A power converter model of the type shown in Figure 3.6 is determined to be of the type required for this voltage mode application. First, a feedback control circuit consisting of the error amplifier, voltage reference, and pulse width modulation block is added. The pulse width modulator is a circuit-averaged block appearing simply as a linear voltage-to-duty ratio, d, converter. This d is the control input to the power converter. For the purposes of this exercise, the control circuit blocks are all simplified functional blocks

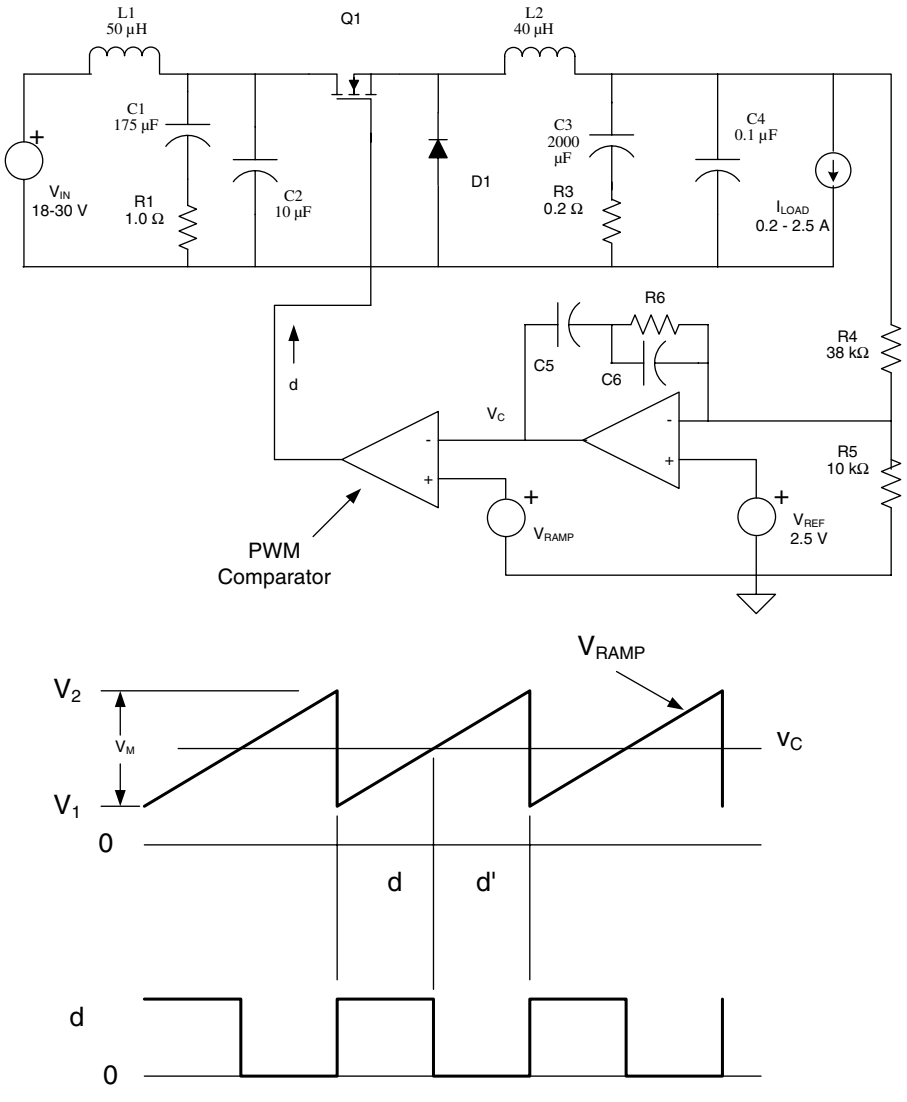
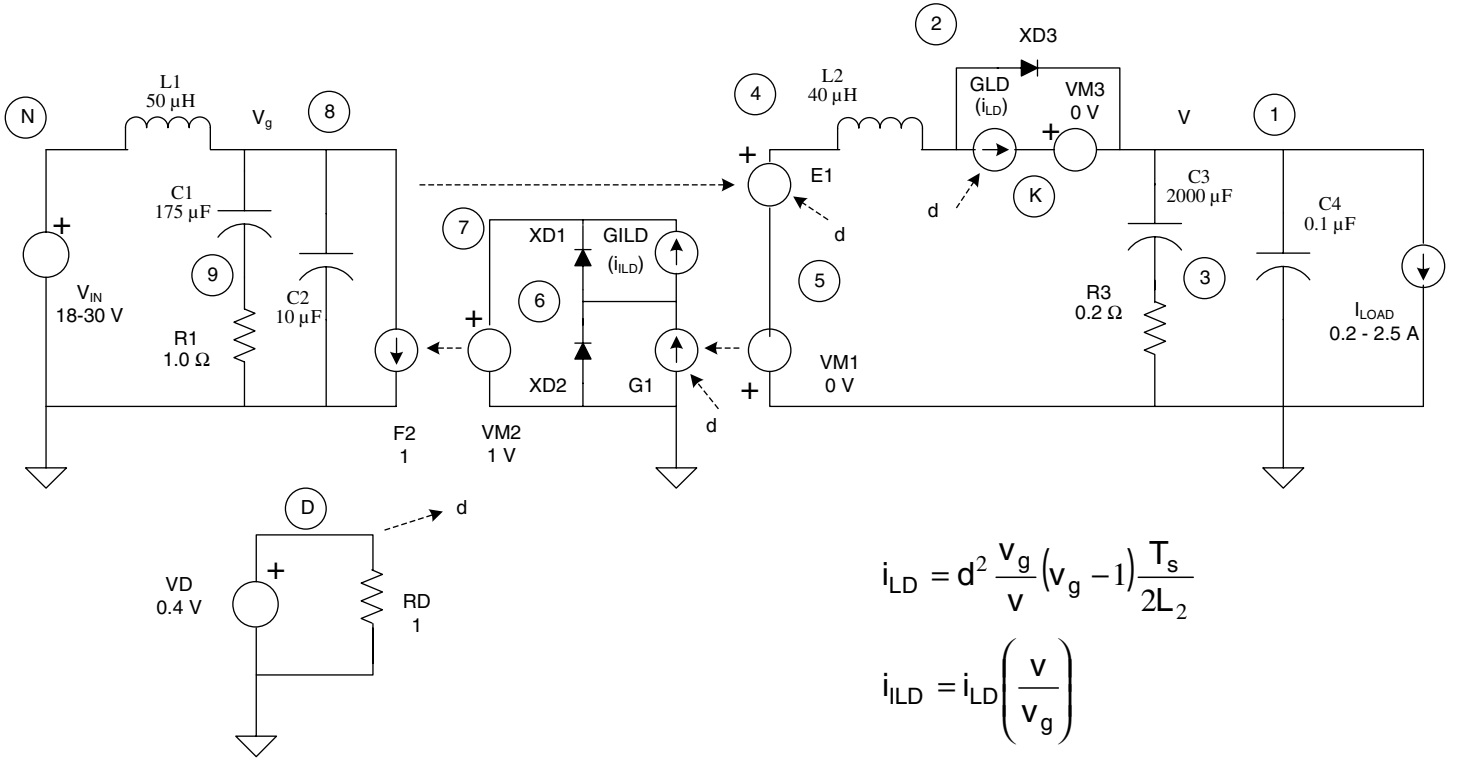


FIGURE 4.1
Simple buck voltage mode switching regulator (conceptual).

with near ideal characteristics. The converter model to be analyzed is of the type shown in Figure 4.2.

4.1.2 Open Loop Analysis (Continuous and Discontinuous Modes)

As a point of departure, the power supply will be analyzed initially by looking at the converter open loop characteristics. Then the feedback control circuit



$$i_{LD} = d^2 \frac{v_g}{v}\left(v_g - 1\right)\frac{T_s}{2L_2}$$

$$i_{ILD} = i_{LD}\left(\frac{v}{v_g}\right)$$

FIGURE 4.2
Buck converter model example.

will be added and the final performance characteristics noted. A PSPICE netlist, labeled Netlist 4.1, is used for these open loop analysis simulations.

NETLIST 4.1

```
BUCK CONVERTER OPEN LOOP ANALYSIS
*
************************************************************
*
** SOURCE-LOAD CONFIGURATION FOR
** FIGURE 4.3
** BUCK CONVERTER DC FORWARD TRANSFER FUNCTION WITH D = 0.4
*
VIN N 0 DC 30
ILOAD 1 0 DC 2
.DC ILOAD 0 2.5 .01 VIN 20 30 5
VD D 0 DC .4 AC 0
*
************************************************************
*
** SOURCE-LOAD CONFIGURATION FOR
** FIGURE 4.4 AND 4.5
** BUCK CONVERTER AC FORWARD TRANSFER FUNCTION
*
*VIN N 0 DC 30 AC 1
*ILOAD 1 0 DC 2
*.STEP ILOAD LIST .2 .7 1.2 2.5
*VD D 0 DC .4 AC 0
*.AC DEC 20 1 100K
*
************************************************************
*
** SOURCE-LOAD CONFIGURATION FOR
** FIGURE 4.6
** BUCK CONVERTER OUTPUT IMPEDANCE (VOLTAGE AND CURRENT MODE)
*
*VIN N 0 DC 30
*ILOAD 1 0 DC 2
*.STEP ILOAD LIST .2 .7 1.2 2.5
*VD D 0 DC .4 AC 0
*IAC 1 0 AC 1
*.AC DEC 20 1 100K
*
************************************************************
*
** SOURCE-LOAD CONFIGURATION FOR
** FIGURE 4.7
** BUCK CONVERTER DC "CONTROL "D" TO OUTPUT" TRANSFER FUNCTION
*
*VIN N 0 DC 30 AC 0
*ILOAD 1 0 DC 2
*.DC ILOAD 0 2.5 .01 VD 0 1 .1
*VD D 0 DC .4 AC 1
*
```

```
************************************************************
*
** SOURCE-LOAD CONFIGURATION FOR
** FIGURE 4.8
** BUCK CONVERTER AC "D TO OUTPUT" TRANSFER FUNCTION (VOLTAGE MODE)
*
*VIN N 0 DC 30 AC 0
*ILOAD 1 0 DC 2
*.STEP ILOAD LIST .2 .7 1.2 2.5
*VD D 0 DC .4 AC 1
*.AC DEC 20 1 100K
*
************************************************************
*
** SOURCE-LOAD CONFIGURATION FOR
** FIGURE 4.18
** BUCK CONVERTER AC FORWARD TRANSFER FUNCTION
** WITH FEEDFORWARD ADDITION (VOLTAGE MODE)
*
*VIN N 0 DC 30 AC 1
*ILOAD 1 0 DC 2
*.STEP ILOAD LIST .2 .7 1.2 2.5
*ED D 0 VALUE = {12/V(8)}
*.AC DEC 20 1 100K
*
************************************************************
*
** BUCK CONVERTER, VOLTAGE MODE, NETLIST
*
RD D 0 1
C4 1 0 .1U
C3 1 3 2000U
R3 3 0 .2
GLD 2 K VALUE = {V(D)**2*(V(8)/V(1))*(V(8)-V(1))*.125}
VM3 K 1
XD3 2 1 DIDEAL
L2 4 2 40U
E1 4 5 VALUE = {V(8)*V(D)}
VM1 0 5
GILD 6 7 VALUE = {I(VM3)*V(1)/V(8)}
G1 0 6 VALUE = {I(VM1)*V(D)}
XD1 6 7 DIDEAL
XD2 0 6 DIDEAL
VM2 7 0 DC 1
F2 8 0 VM2 1
C2 8 0 10U
C1 8 9 175U
R1 9 0 1
L1 N 8 50U
*
.SUBCKT DIDEAL 1 2
EID 3 1 TABLE {V(3,2)} = (-1,1U) (1U,1U) (1,1)
DIO 3 2 D
.MODEL D D IS=1E-12
.ENDS DIDEAL
```

```
*
.PROBE
.END
```

4.1.2.1 Forward Transfer Function

The converter is set up with an input voltage of 30 Vdc and an output voltage of 12 Vdc. This will necessitate a steady state duty ratio, D, of

$$D = \frac{12v}{30v} = 0.4 \tag{4.1}$$

for the no feedback forward transfer analysis. With a fixed frequency of 100 kHz (T_S = 10 μS) and a value of 40 μH for the filter inductor, L2, the critical load current for continuous conduction mode operation is:

$$I_{CRIT} = \frac{VT_S(1-D)}{2L_2} = \frac{12V \times 10\mu S \times (1-0.4)}{2 \times 40\mu S} = 0.9A \tag{4.2}$$

The forward transfer function with continuous conduction mode currents of 1.2 and 2.5 amps (greater than the critical current of 0.9 amps) and then with discontinuous mode currents of 0.2 and 0.7 amps (less than the critical current of 0.9 amps) will be considered. The lowest value of 0.2 amps represents a deep discontinuous conduction mode. Figure 4.2 shows the converter model to be analyzed.

As a sidelight, Figure 4.3 shows how the output voltage of this constant frequency, fixed duty ratio, buck converter varies with a sweep of load current from 0 to 2.5 amps and input voltages of 20, 25, and 30 V. It is interesting to note that a fixed critical load resistance, R_{CRIT} (equal to 13.33 Ω in this case),

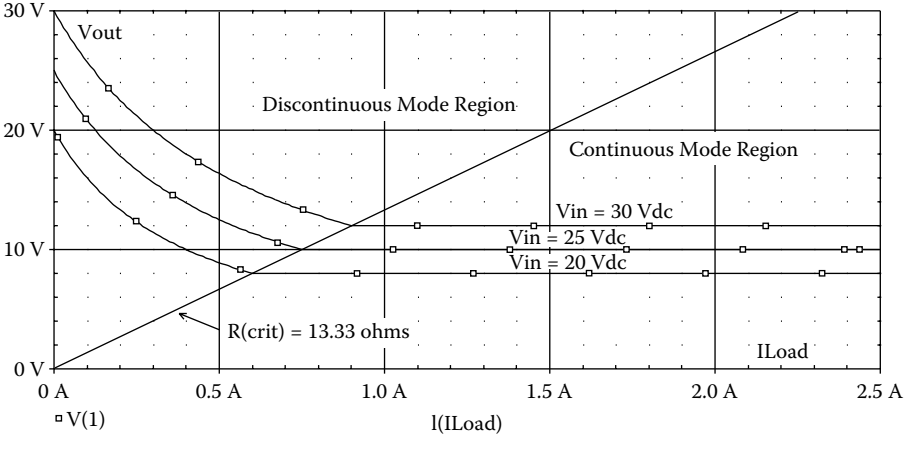


FIGURE 4.3
Buck converter DC forward transfer function with D = 0.4.

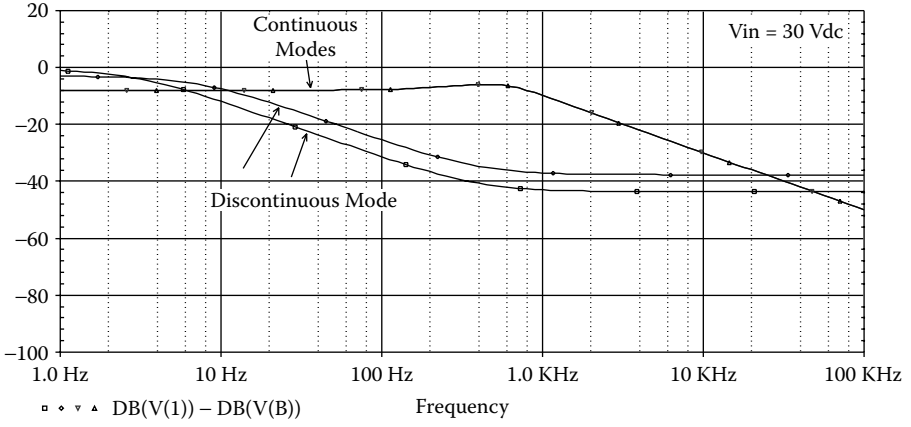


FIGURE 4.4
Buck converter AC forward transfer function.

exists as noted by the straight line intersection of all the critical conduction points separating continuous and discontinuous conduction modes.

Now consider the AC forward transfer characteristics. A constant input voltage of 30 Vdc, $D = 0.4$, and the same two pair of continuous and discontinuous mode DC load current are used here also. For this example, the corner frequencies of the input and output filter are purposefully separated from each other in order to show their possible individual effects. Figure 4.4 shows the transfer function for just the converter portion (node 8 to node 1 in the simulation), and Figure 4.5 shows the overall transfer function, including the input filter. Notice that both continuous mode current transfer

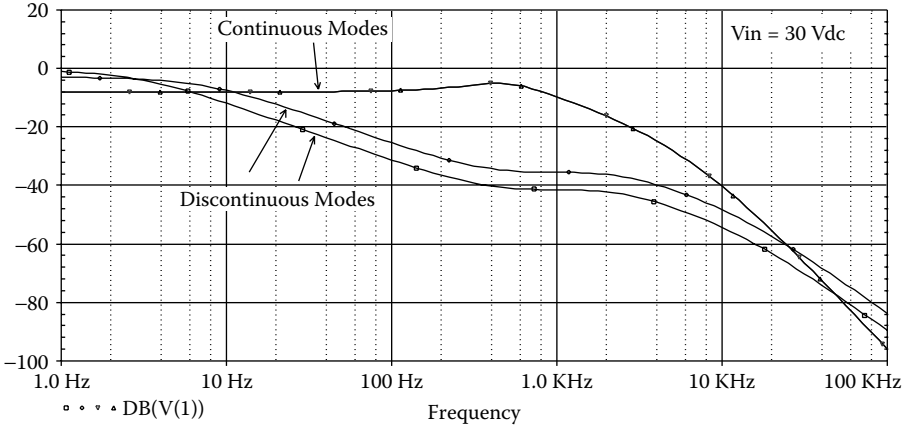


FIGURE 4.5
Buck converter AC forward transfer function with input filter added.

functions are the same and are independent of load current, but the discontinuous mode transfer function varies with load. The smaller the load is, the lower the initial low frequency break point is.

Another interesting observation for the discontinuous mode case is that the converter attenuation starts to flatten out after the output filter capacitor, C3, breaks with it series resistance, R3, at a frequency of 400 Hz. For the continuous mode case with the output filter (L2, C3) near critical damping, an attenuation slope of only 20 dB/Dec occurs after its corner frequency of approximately 600 Hz. Figure 4.5 shows the transfer functions with the addition of the input filter section. For the continuous mode currents, the additional attenuation and steeper slope occur after the input filter corner frequency (approximately 5 kHz). The two discontinuous mode current cases also show the additional attenuation provided by the input filter addition.

4.1.2.2 Output Impedance (Voltage Mode)

Now look at the AC output impedance of the converter for the same conditions as those set up in the previous paragraph. (The input filter section remains in the circuit unless otherwise noted.) Figure 4.6 shows the AC output impedance plots. (0 dB is equivalent to 1 Ω.) The discontinuous mode output impedance is relatively high and also a function of the load current prior to breaking with the output filter capacitor, C3, at frequencies near 10 Hz. At the low frequencies, the output impedance for the continuous mode is essentially the inductive reactance of inductor L2 in series with the reactance of L2 reflected by the duty ratio squared (D^2).

4.1.2.3 Control to Output (Voltage Mode)

Examine the DC transfer functions for the control, D, to output voltage, v. The input voltage will be maintained constant at 30.0 Vdc; in this case, the

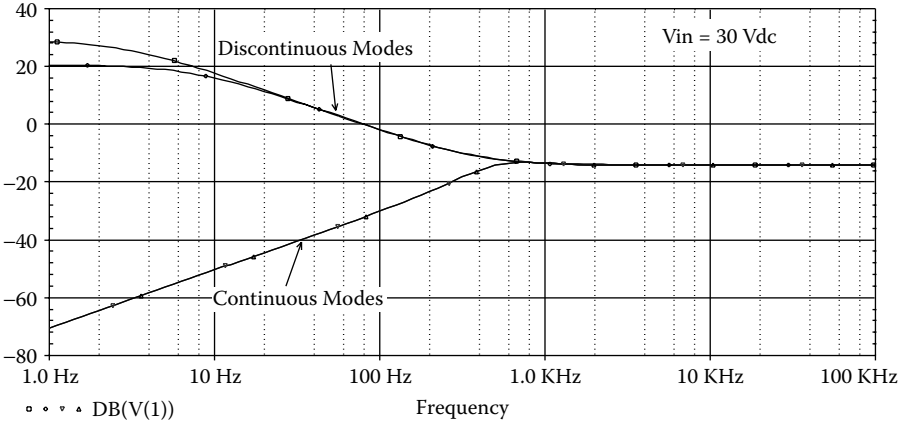


FIGURE 4.6
Buck converter output impedance (voltage mode).

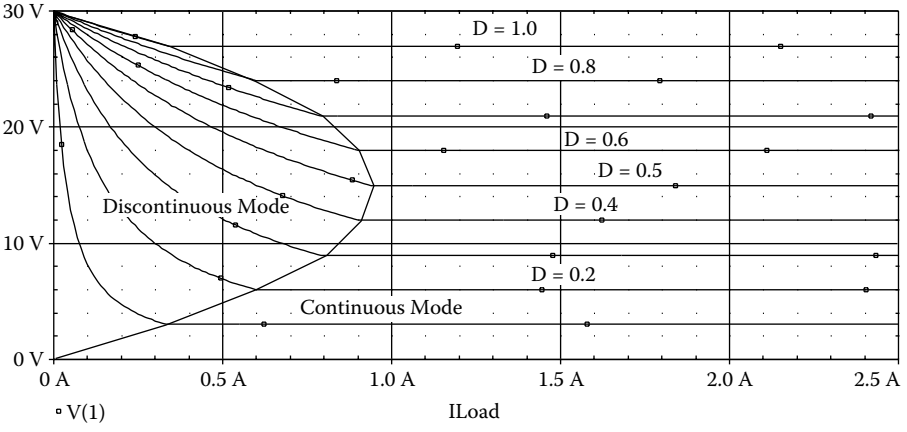


FIGURE 4.7
Buck converter DC "control to output" transfer function with *Vin* = 30 Vdc (voltage mode).

duty ratio, *D*, will be varied over its range of 0 to 1. Figure 4.7 shows the DC transfer functions for values of *D* stepped from 0 to 1 in increments of 0.1. Load currents were swept from 0 to 2.5 amps as was the case for the forward transfer function analysis. Note that the output voltage is independent of load current for continuous mode conduction and varying with load current for discontinuous modes. Of course, the duty ratio must vary considerably with load current in the discontinuous mode to regulate the output voltage, but theoretically may remain fixed for continuous mode currents. It is interesting to note the parabolic loci generated by connecting the critical current points for each of the stepped values of *D*. Also, note the maximum critical current occurring at the duty ratio of $D = 0.5$.

Now consider the AC control to output transfer functions. The same two pairs of continuous and discontinuous mode DC load currents will be used as were used for the forward voltage transfer analysis when analyzing the AC forward transfer function (continuous conduction mode currents of 1.2 and 2.5 amps and discontinuous mode currents of 0.2 and 0.7 amps). Also, as was the case for the forward transfer function, the input will be set to a constant 30 Vdc and the control, *D*, to a DC biased value of 0.4 while this is modulated with the small signal AC stimulus.

Figure 4.8 shows the results. Note that the discontinuous mode gains rolling off at lower corner frequencies are very much proportional to load current. The continuous mode gains roll off at higher frequencies and are seen to be fairly independent of load current. A very small, almost imperceptible dip in gain is noted around 2 kHz. This secondary effect is produced by the finite output impedance of the input filter. When analyzed with the input filter removed (not shown here), this small dip disappears. On the other hand, with an improperly designed input filter, this gain dip may increase and cause such negative effects as reduced loop gain; reduced

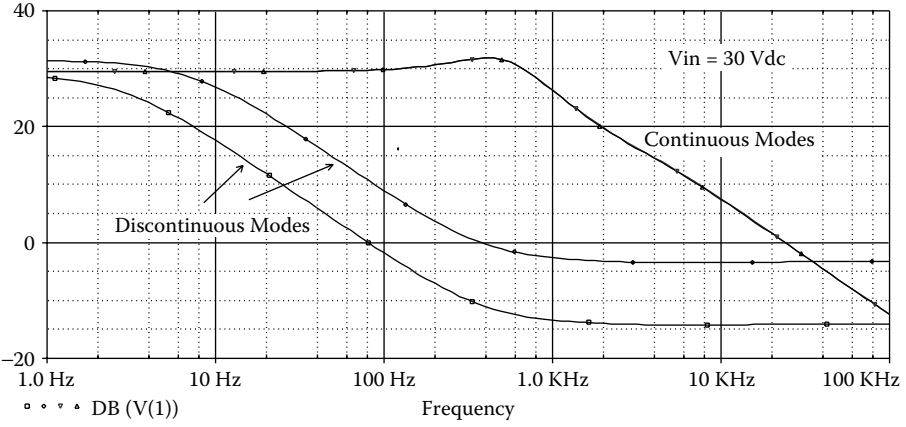


FIGURE 4.8
Buck converter AC "*d* to output" transfer function (voltage mode).

forward transfer attenuation; and higher output impedance; in severe cases, an input filter oscillating instability may occur.[2,13]

4.1.3 SMPS Closed Loop Analysis (Continuous and Discontinuous Modes)

Now add the feedback control circuit, which regulates the output voltage to 12 Vdc, and consider the SMPS characteristics and performance with this addition. Figure 4.9a shows the basic configuration. (A PSPICE netlist, labeled Netlist 4.2, is used for these voltage mode closed loop analysis simulations.) Using the same buck converter, an error amplifier has been added, along with a 2.5-V reference. Then the PWM gain block is inserted and combined with the AC-only loop opening, ultralow-pass filter circuit. It comprises LOL, COL, and VAC. This allows one to maintain the normal closed loop DC operating points while examining the small signal AC open loop characteristics at these operating points. This technique will be used repeatedly in many of the future analyses. VAC is the signal injection stimulus necessary for any AC gain measurement or analysis. The PWM gain is:

$$d = \frac{V(13)}{V_M} \tag{4.3}$$

where V_M is the PWM ramp amplitude (V_M = 1 V for these simulations). The input voltage and load currents are then varied over the same ranges as was done for the preceding open loop analysis. (Figure 4.9b shows the extremely simple op amp model used for illustration purposes.)

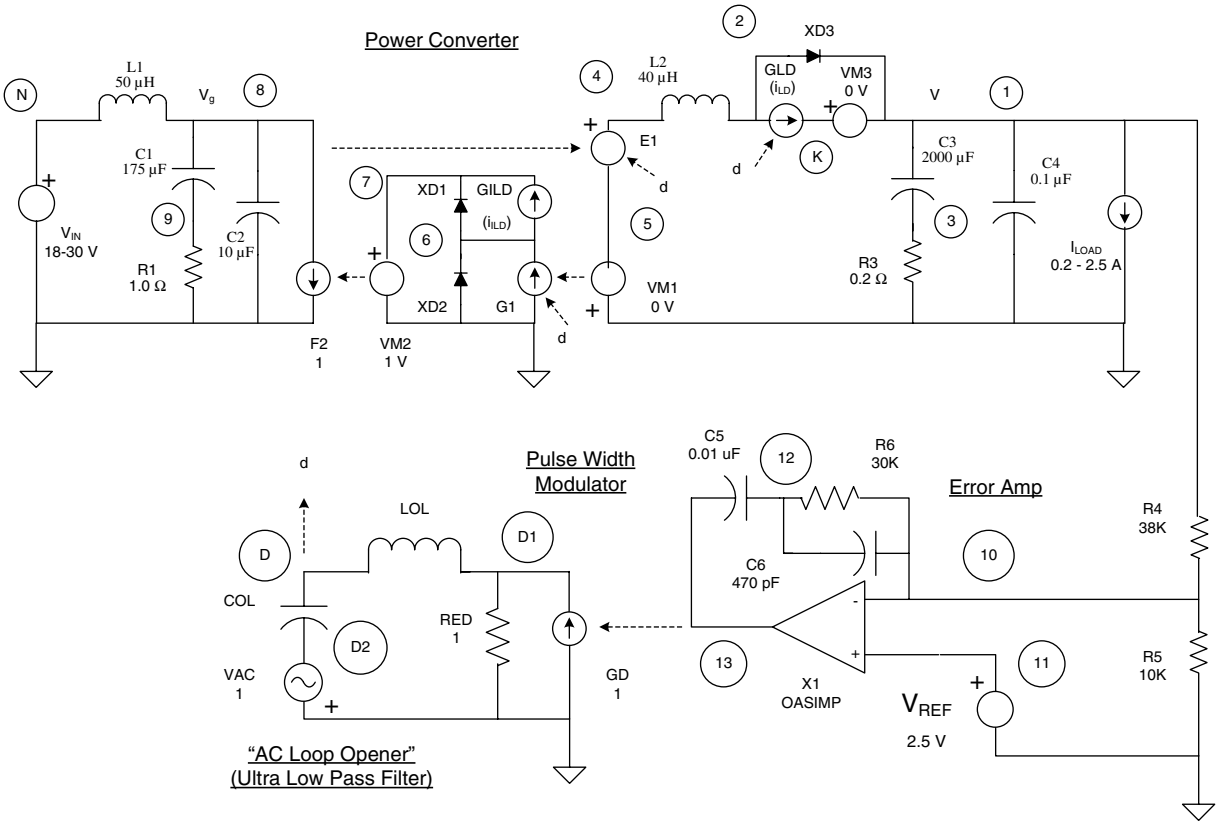


FIGURE 4.9a
Buck converter switching regulator (voltage mode).

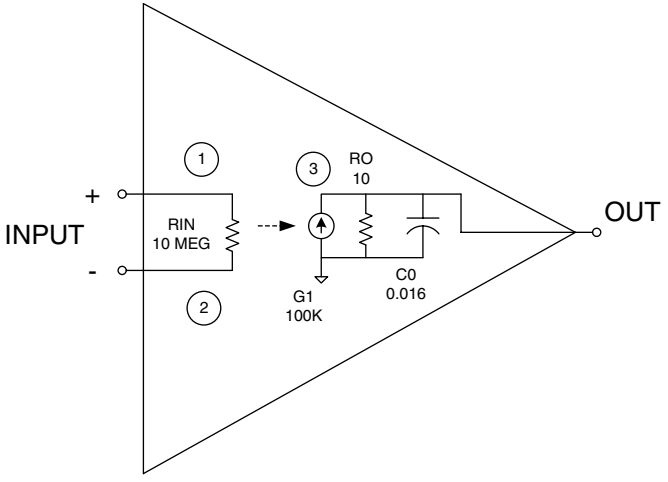


FIGURE 4.9b
Simple 1.0-MHz bandwidth op amp model.

NETLIST 4.2

```
BUCK CONVERTER SMPS, VOLTAGE MODE, CLOSED LOOP ANALYSIS
*
************************************************************
*
** SOURCE-LOAD CONFIGURATION FOR
** FIGURES 4.10 AND 4.11
** BUCK SMPS AC LOOP GAIN AND PHASE
** WITH LOAD CHANGE (VOLTAGE MODE)
*
VIN N 0 DC 30 AC 0
ILOAD 1 0 DC .2
.STEP ILOAD LIST .2 .7 1.2 2.5
LOL D1 D 1K
COL D D2 1K
VAC 0 D2 AC 1
.AC DEC 20 1 100K
*
************************************************************
*
** SOURCE-LOAD CONFIGURATION FOR
** FIGURES 4.12 AND 4.13
** BUCK SMPS AC LOOP GAIN AND PHASE
** WITH INPUT VOLTAGE CHANGE (VOLTAGE MODE)
*
*ILOAD 1 0 DC 2.5
*ILOAD 1 0 DC .2
*VIN N 0 DC 18
*.STEP VIN LIST 18 30
*LOL D1 D 1K
```

```
*COL D D2 1K
*VAC 0 D2 AC 1
*.AC DEC 20 1 100K
*
************************************************************
*
** SOURCE-LOAD CONFIGURATION FOR
** FIGURES 4.14 AND 4.15
** BUCK SMPS AC OUTPUT IMPEDANCE
** WITH INPUT VOLTAGE CHANGE (VOLTAGE MODE)
*
*ILOAD 1 0 DC 2.5
*ILOAD 1 0 DC .2
*VIN N 0 DC 18
*.STEP VIN LIST 18 30
*LOL D1 D 1P
*COL D D2 1P
*VAC 0 D2 AC 0
*IAC 1 0 AC 1
*.AC DEC 20 1 100K
*
************************************************************
*
** SOURCE-LOAD CONFIGURATION FOR
** FIGURES 4.16 AND 4.17
** BUCK SMPS AC FORWARD ATTENUATION
** WITH INPUT DC VOLTAGE CHANGE (VOLTAGE MODE)
*
*ILOAD 1 0 DC .2
*ILOAD 1 0 DC 2.5
*VIN N 0 DC 30 AC 1
*.STEP VIN LIST 18 30
*LOL D1 D 1P
*COL D D2 1P
*VAC 0 D2 AC 0
*.AC DEC 20 1 100K
*.NODESET V(1)=12 V(8)=30 V(13)=1
*
************************************************************
*
** SOURCE-LOAD CONFIGURATION FOR
** FIGURES 4.19 AND 4.20
** BUCK SMPS AC FORWARD ATTENUATION WITH FEEDFORWARD COMPENSATION
** WITH INPUT DC VOLTAGE CHANGE (VOLTAGE MODE)
*
*ILOAD 1 0 DC .2
*ILOAD 1 0 DC 2.5
*VIN N 0 DC 30 AC 1
*.STEP VIN LIST 18 30
*LOL D1 D 1P
*COL D D2 1P
*VAC 0 D2 AC 0
*.AC DEC 20 1 100K
*.NODESET V(1)=12 V(8)=30 V(13)=1
```

```
*.OPTIONS GMIN=1E-10
*
** NOTE: THE FOLLOWING GD REMAINS IN THE CIRCUIT FOR ALL OTHER ANALYSIS
** BUT MUST ALTERNATE WITH THE SECOND GD BELOW FOR THIS
** BUCK SMPS AC FEEDFORWARD ATTENUATION ANALYSIS ONLY
GD 0 D1 13 0 1
*GD 0 D1 VALUE = {LIMIT((12*V(13))/V(8),0,1)}
*
************************************************************
*
**VOLTAGE MODE SMPS NETLIST
*
RED D1 0 1
C4 1 0 .1U
C3 1 3 2000U
R3 3 0 .2
GLD 2 K VALUE = {V(D)**2*(V(8)/V(1))*(V(8)-V(1))*.125}
VM3 K 1
XD3 2 1 DIDEAL
L2 4 2 40U
E1 4 5 VALUE = {V(8)*V(D)}
VM1 0 5
GILD 6 7 VALUE = {I(VM3)*V(1)/V(8)}
G1 0 6 VALUE = {I(VM1)*V(D)}
XD1 6 7 DIDEAL
XD2 0 6 DIDEAL
VM2 7 0 DC 1
F2 8 0 VM2 1
C2 8 0 10U
C1 8 9 175U
R1 9 0 1
L1 N 8 50U
R4 1 10 38K
R5 10 0 10K
VREF 11 0 DC 2.5
X1 11 10 13 OASIMP
C5 13 12 .01U
R6 12 10 30K
C6 12 10 470P
*
.SUBCKT OASIMP 1 2 3
RIN 1 2 10MEG
G1 0 3 1 2 100K
RO 3 0 10
CO 3 0 .016
.ENDS OASIMP
*
.SUBCKT DIDEAL 1 2
VAS 1 3 DC -1U
D1 3 2 D
D2 3 4 D
D3 4 2 D1
FAS 4 2 VAS 1
.MODEL D D IS=1E-6
.MODEL D1 D
```

```
CC 1 2 .1P
.ENDS DIDEAL
*
.PROBE
.END
```

4.1.3.1 AC Loop Gain (Voltage Mode)

Figure 4.10 shows the AC loop gain and phase plots for the two continuous mode loads of 1.2 and 2.5 amps, and Figure 4.11 shows the AC loop gain and phase plots for the two discontinuous mode loads of 0.2 and 0.7 amps. The continuous mode gains in Figure 4.10 are independent of load current variations, as might be expected; however, the gains in the discontinuous mode cases of Figure 4.11 do vary with load current, as also might be expected. Note that the unity gain crossover frequency is reduced for the discontinuous mode cases and continues to decrease for further decreasing loads.

To ensure that the feedback control loop maintains AC stability, the phase shift must not approach or exceed a magnitude of –180° at the unity gain crossover frequency. The actual phase difference, or "phase margin," from –180° at the unity gain crossover frequency is conventionally considered the most important figure of merit for determining the degree of AC stability of a feedback control system. The accompanying figure of merit is the gain margin. This is the reduction in loop gain magnitude below unity (0 dB) corresponding to the –180° phase shift point. Typical numbers desired for the phase and gain margin are 45° and 10 dB. See Kuo[10] and D'Azzo and Houpis[11] for more fundamental information on feedback control stability.

Now consider the effects of input DC voltage variations on loop gain by stepping V_{in} from 18 to 30 Vdc with the load cases of 2.5 amps (continuous)

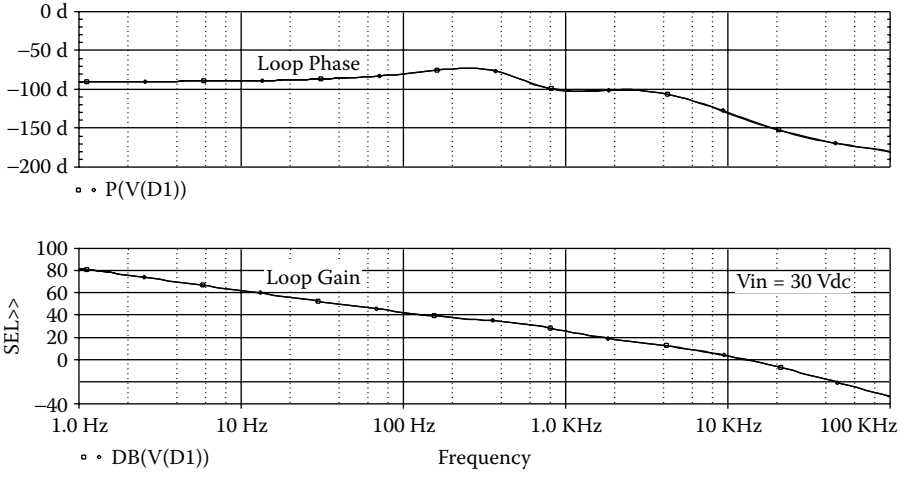


FIGURE 4.10
Buck SMPS continuous mode AC loop gain and phase with load change (voltage mode).

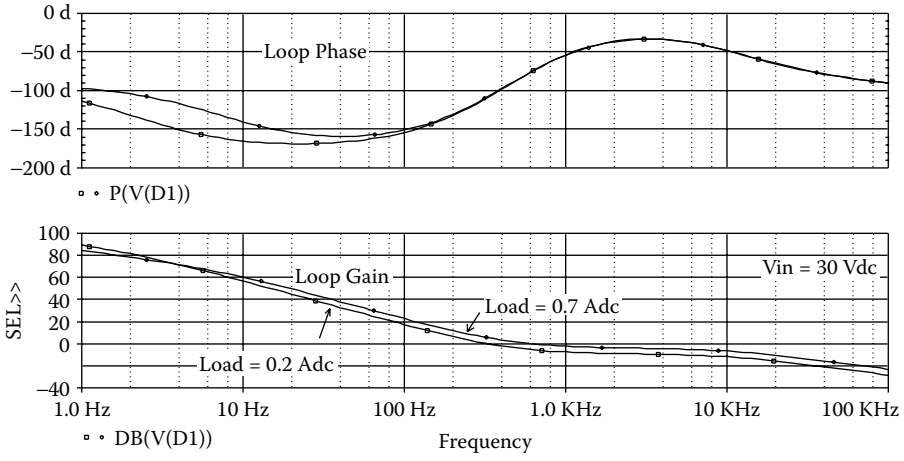


FIGURE 4.11
Buck SMPS discontinuous mode AC loop gain and phase with load change (voltage mode).

and 0.2 amps (discontinuous). Figure 4.12 and Figure 4.13 show the respective plots. Both plots indicate a shift in gain that is somewhat proportional to the input voltage change ratio.

4.1.3.2 SMPS Output Impedance (Voltage Mode)

Now look at the SMPS output impedance for extreme variations in line voltage and load currents that were considered in the preceding loop gain analyses. By examining the plots of Figure 4.14 and Figure 4.15, AC impedance

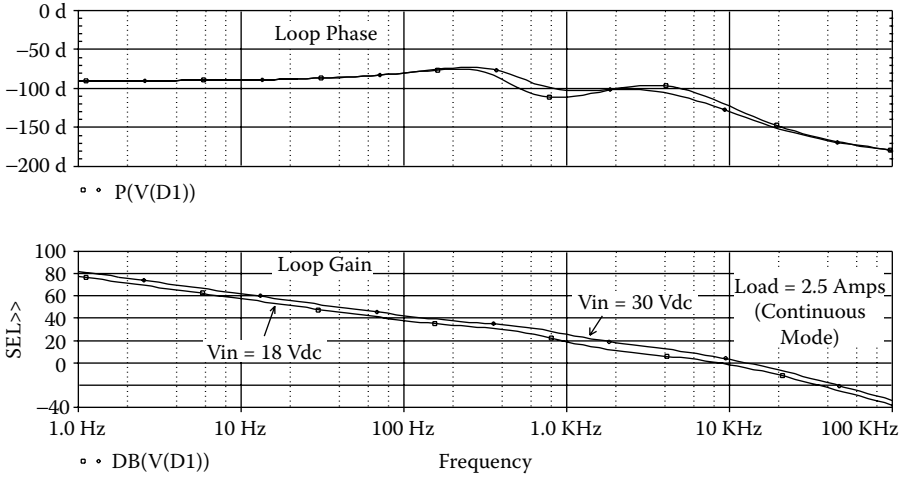


FIGURE 4.12
Buck SMPS continuous mode AC loop gain and phase with input voltage change (voltage mode).

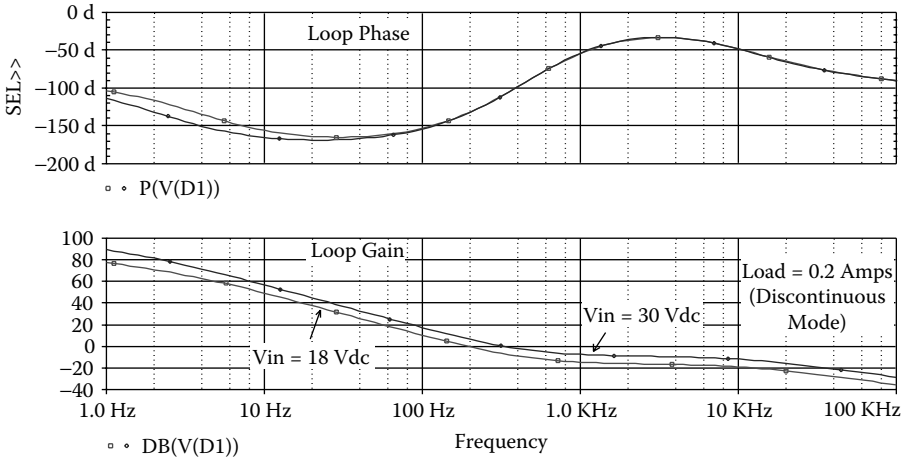


FIGURE 4.13
Buck SMPS discontinuous mode AC loop gain and phase with input voltage change (voltage mode).

magnitudes for input voltages of 18 and 30 Vdc, respectively, can be observed. The 30-Vdc cases provide higher loop gains, which produce the lower output impedances that might be expected (see Equation 2.2). To illustrate specifically for the 30-Vdc input case, the impedance plots of Figure 4.14 and Figure 4.15 could be essentially derived by dividing the open loop impedance of Figure 4.6 by one plus the corresponding loop gains of Figure 4.12 and Figure 4.13 (see Equation 2.2).

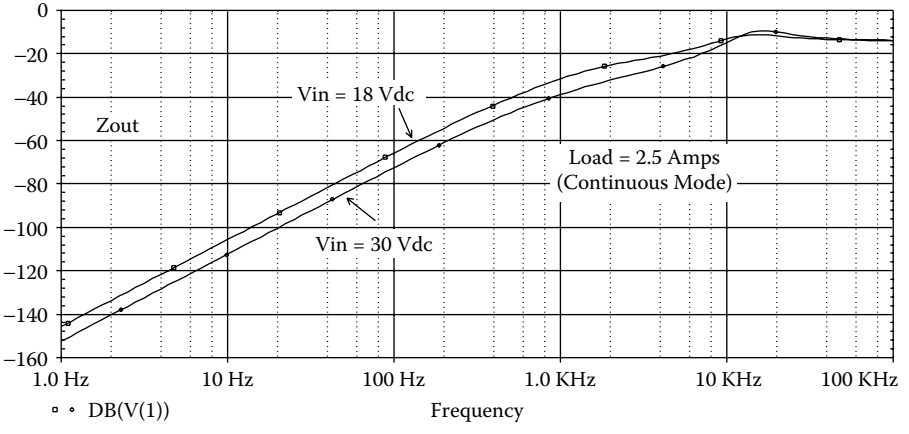


FIGURE 4.14
Buck SMPS continuous mode AC output impedance with input voltage change.

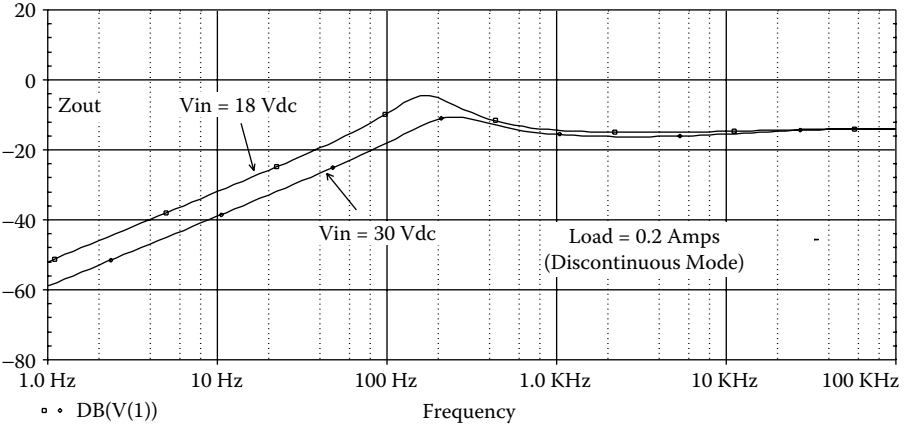


FIGURE 4.15
Buck SMPS discontinuous mode AC output impedance with input voltage change.

4.1.3.3 SMPS Line Regulation (Voltage Mode)

Consider the AC line rejection characteristics of the closed loop configuration. This is sometimes called "audio susceptibility." Figure 4.16 and Figure 4.17 show the AC attenuation of the SMPS for the indicated operating conditions of line and load. By examining the plots of these two figures, it is possible to observe the AC forward attenuation at input voltages of 18 and 30 Vdc for discontinuous and continuous modes, respectively. The 30-Vdc cases with the higher loop gains provide the greater attenuations, as one might expect (see Equation 2.1). To illustrate specifically for the 30-Vdc input case, the attenuation plots of Figure 4.16 and Figure 4.17 could be essentially derived

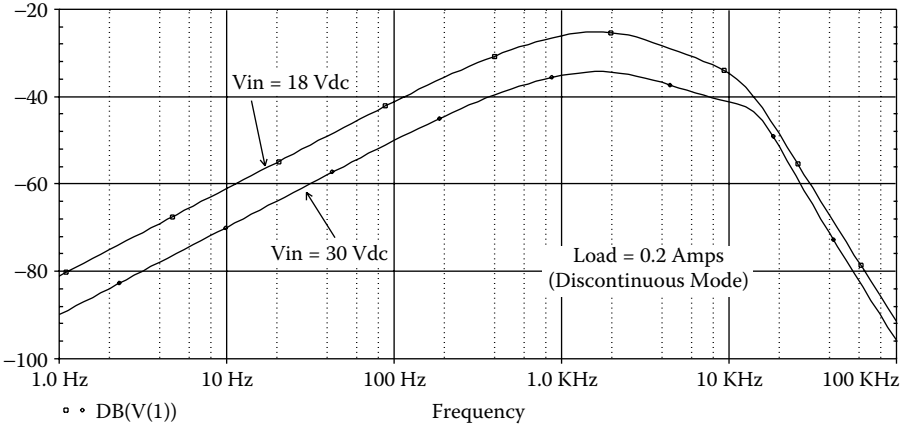


FIGURE 4.16
Buck SMPS continuous mode AC forward attenuation with input DC voltage change.

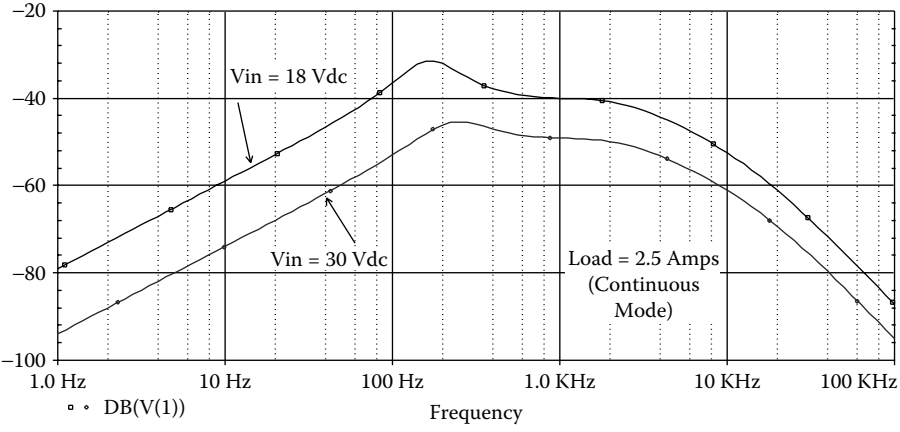


FIGURE 4.17
Buck SMPS discontinuous mode AC forward attenuation with input DC voltage change.

by dividing the open loop attenuations of Figure 4.8 by one plus the corresponding loop gains of Figure 4.12 and Figure 4.13 (Equation 2.1).

4.1.3.4 SMPS Feedforward Analysis

In many applications that utilize voltage mode control, the AC line rejection requirements are sometimes difficult to satisfy because of the difficulty in achieving the required AC loop gain and maintaining AC loop stability in the continuous mode. One technique of improving this situation is to provide a type of input voltage feedforward. This is implemented by letting the slope of the pulse width modulator (PWM) control ramp (Figure 4.1) be proportional to the input line voltage. For fixed-frequency converters, this translates into a control ramp amplitude that is proportional to input voltage.

Since the PWM gain is inversely proportional to this ramp amplitude, it has the effect of *reducing* loop gain with increasing input voltage. On the other hand, an increasing input voltage will increase the converter control to output gain, thereby *increasing* loop gain. With these offsetting effects, the feedback control loop can effectively be fixed and "linearized" by being almost if not completely independent of input voltage variations. Although this gain stabilizing effect simplifies the control loop, the AC line rejection improvement is in reality achieved by the immediate duty ratio adjustment being made with the immediate change in input voltage. Perfect feedforward compensation is generally not practical, but considerable improvements can be realized.

Take the open loop converter that produced the results of Figure 4.5 and, instead of a fixed $D = 0.4$, ideally add some feedforward by letting d have the following inverse relationship to V_g:

$$d = \frac{1}{\left(\frac{v_g}{V}\right)} = \frac{1}{\left(\frac{v_g}{12}\right)} = \frac{12}{v_g} \tag{4.4}$$

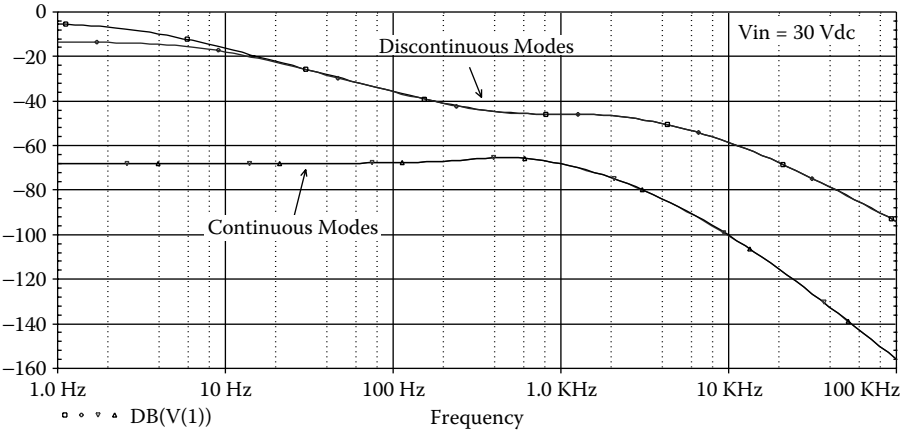


FIGURE 4.18
Buck converter AC forward transfer function with feedforward.

Comparing the results of Figure 4.5 to those in Figure 4.18 makes it possible to see the dramatic increase in line to output attenuation for the continuous mode cases at the lower frequencies (~60 dB improvement). The discontinuous modes are only slightly affected.

4.1.4 SMPS Combined Feedback and Feedforward Analysis (Line Regulation)

Now take the closed loop feedback regulated circuit of Figure 4.9 and add the feedforward implementation of Section 4.1.3.4 to it and compare the AC line rejection characteristics to those obtained with feedback only, as shown in Figure 4.16 and Figure 4.17. With the PWM control ramp amplitude simply modulated by the input voltage, the implementation is simply to multiply the circuit model control voltage, d, by a function inversely proportional to the input voltage. A function as expressed by Equation 4.5 might be a possible idealistic implementation:

$$d = \frac{v_e}{\left(\frac{v_g}{12}\right)} = 12\left(\frac{v_e}{v_g}\right) \tag{4.5}$$

The results are shown in Figure 4.19 and Figure 4.20. Compare these figures with Figure 4.16 and Figure 4.17, respectively, and note the improvement in forward attenuation with the addition of the feedforward compensation. About 50 dB of additional attenuation was noted for the

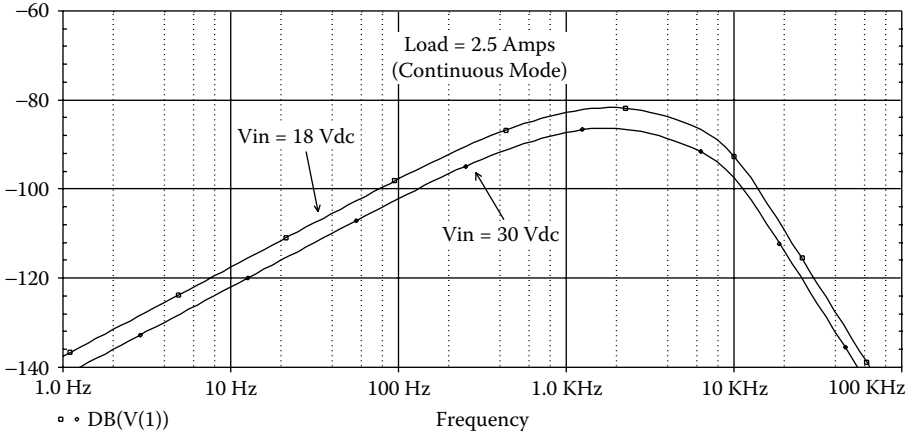


FIGURE 4.19
Buck SMPS with feedforward compensation. Continuous mode AC forward attenuation with input DC voltage change.

continuous mode cases, but practically no noticeable increase was noted for the discontinuous mode cases. The idealistic feedforward addition considered here, combined with the feedback, provides somewhat idealistic results that may not be achievable in actual practice. Nevertheless, the method of analysis and the general expected results have been shown.

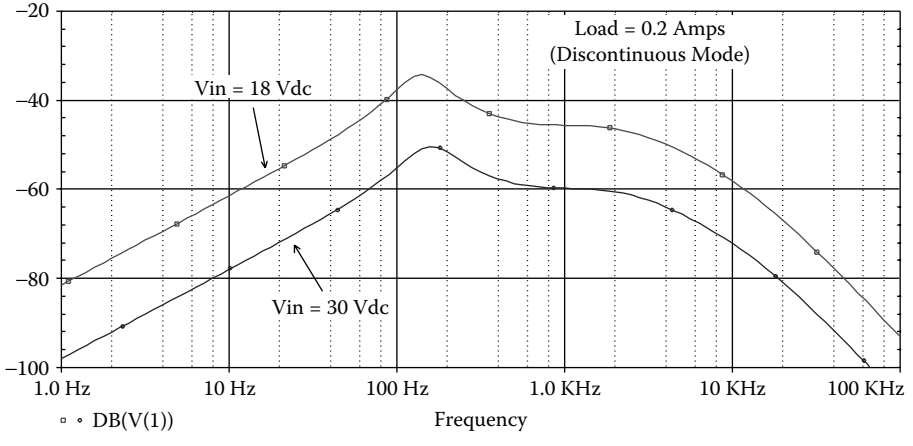


FIGURE 4.20
Buck SMPS with feedforward compensation. Discontinuous mode AC forward attenuation with input DC voltage change.

4.2 Buck Converter SMPS Analysis (Current Mode)

A current mode control converter actually starts out as the voltage mode converter described in Section 4.1. An inductor current sense circuit is added and a feedback control loop is established so that an applied control signal can regulate or control the inductor current. Several types of control for this current are possible, depending on the desired characteristics. When the inductor current is triangular and has an averaged DC value, one can sense and regulate the peak current or, in some cases, the converse valley current. In some designs, the average inductor current is determined and regulated, providing a possibly more desirable control for some applications. For output voltage regulation, a second outer control loop circuit senses output voltage and its output provides the control signal for regulating the inductor current. Controlling the inductor current subsequently allows regulation of the output voltage.[5,12] (A PSPICE netlist, labeled Netlist 4.3, is used for these current mode analysis simulations.)

NETLIST 4.3

```
BUCK CONVERTER SMPS, CURRENT MODE, ANALYSIS
*
************************************************************
*
** SOURCE-LOAD CONFIGURATION FOR
** FIGURES 4.24 AND 4.25
** BUCK SMPS AC LOOP GAIN AND PHASE
** WITH LOAD CHANGE (CURRENT MODE)*
VIN N 0 DC 30
ILOAD 1 0 DC .2
.STEP ILOAD LIST .2 .7 1.2 2.5
LOL 14 16 1K
COL 16 15 1K
VAC 0 15 AC 1
.AC DEC 20 1 100K
.OPTIONS ITL2=200
*
************************************************************
*
** SOURCE-LOAD CONFIGURATION FOR
** FIGURES 4.26 AND 4.27
** BUCK SMPS AC LOOP GAIN AND PHASE
** WITH INPUT VOLTAGE CHANGE (CURRENT MODE)*
*ILOAD 1 0 DC 2.5
*ILOAD 1 0 DC .2
*VIN N 0 DC 30
*.STEP VIN LIST 18 30
*LOL 14 16 1K
*COL 16 15 1K
*VAC 0 15 AC 1
*.AC DEC 20 1 100K
```

```
*.OPTIONS STEPGMIN ITL2=200
*.NODESET  V(1)=12 V(8)=30 V(D)=.6 V(17)=1 V(13)=1 V(14)=1
*
************************************************************
*
** SOURCE-LOAD CONFIGURATION FOR
** FIGURE 4.28
** OUTPUT IMPEDANCE OF THE "OPEN VOLTAGE LOOP" CURRENT MODE
** CONVERTER*
*ILOAD 1 0 DC .2
*.STEP ILOAD LIST .2 .7 1.2 2.5
*VIN N 0 DC 30
*LOL 14 16 1K
*COL 16 15 1K
*VAC 0 15 AC 0
*IAC 1 0 AC 1
*.AC DEC 20 1 100K
*.OPTIONS STEPGMIN ITL2=200
*
************************************************************
*
** SOURCE-LOAD CONFIGURATION FOR
** FIGURE 4.29 AND 4.30
** AC FORWARD TRANSFER FUNCTION OF THE "OPEN VOLTAGE LOOP"
** CURRENT MODE CONVERTER WITHOUT THE INPUT FILTER.*
*ILOAD 1 0 DC .2
*.STEP ILOAD LIST .2 .7 1.2 2.5
*VIN N 0 DC 30 AC 1
*LOL 14 16 1K
*COL 16 15 1K
*VAC 0 15 AC 0
*.AC DEC 20 1 100K
*.OPTIONS STEPGMIN ITL2=200
*
************************************************************
*
** SOURCE-LOAD CONFIGURATION FOR
** FIGURE 4.31
**BUCK CONVERTER AC "D TO OUTPUT" TRANSFER FUNCTION (CURRENT MODE).*
*ILOAD 1 0 DC .2
*.STEP ILOAD LIST .2 .7 1.2 2.5
*VIN N 0 DC 30
*LOL 14 16 1K
*COL 16 15 1K
*VAC 0 15 AC 1
*.AC DEC 20 1 100K
*.OPTIONS STEPGMIN ITL2=200
*
************************************************************
*
** SOURCE-LOAD CONFIGURATION FOR
** FIGURE 4.32
** INNER INDUCTOR CURRENT CONTROL LOOP GAIN*
*ILOAD 1 0 DC .2
*.STEP ILOAD LIST 1.2 2.5
```

```
*VIN N 0 DC 30
*LOL 14 16 1K
*COL 16 15 1K
*VAC 0 15 AC 0
*HI 100 0 VM1 1
*LOL2 100 101 1000
*COL2 101 102 1000
*VAC2 0 102 AC 1
*.AC DEC 20 1 100K
*.OPTIONS STEPGMIN ITL2=200
*
** NOTE: THE FOLLOWING EDC REMAINS IN THE CIRCUIT FOR ALL ANALYSIS
** BUT MUST ALTERNATE WITH THE SECOND EDC BELOW FOR THIS
** INNER INDUCTOR CURRENT CONTROL LOOP GAIN ANALYSIS ONLY
EDC 17 0 VALUE = {(V(16)/1-I(VM1))/(.125*(24+V(8)-V(1)))}
*EDC 17 0 VALUE = {(V(16)/1-V(101))/(.125*(24+V(8)-V(1)))}
*
************************************************************
*
** SOURCE-LOAD CONFIGURATION FOR
** FIGURE 4.33
** OUTPUT IMPEDANCE OF THE CURRENT MODE SMPS*
*ILOAD 1 0 DC .2
*.STEP ILOAD LIST .2 .7 1.2 2.5
*VIN N 0 DC 30
*LOL 14 16 1P
*COL 16 15 1P
*VAC 0 15 AC 0
*IAC 1 0 AC 1
*.AC DEC 20 1 100K
*.OPTIONS STEPGMIN ITL2=200
*
************************************************************
*
** SOURCE-LOAD CONFIGURATION FOR
** FIGURE 4.34 AND 4.35
** AC LINE REJECTION OF THE CURRENT MODE SMPS*
*VIN N 0 DC 30 AC 1
*VIN N 0 DC 18 AC 1
*ILOAD 1 0 DC .2
*.STEP ILOAD LIST .2 .7 1.2 2.5
*LOL 14 16 1P
*COL 16 15 1P
*VAC 0 15 AC 0
*.AC DEC 20 1 100K
*.OPTIONS STEPGMIN ITL2=200
*.NODESET  V(1)=12 V(8)=30 V(D)=.6 V(17)=1 V(13)=1 V(14)=1
*
************************************************************
*
**CURRENT MODE SMPS NETLIST
*
C4 1 0 .1U
```

```
C3 1 3 2000U
R3 3 0 .2
GLD 2 K VALUE = {V(D)**2*(V(8)/V(1))*(V(8)-V(1))*.125}
VM3 K 1
XD3 2 1 DIDEAL
L2 4 2 40U
E1 4 5 VALUE = {V(8)*V(D)}
VM1 0 5
GILD 6 7 VALUE = {I(VM3)*V(1)/V(8)}
G1 0 6 VALUE = {I(VM1)*V(D)}
XD1 6 7 DIDEAL
XD2 0 6 DIDEAL
VM2 7 0 DC 1
F2 8 0 VM2 1
C2 8 0 10U
C1 8 9 175U
R1 9 0 1
L1 N 8 50U
R4 1 10 38K
R5 10 0 10K
VREF 11 0 DC 2.5
X1 11 10 13 OASIMP
C5 13 12 .01U
R6 12 10 300K
C6 12 10 470P
EVC 14 0 13 0 1
*
.SUBCKT OASIMP 1 2 3
RIN 1 2 10MEG
G1 0 3 1 2 100K
RO 3 0 10
CO 3 0 .016
.ENDS OASIMP
*
X2 D 17 DIDEAL
EDD 18 0 VALUE = {(V(16)/1)/(.25*(12+V(8)-V(1)))}
X3 D 18 DIDEAL
IRM 0 D DC 1M
RM 0 D 10K
*
.SUBCKT DIDEAL 1 2
VAS 1 3 DC -1U
D1 3 2 D
D2 3 4 D
D3 4 2 D1
FAS 4 2 VAS 1
.MODEL D D IS=1E-6
.MODEL D1 D
CC 1 2 .1P
.ENDS DIDEAL
*
.PROBE
.END
```

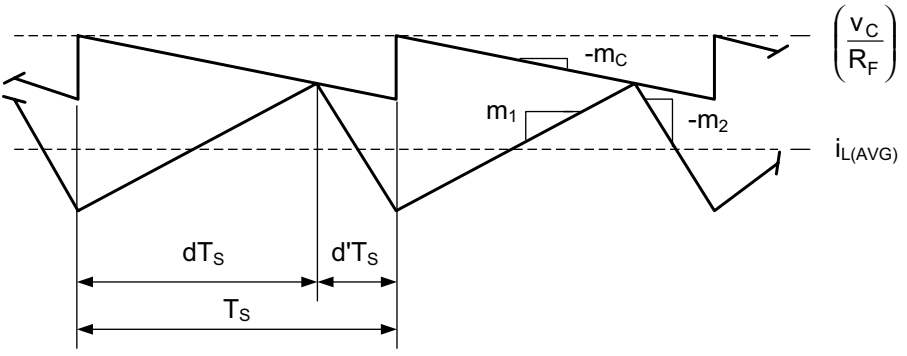


FIGURE 4.21
Peak current sensing current mode control waveforms (continuous conduction mode).

4.2.1 Current Mode Converter Model Setup

To maintain a sense of consistency, use the same converter of Figure 4.1 and its model (Figure 4.2) and implement a current mode control scheme with it for the current mode analysis. Figure 4.21 and Figure 4.22 show the fundamental inductor current and current control waveforms for the continuous and discontinuous modes of operation, respectively. From these waveforms, the following expressions for the control parameter, d, are determined. Slope m_1 is the ON time slope of the inductor current and $-m_2$ is the OFF time slope. Slope m_C is that of the stabilizing ramp added to the peak current control voltage, v_C/R_f, for stability.[12] For continuous conduction mode, d is derived from Figure 4.21 as:

$$d = \frac{\frac{v_C}{R_f} - i_{L2}}{\frac{T_S}{2L_2}(2m_C L_2 + v_g - v)} \tag{4.6}$$

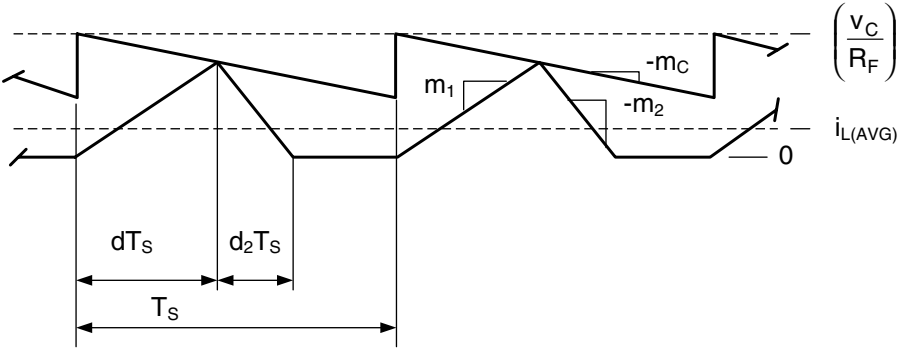


FIGURE 4.22
Peak current sensing current mode control waveforms (discontinuous conduction mode).

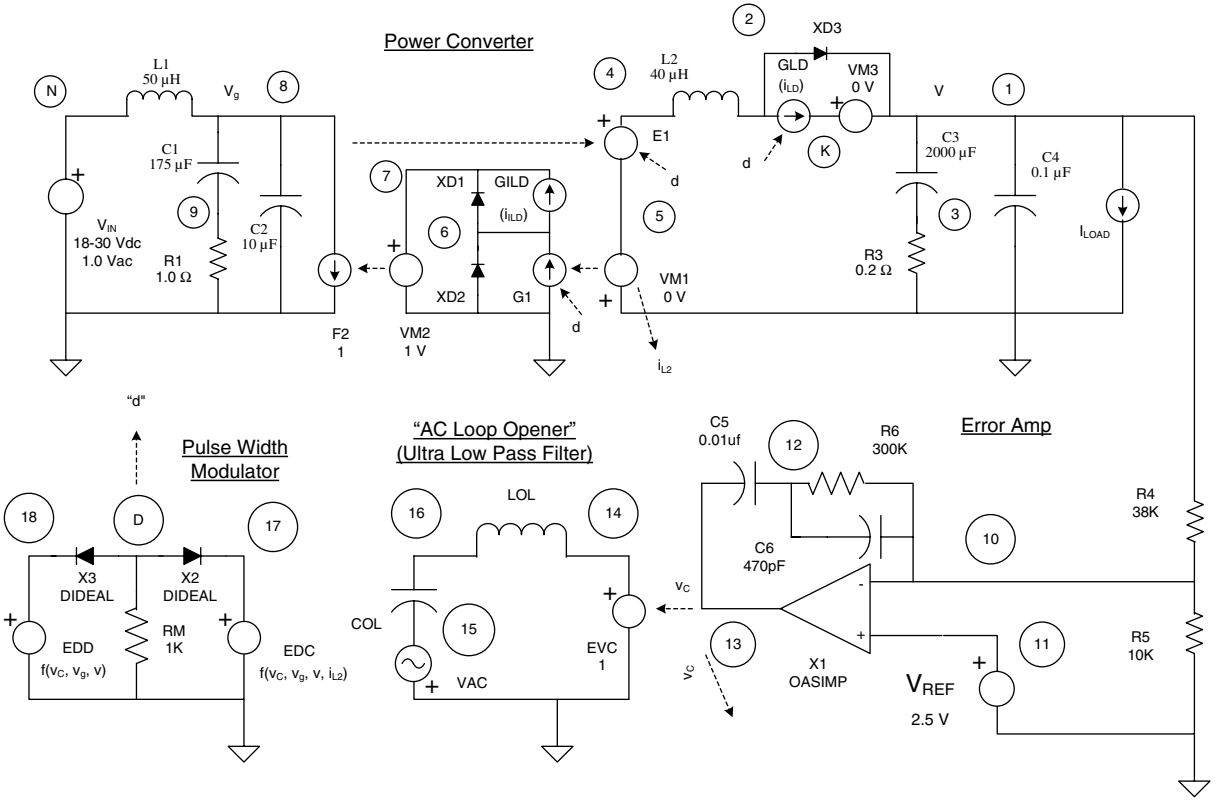


FIGURE 4.23
Buck converter switching regulator model (current mode).

and the discontinuous mode case from Figure 4.22 is:

$$d = \frac{\frac{v_C}{R_f}}{\frac{T_S}{L_2}(m_C L_2 + v_g - v)} \tag{4.7}$$

The current mode analysis model is shown in Figure 4.23. The dependent voltage source EDC will produce a voltage at node 17 that is equal to the calculated magnitude of the continuous mode duty ratio, d, as expressed by Equation 4.6. The dependent voltage source EDD produces a voltage at node 18 representing the calculated magnitude of the discontinuous mode duty ratio, d, expressed by Equation 4.7. Each of these two duty ratio parameters is continuously calculated and diode ORed by the two ideal diodes, X2 and X3, producing the smaller value of d at node D. This smaller value is the correct d to be used for control of the converter and will correspond to its correct conduction mode. (This is also true for the current mode boost and buck–boost current mode topologies.) The correct conduction mode for the converter is determined implicitly as usual. For optimum stability,[5] m_C is set equal to $-m_2$ or

$$m_C = \frac{V}{L_2} = \frac{12V}{40\,\mu H} = 0.3\frac{V}{\mu S} \tag{4.8}$$

R_f will be 1 Ω because this scaling will be appropriate for this analysis (Chapter 6 contains more information about this selection). With the value of T_S still at 10 μS, and L_2 at 40 μH, equations for the values of EDC and EDD can now be inserted in the model.

4.2.2 Open Voltage Loop AC Analysis (Continuous and Discontinuous Modes)

The plot of Figure 4.24 shows the continuous mode loop gain and phase of the outer voltage control loop of the current mode switching regulator; Figure 4.25 shows the discontinuous mode cases. (The inner current control loop is closed via the equation for EDC.) The loads are the same as they were for the voltage mode regulator in Section 4.1.3. The error amplifier frequency response characteristic was modified from the voltage mode example to provide more practical results for the current mode analysis.

As was the case for the voltage mode converter, note that the continuous mode gains in Figure 4.24 are independent of load current variations (current sink loads), but that the gains in the discontinuous mode case of Figure 4.25 do vary with load currents. Note that the unity gain crossover frequency is

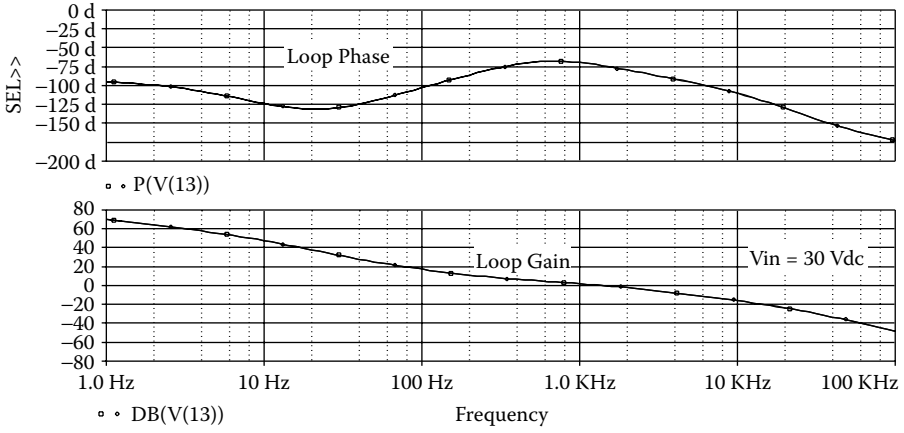


FIGURE 4.24
Buck SMPS continuous mode AC loop gain and phase with load change (current mode).

reduced for the discontinuous mode cases and continues to decrease for continuously decreasing loads. Also, to ensure that the feedback control loop maintains AC stability, the phase shift must not approach or exceed a magnitude of –180° at the unity gain crossover frequency. As stated earlier, typical desired numbers for the phase and gain margins are 45° and 10 dB, respectively. Kuo[10] and D'Azzo and Houpis[11] offer more fundamental information on feedback control stability.

Now consider the effects of input DC voltage variations on loop gain by stepping V_{in} from 18 to 30 Vdc with the load cases of 2.5 amps (continuous)

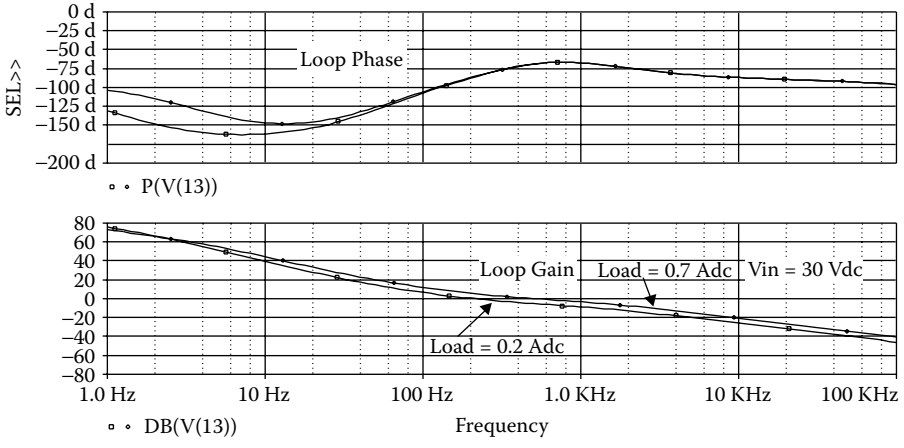


FIGURE 4.25
Buck SMPS discontinuous mode AC loop gain and phase with load change (current mode).

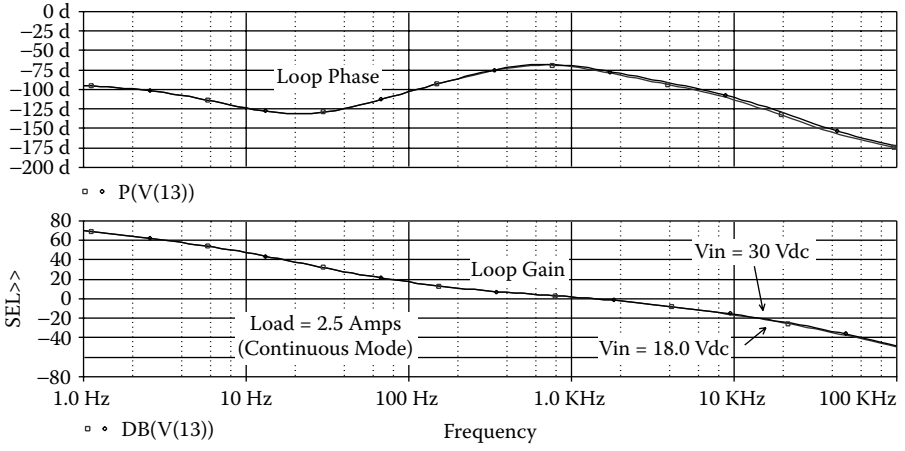


FIGURE 4.26
Buck SMPS continuous mode AC loop gain and phase with input voltage change (current mode).

and 0.2 amps (discontinuous). Figure 4.26 and Figure 4.27 show the respective plots. Only the discontinuous mode case plot indicates a noticeable shift in gain with the input voltage. This may not be true for all designs, but a small change will generally be noticed.

4.2.2.1 Open Voltage Loop AC Output Impedance (Current Mode)

Now look at the AC output impedance of the converter for the same conditions as those set up in the previous section. This is the output impedance of the

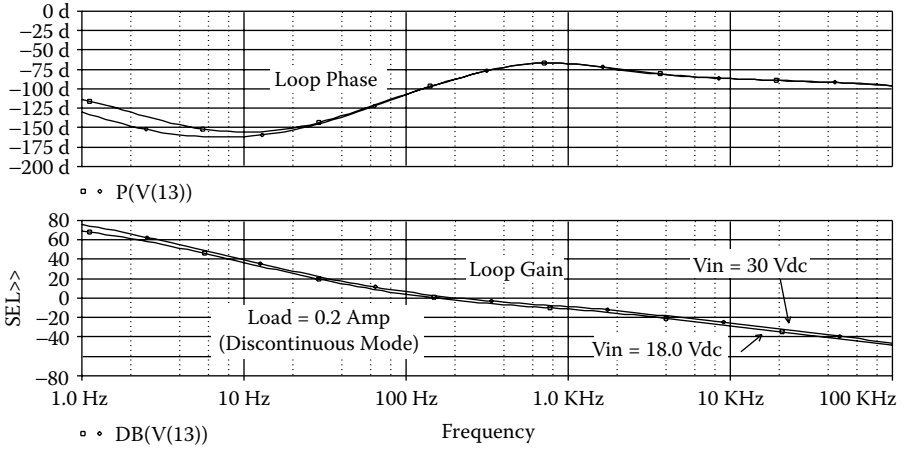


FIGURE 4.27
Buck SMPS discontinuous mode AC loop gain and phase with input voltage change (current mode).

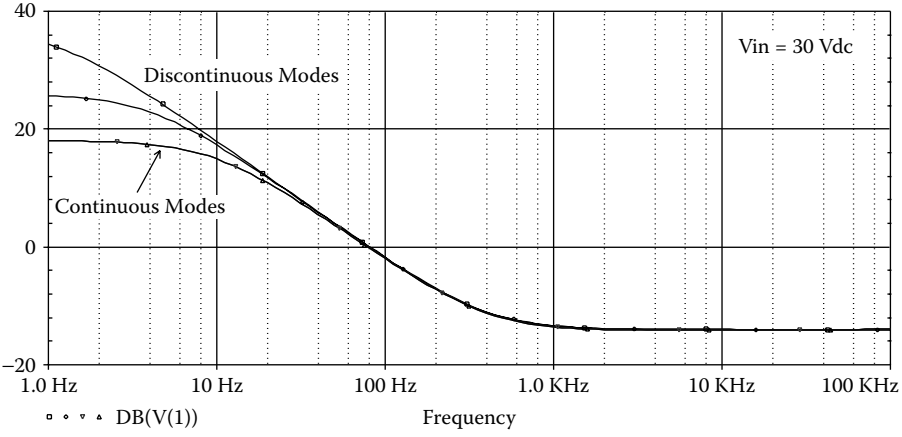


FIGURE 4.28
Output impedance of the open voltage loop current mode converter.

SMPS with the inner inductor current control loop closed and the outer output voltage control loop opened "AC wise" with the ultralow-pass filter circuit (see Section 4.1.3). Figure 4.28 shows the plot (0 dB is equivalent to 1 Ω). The low-frequency discontinuous mode output impedances are relatively high and also a function of the load current prior to breaking with the output filter capacitor, C3, at frequencies near 4 Hz. The continuous mode cases are theoretically independent of load current and have high impedance at low frequencies and even approaching that of the discontinuous mode cases. This is considerably higher than that of the voltage mode output impedance when comparing this same converter with that of the voltage mode case shown in Figure 4.6. This is characteristic of current mode converters.

4.2.2.2 Open Voltage Loop Forward Transfer Function (Current Mode)

The AC line rejection of the current mode open voltage loop configuration will now be examined. Figure 4.29 shows the results without the input filter. Figure 4.30 shows the result with the input filter added.

4.2.2.3 Control to Output Analysis (Current Mode)

With the voltage loop opened AC wise by letting LOL and COL (Figure 4.23) be very large values, the control to output AC voltage transfer function of the current mode converter is now considered. The load currents are 1.2 and 2.5 amps for continuous conduction mode and 0.2 and 0.7 amps for the discontinuous conduction mode cases. The input voltage is fixed at 30 Vdc and the output voltage is maintained at 12 Vdc by the voltage loop DC-only feedback control. Figure 4.31 shows the analysis results. Note that the continuous mode gains are independent of load and the discontinuous mode

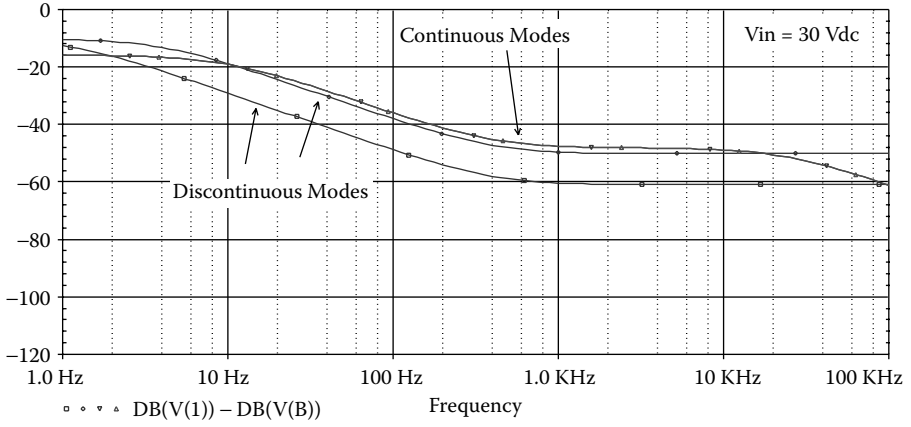


FIGURE 4.29
AC forward transfer function of the open voltage loop current mode converter without the input filter.

cases do vary with load current. The gain decreases at a slope of –1, which is generally characteristic of current mode converters in continuous and discontinuous modes of operation.

4.2.2.4 Inner Inductor Current Control Loop Gain

Occasionally, it may be desirable to examine the inner inductor current control loop to see if its AC characteristics are as expected. This is accomplished by opening the inductor current feedback signal AC wise (this current is sensed

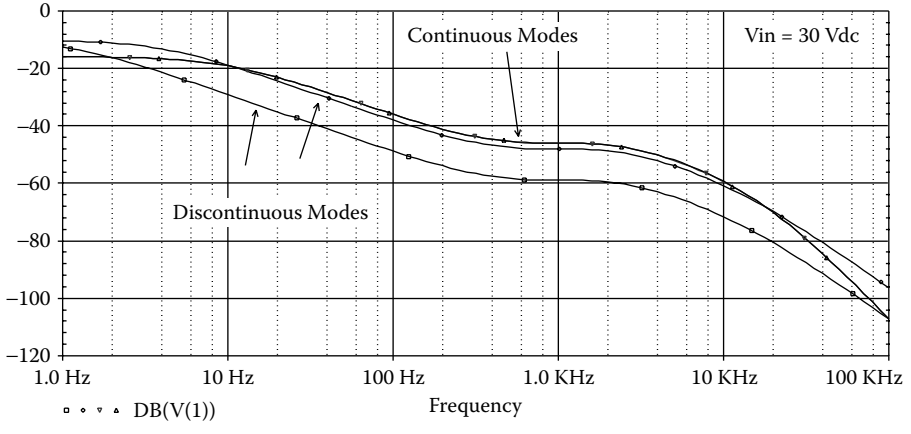


FIGURE 4.30
AC forward transfer function of the open voltage loop current mode converter with input filter added.

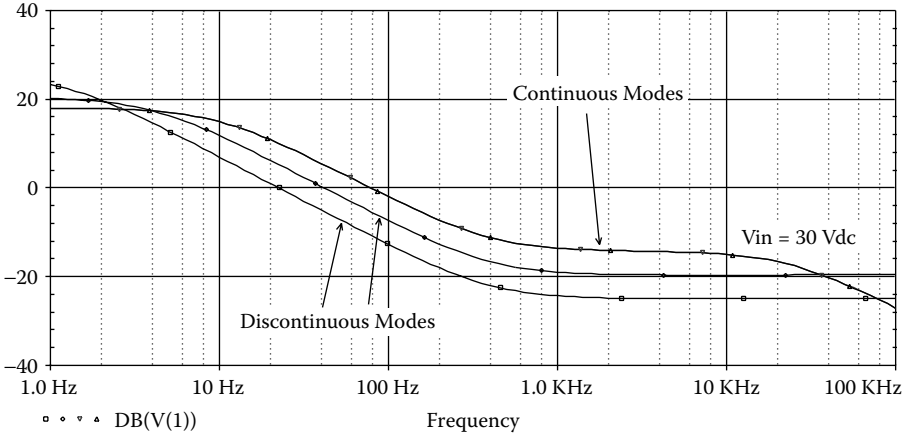


FIGURE 4.31
Buck converter AC "*d* to output" transfer function (current mode).

by VM1 in Figure 4.23). The outer voltage loop will also be opened for AC signals by maintaining the ultralow-pass filter with large values of LOL and COL; however, its VAC is now set to zero. Then another ultralow-pass filter is created for the inductor current signal to open its loop for AC analysis. (Note: the circuit for this second ultralow-pass filter is not shown on the model schematic of Figure 4.23, but it can be easily visualized from the current mode netlist, Netlist 4.3.) VAC for this new ultralow-pass filter insertion is conveniently set to 1.0 VAC as the AC stimulus for analysis for this loop. Figure 4.32 shows the results.

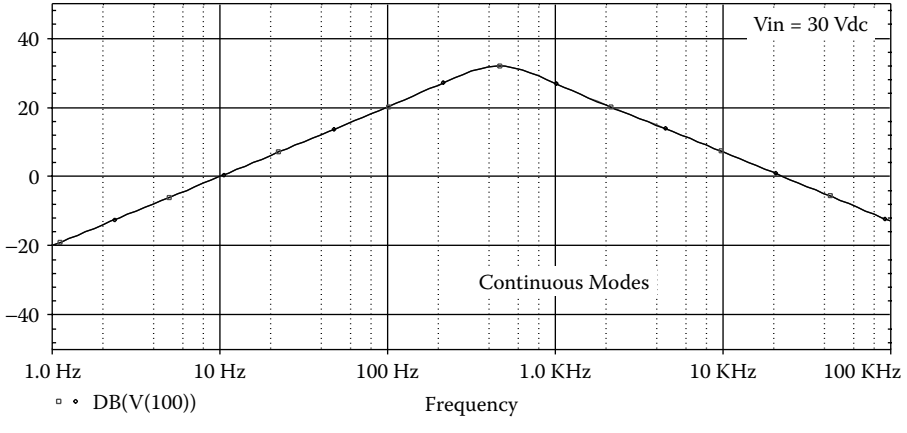


FIGURE 4.32
Inner inductor current control loop gain.

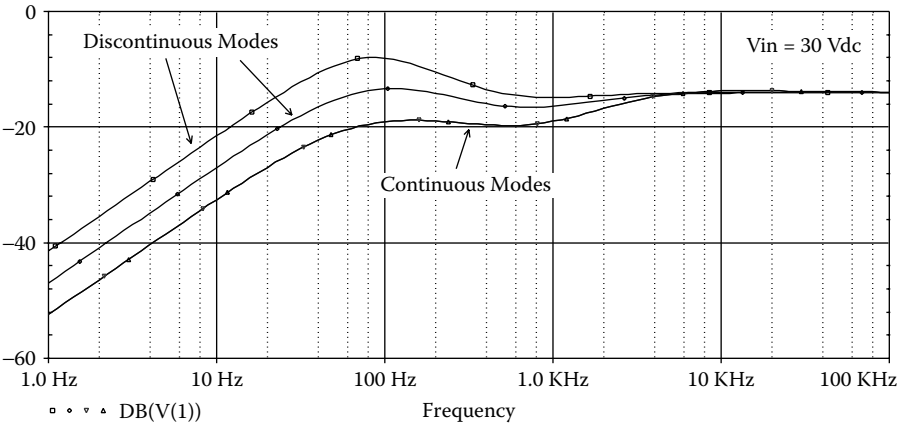


FIGURE 4.33
Output impedance of the current mode SMPS.

4.2.3 SMPS Closed Loop Analysis (Current Mode)

Now close the inner current loop and the outer voltage loop, configure the SMPS in its normal operating configuration, and then examine its properties of output impedance and line regulation. The addition of an input voltage feedforward analysis is not considered here. This implementation is generally not necessary with current mode control because of its superior line rejection characteristics in continuous as well as discontinuous modes.

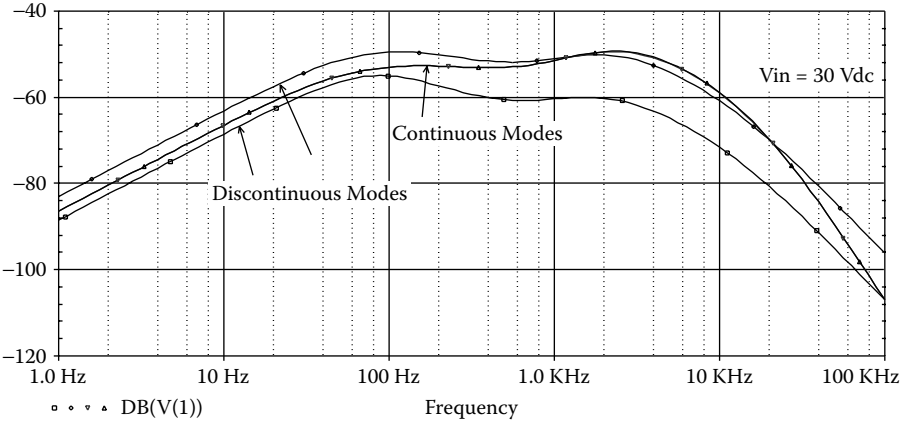


FIGURE 4.34
AC line rejection of the current mode SMPS (*Vin* = 30 Vdc).

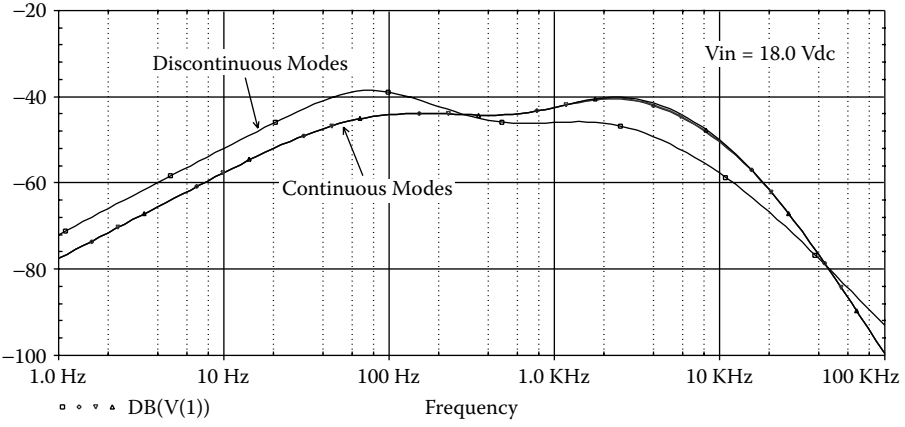


FIGURE 4.35
AC line rejection of the current mode SMPS (*Vin* = 18 Vdc).

4.2.3.1 SMPS Output Impedance (Current Mode)

Now look at the SMPS output impedance for the extreme variations in load currents considered in the open voltage loop gain analyses in Section 4.2.2.1. Input voltage was held at 30 Vdc. The plot of Figure 4.33 shows the AC impedance magnitudes. Notice that the impedances of Figure 4.28 are reduced to those of Figure 4.33 by the voltage loop gain factor of Equation 2.2.

4.2.3.2 SMPS Line Regulation (Current Mode)

Figure 4.34 and Figure 4.35 show the plots of AC line rejection for input voltages of 30 and 18 Vdc, respectively. Note the excellent line rejection for all conditions; this is one of the salient characteristics of current mode control.

4.3 Summary

This chapter has considered most of the fundamental kinds of DC and AC analysis in which one might be interested when analyzing a very basic switching regulator. These have been for the power converter with no duty ratio control; the voltage mode-controlled SMPS; and the current mode-controlled SMPS. Chapter 6 will continue with the general theme of this chapter and provide more advanced or comprehensive detailed analysis methods.

These will include the large signal transient analyses as well as the DC and AC analysis methods presented in this chapter. To be on firm ground, it is recommended that the reader consult some of the numerous references[14,24,26] regarding the fundamentals of SMPSs because here only the fundamentals of analysis and very few basic theoretical, operating, or design fundamentals have been presented.