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# **Application Note**

AN-SMPS-16822CCM-1

**CoolSET**<sup>TM</sup>

Design of Flyback SMPS in continous conduction mode operation

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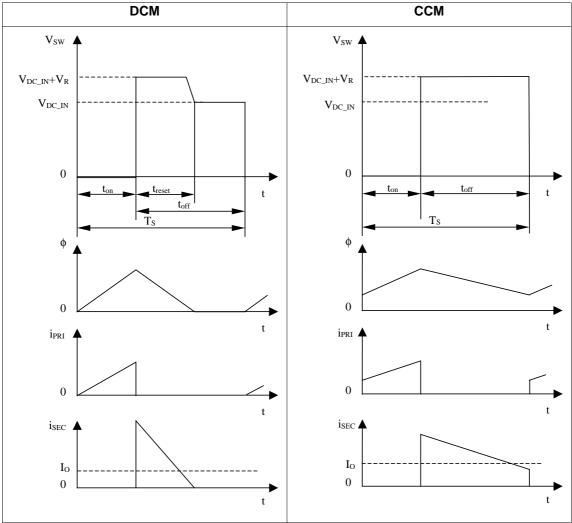


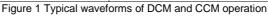
# Design of Flyback SMPS in continuous conduction mode operation Abstract

For SMPS in flyback configuration, discontinuous conduction mode (DCM) is popular because of its simple transfer function characteristics. However, in some applications, continuous conduction mode (CCM) is preferred to achieve high efficiency. In the paper, CCM operation is discussed in detail. CoolSET<sup>™</sup> TDA16822, which includes the PWM controller and CoolMOS<sup>™</sup>, is introduced for SMPS application. It can work at both of DCM and CCM. The application circuit with TDA16822 is described briefly. Based on the same output specification requirement, two evaluation boards with TDA16822, for DCM and CCM operation respectively, are set up. The experimental test is done for these two boards and the performances for DCM and CCM are summarized in the final.

# Introduction to continuous conduction mode in flyback converter with current mode control

the difference between discontinuous (DCM) and continuous conduction mode (CCM)







The typical voltage, current and magnetic flux waveforms in continuous conduction mode (CCM) for flyback converter are shown in Figure 1. For comparison, the typical waveforms in DCM are demonstrated together. It can be seen that in CCM neither the primary current nor the secondary current is truly continuous. Hence, for flyback converter, continuous conduction mode refers to the incomplete demagnetization of the transformer core over a cycle of operation.

### Introduction to current mode control

Current mode control is very popular in SMPS design. In current mode control, a control voltage  $V_{FB}$  directly controls the inductor current that feeds the output stage and thus output voltage. It has a several advantages over the conventional direct duty cycle control:

- (1) The peak current of the switch can be limited by simply putting an upper limit on the control voltage and the overload protection is obtained.
- (2) One pole corresponding to the primary inductor is removed from the control-to-output transfer function  $V_O(s)/V_{FB}(s)$ , thus simplifying the compensation in the negative-feedback system.
- (3) Good line regulation is obtained. The duty cycle will be adjusted directly to accommodate the changes in the input voltage, resulting in excellent rejection of input line transients.

# Benefit of CCM compared to DCM in flyback converter with current mode control

#### Low peak current and RMS current

The shapes of primary and secondary current waveforms in CCM operation are trapezoid instead of triangular in DCM operation. So at the same output power situation the peak current and the equivalent RMS current are lower than those in DCM operation. Then the conduction loss on the primary switch and secondary rectifier diode is less than that in DCM. It will help to increase the total efficiency of the SMPS.



# Drawback of CCM compared to DCM in flyback converter with current mode control

- (1) A right-half-plane zero exists and provides additional phase lag while boosting gain. It makes good compensation difficult.
- (2) The overload protection threshold changes with input voltage variation.

For DCM operation, the output power  $P_{out}$  is obtained as:

$$P_{out} = \eta P_{in} = \frac{1}{2} \eta L_P I_{peak}^2 f_S$$
<sup>(1)</sup>

where,  $\eta$  is efficiency of the SMPS,  $P_{in}$  is the input power,  $L_P$  is the primary inductance of the transformer,  $I_{peak}$  is the peak current passing through the power MOS and  $f_s$  is the switching frequency of the power MOS. For fixed switching frequency operation,  $P_{out}$  is only dependent on  $I_{peak}$  which is controlled by  $V_{FB}$ . Hense the upper limit  $V_{FB}$  will limit the maximum  $P_{out}$  which is not dependent on the input line voltage for DCM operation.

However for CCM operation, the equation (1) is not valid any more. It should be modified as follow. The primary current waveform is shown in Figure 2. Then the input power  $P_{in}$  is derived as:

$$P_{in} = V_{in}I_a D = N_{ratio}V_O(1-D)I_a$$
<sup>(2)</sup>

where,  $V_{in}$  is the input DC voltage,  $I_a$  is the average inductor current during turn-on period, D is the switching duty cycle,  $N_{ratio}$  is the turn ratio of the transformer and  $V_0$  is the output voltage. The inductor current ripple  $\Delta I_L$  is

$$\Delta I_L = \frac{V_{in}}{L_P} DT_S = \frac{N_{ratio} V_O(1-D)}{L_P f_S}$$
(3)



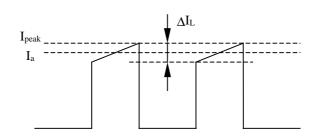


Figure 2 Primary current waveform in CCM operation

$$I_{peak} = I_a + \frac{1}{2}\Delta I_L \tag{4}$$

from Equation (4), it is obtained

$$I_{a} = I_{peak} - \frac{1}{2}\Delta I_{L} = I_{peak} - \frac{V_{in}}{2L_{p}}DT_{S} = I_{peak} - \frac{N_{ratio}V_{O}(1-D)}{2L_{p}f_{S}}$$
(5)

combine Eq(2) and Eq(5), then

$$P_{in} = N_{ratio} V_O (1 - D) (I_{peak} - \frac{N_{ratio} V_O (1 - D)}{2L_P f_S})$$
(6)

$$P_{out} = \eta P_{in} = \eta N_{ratio} V_O (1 - D) (I_{peak} - \frac{N_{ratio} V_O (1 - D)}{2L_P f_S})$$
(7)

It can be seen that the maximum output power is not only dependent on the peak current but also the duty cycle, i.e. input voltage.



# SMPS circuit with TDA16822

## Introduction to CoolSET<sup>™</sup> TDA16822

The TDA16822 is a current mode control pulse width modulator with built in CoolMOS<sup>TM</sup> transistor and working at fix switching frequency  $f_S=100kHz$ . It fulfills the requirement of minimum external control circuitry for a flyback application. The block diagram with the typical application circuit is shown in Figure 3.

There are only 6 active Pins with DIP8 package. To safeguard the system, some basic protection function such as IC undervoltage lockout, maximum duty cycle limitation, overload and open loop protection, overvoltage protection during startup and latched thermal shutdown are built in. With external current sense resistor, the maximum peak current limitation is adjustable. With the propagation delay compensation, the current overshoot dependent on *di/dt* is minimized. Because there is no demagnetized protection for this IC, it can work in both DCM and CCM.

## SMPS circuit design on CCM operation with TDA16822

In this section we concentrate on the design for CCM operation. The detail circuit design steps of transformer and the regulation loop will be introduced with a design example of 8.8V/1.7A SMPS. For DCM design, please refer to the application notes of "CoolSET<sup>™</sup> TDA16831...-34 for OFF-Line Switch Mode Power Supplies" and "CoolSET<sup>™</sup> application note supplement".

The target specification is as below.

Universal AC input:  $85VAC \sim 265VAC$ . Output voltage  $V_0$ : 8.8VOutput current  $I_0$ : 1.7AEfficiency: 80%



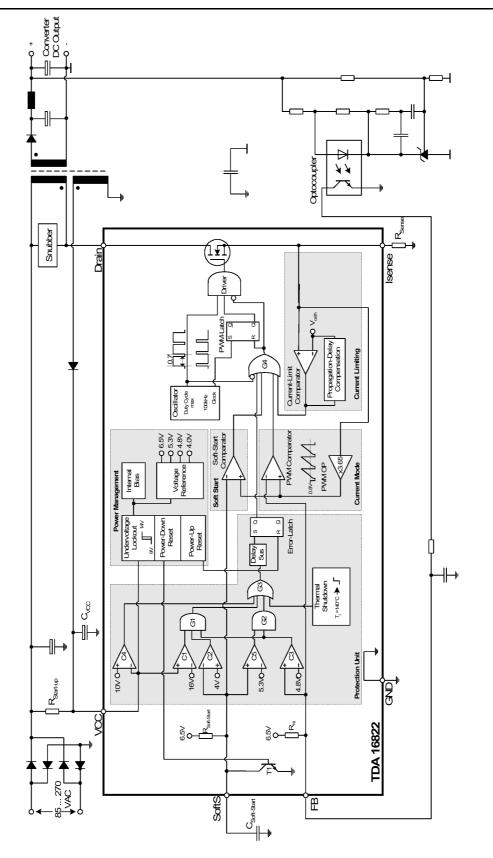


Figure 3 Block diagram and typical application of TDA16822



## Transformer design

#### (1) maximum duty cycle D<sub>max</sub>

The transformer turn ratio of primary to secondary could be obtained as:

$$N_{ratio} = \frac{V_{ds\,max} - V_{i\,max}}{V_o + V_{diode}} \tag{8}$$

where,  $V_{dsmax}$  is the maximum voltage across drain to source of the MOSFET,  $V_{imax}$  is the maximum input DC voltage and  $V_{diode}$  is the on state voltage drop of secondary rectifier diode. Then the maximum duty cycle  $D_{max}$  is shown as:

$$D_{max} = \frac{(V_o + V_{diode})N_{ratio}}{V_{imin} + (V_o + V_{diode})N_{ratio}}$$
(9)

where,  $V_{imin}$  is the minimum input DC voltage. If  $D_{max}$  is higher than 0.5, the slope compensation is required for the system stability.

In this design, we choose  $V_{dsmax}$ =450V,  $V_{imax}$ =380V,  $V_{imin}$ =90V,  $V_{O}$ =8.8V and  $V_{diode}$ =0.5V, and then the turn ratio is

$$N_{ratio} = \frac{V_{ds\,max} - V_{i\,max}}{V_o + V_{diode}} = \frac{450 - 380}{8.8 + 0.5} = 7.53 \tag{10}$$

and

$$D_{\max} = \frac{(V_o + V_{diode})N_{ratio}}{V_{i\min} + (V_o + V_{diode})N_{ratio}} = \frac{(8.8 + 0.5) \cdot 7.53}{90 + (8.8 + 0.5) \cdot 7.53} = 0.44$$
(11)

Slope compensation is not necessary for this design.

### (2) transformer primary inductance $L_P$

For CCM operation, there is no upper limit for primary inductance  $L_P$  to guarantee the demagnetization of the transformer. The larger the  $L_P$ , the lower the inductor current ripple  $\Delta I_L$  and the lower the RMS values of the primary current through the MOSFET and secondary current through rectifier diode. Accordingly, the conduction losses of the MOSFET and rectifier diode could be lower. Hence the  $L_P$  is set as large as possible within the limitation of core size. In this design, we choose  $L_P=1.85mH$  with EFD20/N67 core type.



(3) Maximum primary peak current *I*<sub>peak\_max</sub>, primary RMS current through MOSFET *I*<sub>PRMS\_max</sub> and secondary RMS current through rectifier diode *I*<sub>SRMS max</sub>

from Eq. (2), (3) and (4):

$$I_{peak\_max} = \frac{P_{in}}{V_{imin}D} + \frac{1}{2}\Delta I_L = \frac{P_{out}}{\eta V_{imin}D} + \frac{1}{2}\frac{N_{ratio}V_O(1-D)}{L_P f_S} = 0.589A$$
(12)

$$I_{PRMS_max} = \sqrt{\frac{1}{T_s} \int_0^{T_s} i_p^{-2}(t) dt} = \sqrt{\frac{D}{3} (3(\frac{P_{out}}{\eta V_{imin}D})^2 + \frac{\Delta I_L^2}{4})} = 0.32A$$
(13)

$$I_{SRMS_max} = \sqrt{\frac{1}{T_s} \int_0^{T_s} i_s^{2}(t) dt} = \sqrt{\frac{1 - D}{3} (3(\frac{I_o}{1 - D})^2 + \frac{(\Delta I_L * N_{ratio})^2}{4})} = 2.29A$$
(14)

(4) Primary and secondary turn numbers,  $N_P$  and  $N_S$ 

To prevent the saturation of the transformer, the  $N_P$  should be:

$$N_P \ge \frac{I_{peak\_max}L_P}{B_{max}A_{min}}$$
(15)

where,  $B_{max}$  is the maximum flux density of the core and  $A_{min}$  is the minimum magnetic cross section area of the core. In this case,  $A_{min}=31mm^2$  and we choose  $B_{max}=0.33T$ . And then,

$$N_P \ge \frac{I_{peak\_max}L_P}{B_{max}A_{min}} = 106.5 \tag{16}$$

we choose  $N_P=108$ . And

$$N_s = \frac{N_P}{N_{ratio}} = 14.3 \tag{17}$$

we choose  $N_{\rm S}$ =14.

## Voltage regulation loop design

#### (1) Power stage transfer function

For current mode control flyback converter in continuous conduction mode operation, its transfer function of output voltage  $v_o$  to control voltage  $v_{FB}$  is shown as follow.



$$G_{S}(S) = \frac{v_{O}(S)}{v_{FB}(S)} = \frac{KN_{ratio}R(1-D)}{1+D} \cdot \frac{(1+SCR_{C})(1-\frac{SL_{P}D}{N_{ratio}^{2}R(1-D)^{2}})}{1+\frac{SCR}{1+D}}$$
(18)

where, *K* is the gain of  $i_L(S)$  to  $v_{FB}(S)$ , *R* is the load resistance, *C* is output capacitance and  $R_C$  is the parasitic ESR of output capacitor. According to TDA16822 datasheet, *K* could be calculated as follow.

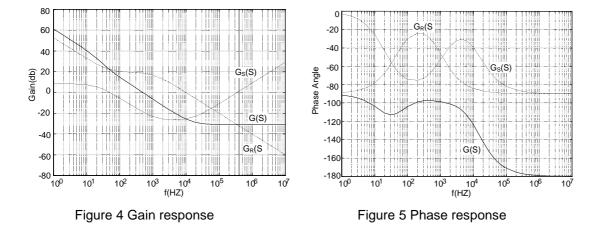
$$K = \frac{i_L(S)}{v_{FB}(S)} = \frac{1}{R_{sense}A_V}$$
(19)

where,  $R_{sense}$  is the primary current sense resistance and  $A_V$  is the gain of PWM operating amplifier.

It can be seen a right half plane (RHP) zero exists in  $G_{\rm S}(S)$ . The RHP zero provides additional phase lag while boosting gain. It is also a moving zero varied with *D*. Hence, large bandwidth  $\omega_{\rm C}$  is not normally obtainable with CCM operation in flyback converter. In the application,

 $R_{sense}$ =1.5 $\Omega$  $A_V$ =3.65 from TDA16822 datasheet R=8.8/1.7=5.2 $\Omega$ C=2200 $\mu$ F  $R_C$ =0.06 $\Omega$ 

The gain and phase response characteristics of  $G_{S}(S)$  are shown in Figure 4 and 5.





#### (2) Feedback loop design

The feedback loop circuit is shown in Figure 6. It consists of compensation network (*TL431*,  $R_1$ ,  $R_2$ ,  $R_3$ ,  $R_4$ ,  $C_1$  and  $C_2$ ) and optocoupler.

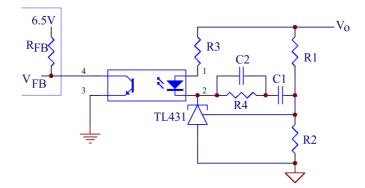


Figure 6 Feedback loop circuitry

The total transfer function  $\frac{v_{FB}(S)}{v_{O}(S)}$  of the feedback loop is

$$G_{R}(S) = \frac{v_{FB}(S)}{v_{O}(S)} = \frac{G_{C}R_{FB}}{R_{3}} \cdot \frac{1 + S(C_{1} + C_{2})R_{4}}{SC_{1}R_{1}(1 + SC_{2}R_{4})}$$
(20)

where,  $G_C$  is the current transfer ratio of the optocoupler.

In this design,

 $G_{c}$ =100% (optocoupler: SFH617-3)  $R_{FB}$ =3.7K $\Omega$  (from TDA16822 datasheet)  $R_{1}$ =6.2K $\Omega$   $R_{2}$ =2.4K $\Omega$   $R_{3}$ =1K $\Omega$   $R_{4}$ =15K $\Omega$   $C_{1}$ =0.22 $\mu$ F  $C_{2}$ =10nF

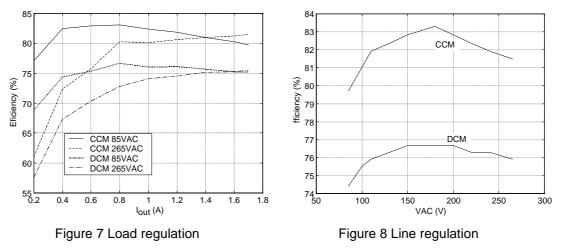
The gain and phase response characteristics of  $G_R(S)$  and final  $G(S)=G_S(S)+G_R(S)$  are shown in Figure 4 and 5. The cross frequency is around *500Hz* and the phase margin is about 82°.



## Experimental test

Based on the same output specification (8.8V/1.7A), two SMPS boards, operating in CCM and DCM respectively, are set up with TDA16822 implementation. The main differences of the two boards are the transformer design and current sense resistor. For DCM design, the primary inductance is  $409\mu$ H and sense resistor is  $1\Omega$ . For CCM design, the primary inductance is  $1850\mu$ H and sense resistor is  $1.5\Omega$ . The testing is done for both of the two boards and the performances are demonstrated for the comparison.

Load efficiency (Figure 7): The graph shows the efficiency changes with load current at 85VAC and 265VAC inputs. It can be seen that the efficiency of CCM board is generally *5%* higher than that of DCM board.



Line efficiency (Figure 8): This graph shows the efficiency changes with AC input voltage at full load current. Again, *5%* improvement on efficiency is obtained from CCM operation.

Standby /No load power dissipation (Figure 9): This figure shows the power loss at standby/no-load condition. There is not much difference on the standby input power for CCM and DCM operation. Both of them are below *1W*.

Overload protection threshold (Figure 10): This figure shows the overload protection threshold, i.e. maximum output power set by the circuit. It can be seen, for DCM board, the maximum output power is almost a constant value and not dependent on the input voltage. However, for CCM board, the threshold value increases with the increasing of the line voltage. From *16W* at 85VAC to *21.6W* at 265VAC, it corresponds to *35%* overshoot. This phenomenon has be predicted by the mathematical derivation in Eq(7).



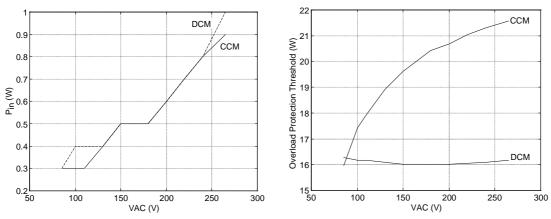


Figure 9 Standby /No load power dissipation

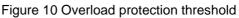


Figure 11 shows the test waveform at full load, 220VAC input for DCM board. Figure 12 shows the test waveform at full load, 220VAC input for CCM board. It can be seen that the primary turn on current does not start from zero and the shape of the current waveform is trapezoid in CCM, instead of triangular in DCM. And the peak current is

$$I_{peak} = 0.8/1.5 = 0.53A$$

it is lower than that in DCM board which is

$$I_{peak} = 0.9/1 = 0.9A$$

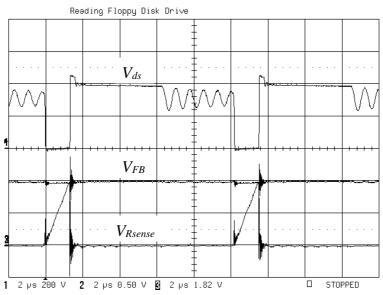


Figure 11 test waveforms at full load, 220VAC input for DCM board. Channel 1:  $V_{ds}$ , 200V/div, Channel 2:  $V_{Rsense}$ , 0.5V/div, Channel 3:  $V_{FB}$ , 1.82V/div, time: 2µs/div.



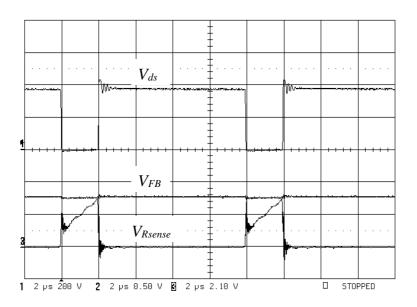


Figure 12 test waveforms at full load, 220VAC input for DCM board. Channel 1:  $V_{ds}$ , 200V/div, Channel 2:  $V_{Rsense}$ , 0.5V/div, Channel 3:  $V_{FB}$ , 2.10V/div, time: 2µs/div.

Figure 13 and Figure 14 show the dynamic performance of DCM operation. Due to the large bandwidth  $\omega_{\rm C}$ =3*KHz*, SMPS response immediately and there is almost no DC ripple when the load is switched between no load and full load.

Figure 15 and Figure 16 show the dynamic performance of CCM operation. Compared to DCM board, CCM operation has high DC ripple when the load is switched between no load and full load. From no load to full load, the response time is around 10ms and the transient voltage drop is 0.2V. From full load to no load, the response time is about 40ms and the transient voltage overshoot is 0.12V. This is because of the narrow bandwidth  $\omega_{c}$ =500Hz which leads to the slow response for the load regulation. Hence the output voltage suppressor is normally required in CCM operation to prevent the voltage overshoot when the load is suddenly cut off.



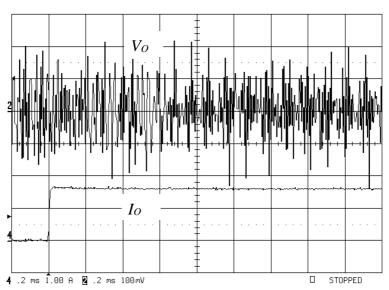


Figure 13 test waveforms for DCM board when the load is switched from no load to full load (1.7A), test condition: 220VAC input. Channel 2:  $V_0$ , 0.1V/div, Channel 4:  $I_0$ , 1A/div, time: 0.2ms/div.

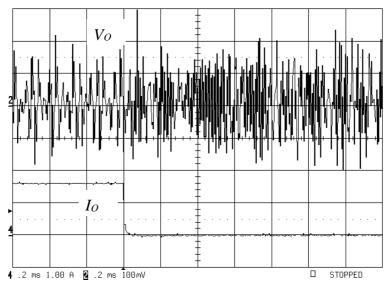


Figure 14 test waveforms for DCM board when the load is switched from full load (1.7A) to no load, test condition: 220VAC input. Channel 2:  $V_{O}$ , 0.1V/div, Channel 4:  $I_{O}$ , 1A/div, time: 0.2ms/div.



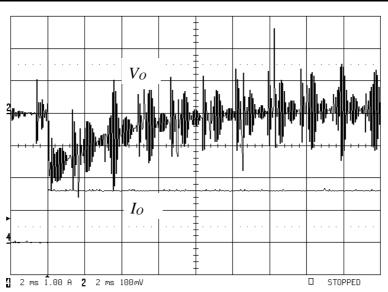


Figure 15 test waveforms for CCM board when the load is switched from no load to full load (1.7A), test condition: 220VAC input. Channel 2:  $V_0$ , 0.1V/div, Channel 4:  $I_0$ , 1A/div, time: 2ms/div.

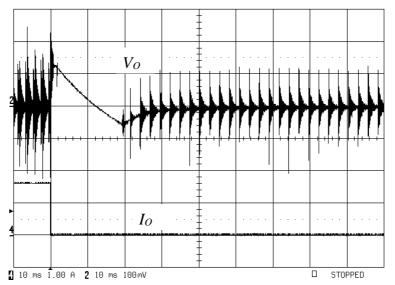


Figure 16 test waveforms for CCM board when the load is switched from full load (1.7A) to no load, test condition: 220VAC input. Channel 2:  $V_0$ , 0.1V/div, Channel 4:  $I_0$ , 1A/div, time: 10ms/div.



## Conclusion

The benefit and drawback of the CCM operation for flyback converter are analyzed in detail in this paper. Experiments are done and the steady state and dynamic performances are demonstrated for both of DCM and CCM operation. DCM is much popular for SMPS design because of its simple transfer function characteristic and good line and load regulation. Most importantly the maximum output power can be set at a constant value and no power overshoot during fault. However, CCM can provide the higher efficiency which is required by more and more applications. In CCM operation, both of the peak current and RMS current are lower than that of DCM operation. Although its overload protection threshold varies with the input voltage, CCM operation is still attractive for the applications with high efficiency requirement.

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