PIN diodes in RF switch applications

About this document

Scope and purpose

This application note shows radio frequency (RF) switches for signal routing between different transmission paths with Infineon PIN diodes. The single-pole single-throw (SPST) and single-pole double-throw (SPDT) based switch structures are outlined. Various Infineon PIN diodes are used, namely BAR50-02V, BAR63-02L, BAR64-02V and BAR90-02EL.

Intended audience

This document is intended for engineers who need to design RF PIN diode switches.

Table of contents

1 Introduction

1.1 RF switches

Many applications require switching the RF signal path to route and connect to different antennas, filters and amplifiers. With the growth and development of wireless communication, high-speed data networks and other advanced technologies such as switchable band-pass filters, the need for high performance switching devices is increasing.

The PIN diode is one of the popular device options for switches. The PIN diode comprises three regions, namely the P-region (p-type semiconductor), I-region (intrinsic semiconductor) and N-region (n-type semiconductor). The wide intrinsic region in the PIN diode makes it suitable for fast switches, attenuators and high voltage power applications.

The two most common configurations of RF switches are shown in the following figures. The SPST switch has one input port and one output port, as shown in Figure 1. The SPST is a basic switch, which is used to connect or break the connection between the two terminals. It can be utilized to connect RF input to RF output by providing a positive bias voltage to the diode.

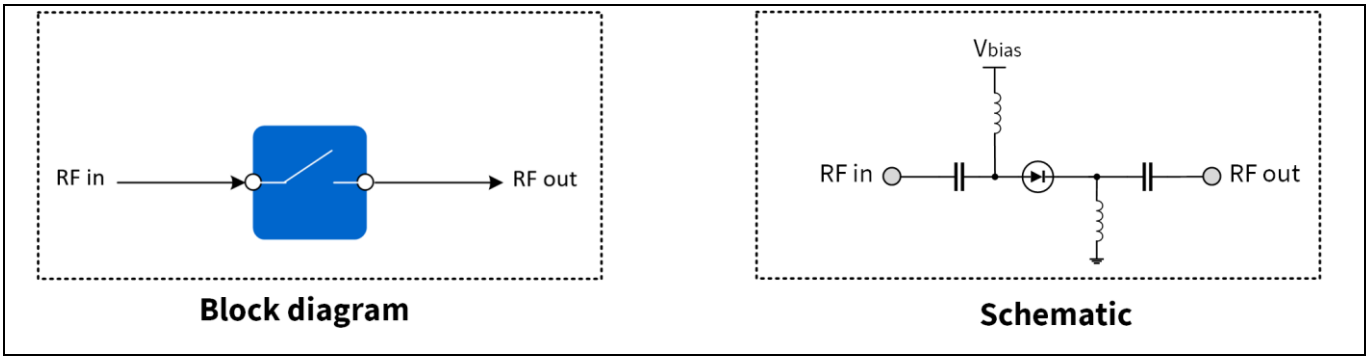

Figure 1 The SPST switch configuration

The SPDT switch has one common port and two output branches, as shown in Figure 2. The SPDT is ideal for use in Rx-Tx (receive–transmit) antenna switches. The SPDT schematic shown in Figure 2 contains one series diode in each branch of the switch. By providing positive bias voltage to the respective diode, the RF signal is routed from the common input port to either one of the two output branches.

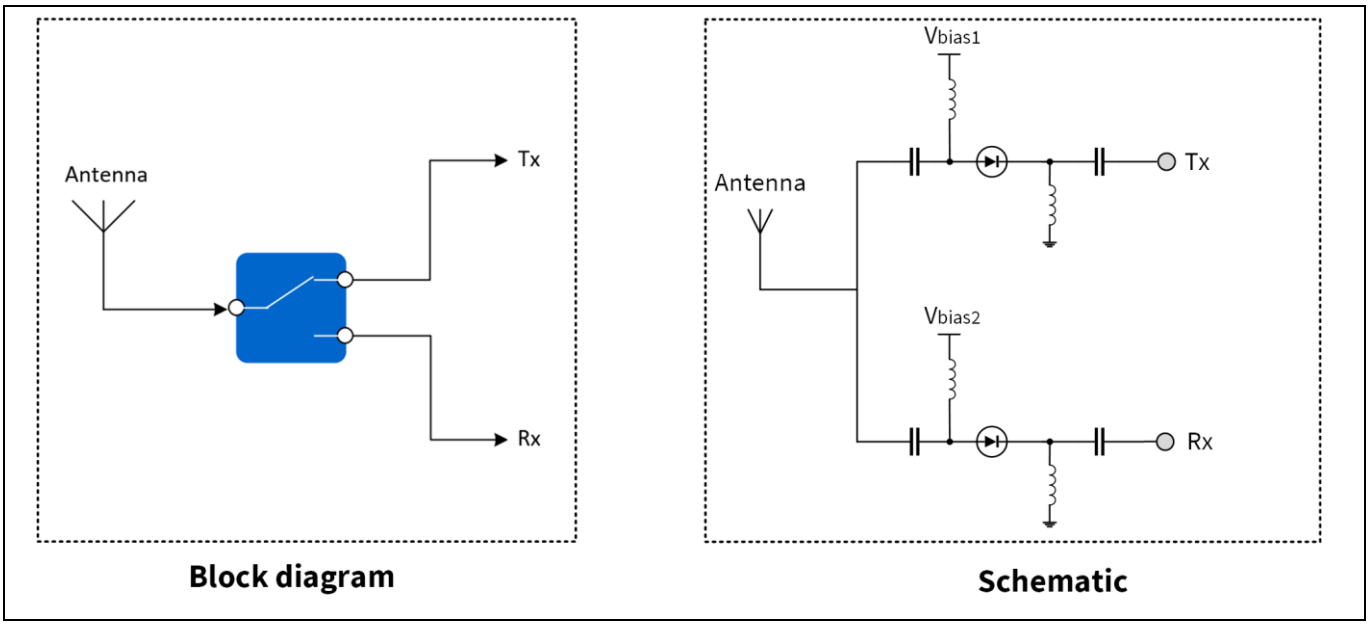

Figure 2 The SPDT series switch configuration

Adding a shunt PIN diode in each switching branch improves the isolation provided by the switch. Figure 3 shows the schematic of the SPDT series and shunt switch.

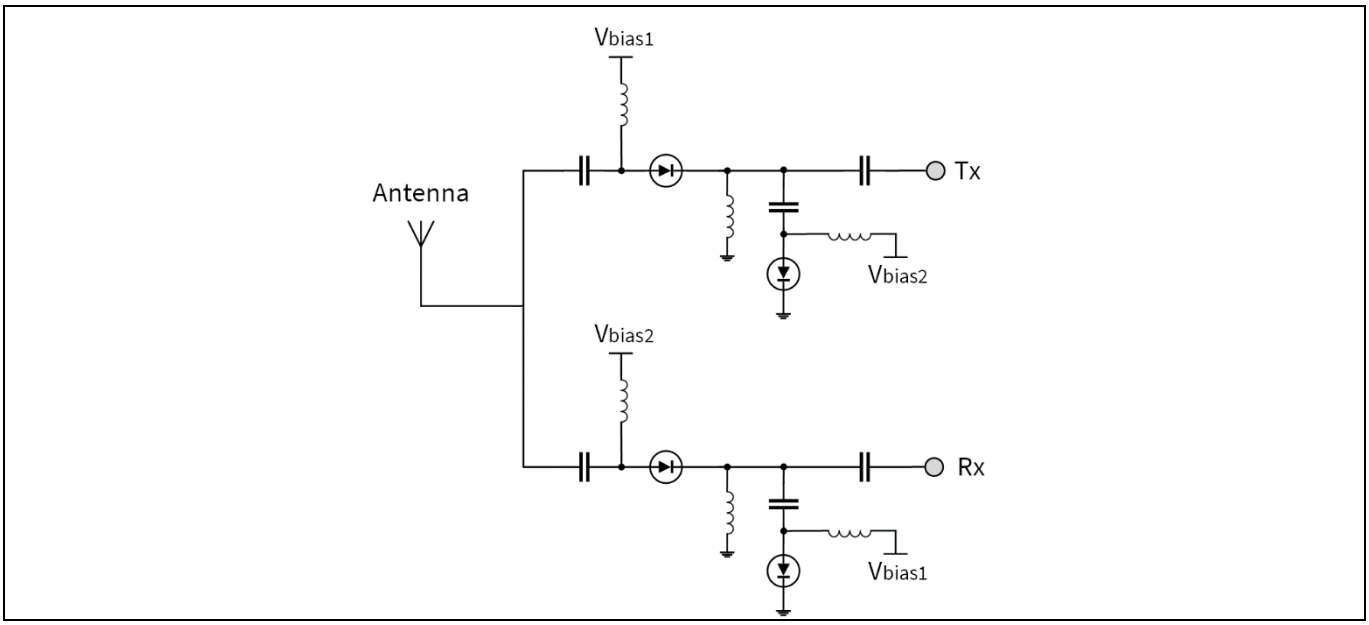

Figure 3 The SPDT series and shunt switch schematic

1.2 Infineon PIN diodes

Infineon PIN diodes are ideal for a wide range of RF applications. Their low insertion loss and fast switching time makes them ideal for use in Rx-Tx antenna switches. They are offered in industry-standard 0201 and 0402 form factors as well as conventional industry packages and various junction diode configurations.

Key parameters of PIN diodes used in this application note are listed in Table 1.

Table 1 PIN diodes – key parameters

Product type	C_T at 0 V, f = 1.8 GHz [pF]	R_f at 10 mA [Ω]	τ_{rr} [ns]	Package
BAR50-02V	0.15	3.0	1100	SC79
BAR63-02L	0.3	1.0	75	TSLP-2
BAR64-02V	0.17	2.1	1550	SC79
BAR90-02EL	0.18	0.8	750	TSLP-2

2 PIN diode SPST switches

2.1 Sub-GHz range

2.1.1 Performance overview

The following table shows the SPST switch performance with PIN diode BAR63-02L.

Table 2 Summary of measurement results of SPST switch circuit

Parameter	Symbol	Value	Unit	Notes
Device		BAR63-02L		
Bias voltage	V_{bias}	3.3	V	On state
Bias current	I_{bias}	9.8	mA	On state
Frequency	f	300 to 1000	MHz	
Insertion loss (on state)	IL	0.24[1)] 0.20[2)] 0.19[3)]	dB	SMA and PCB losses subtracted 1) Measured at 315 MHz (losses = 0.04 dB) 2) Measured at 434 MHz (losses = 0.04 dB) 3) Measured at 868 MHz (losses = 0.09 dB)
Input return loss	RL_{in}	>25	dB	
Output return loss	RL_{out}	>24.8	dB	
Isolation (off state)	ISO_{off}	24.4[4)] 22.3[5)] 16.9[6)]	dB	Off state (I_{bias} = 0 A) 4) Measured at 315 MHz 5) Measured at 434 MHz 6) Measured at 868 MHz
Input third order intercept point	IIP_3	> 45	dBm	Measured at P_{IN} = 5 dBm
Third order intermodulation distortion	IMD3	> 85	dBc	

2.1.2 Schematic

The following figure shows the schematic of the SPST switch. In the schematic, the resistor R1 is used to set the bias current. The inductor L2 provides the DC return path for the bias current. The capacitor C2 serves as the RF bypass. The input matching is achieved by the capacitor C1 and the inductor L1. The output matching network is formed by the capacitor C3 and the inductor L2.

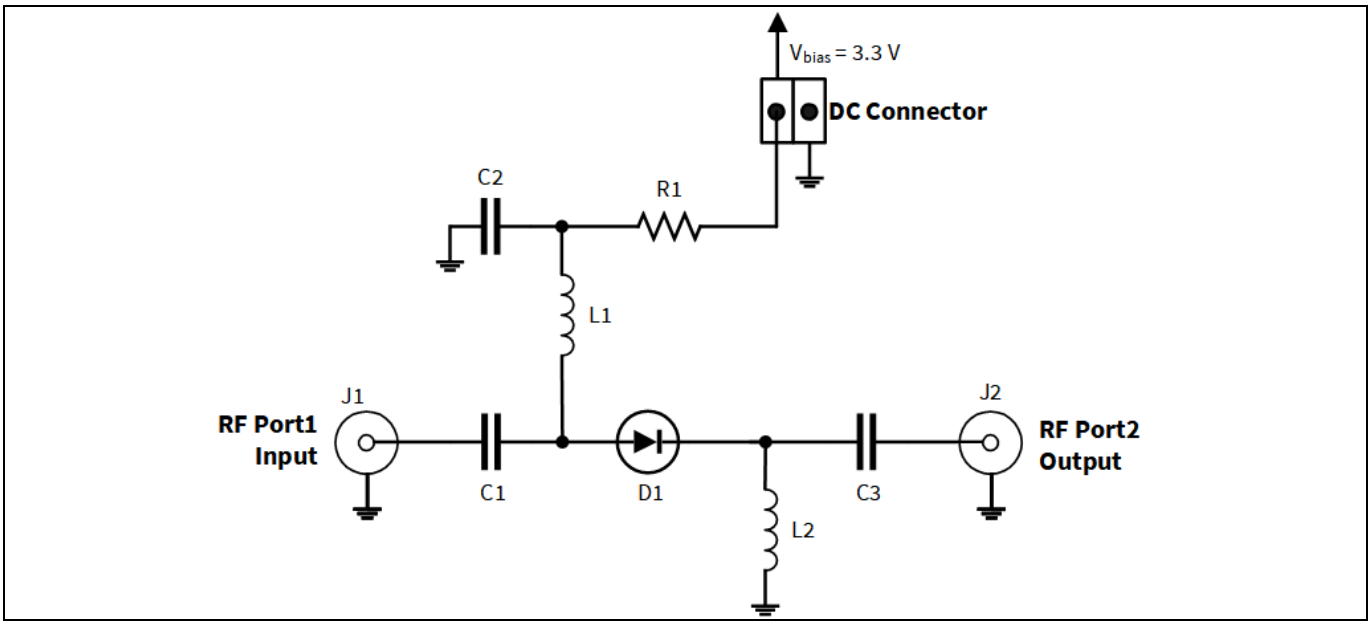

Figure 4 The SPST switch schematic

2.1.3 Bill of materials (BOM)

Table 3 BOM of the SPST switch circuit with BAR63-02L

Symbol	Value	Unit	Size	Manufacturer	Comment
D1	BAR63-02L	–	TSLP-2	Infineon	PIN diode
C1	22	pF	0402	Various	DC block and input matching
C2	220	nF	0402	Various	RF bypass
C3	22	pF	0402	Various	DC block and output matching
L1	68	nH	0402	Murata LQW	RF choke
L2	68	nH	0402	Murata LQW	DC return
R1	240	Ω	0402	Various	DC bias

2.1.4 Evaluation board and layout information

The evaluation board information for the SPST switch circuit with BAR63-02L:

- PCB material: FR4
- PCB marking: M180629 RF Diode 3

Images of the evaluation board and the PCB stack information are shown in the following figures.

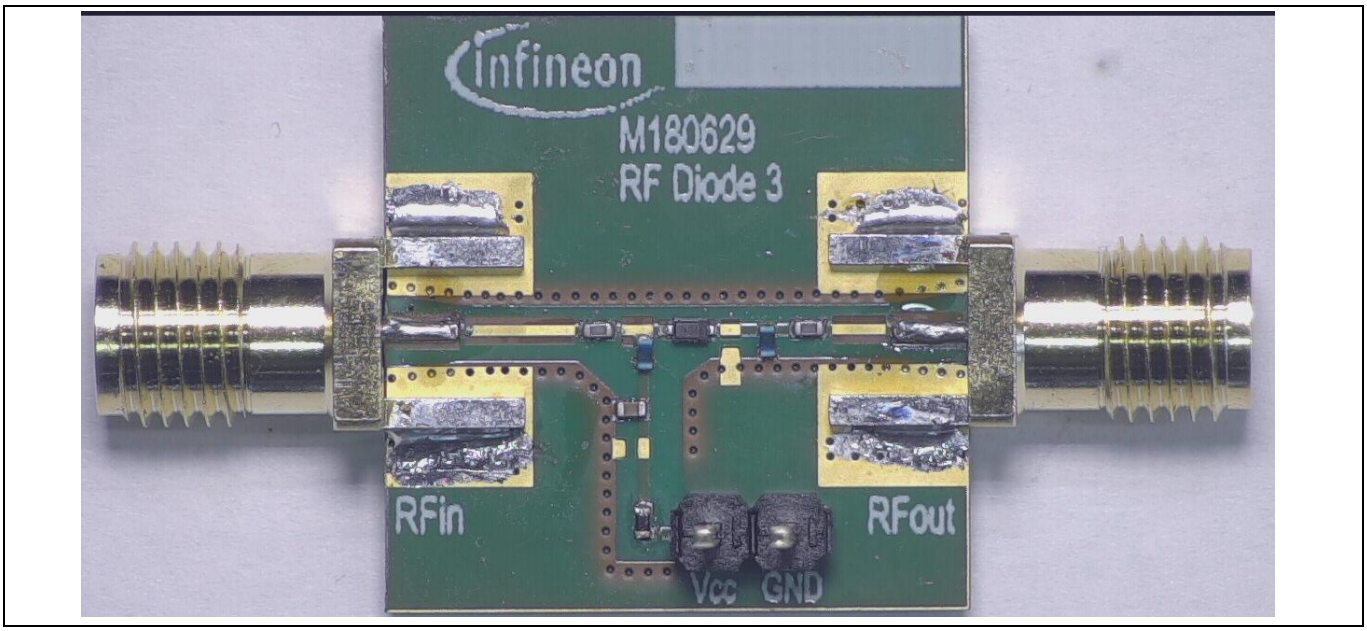

Figure 5 Photo of the evaluation board for PIN diode SPST switch with BAR63-02L

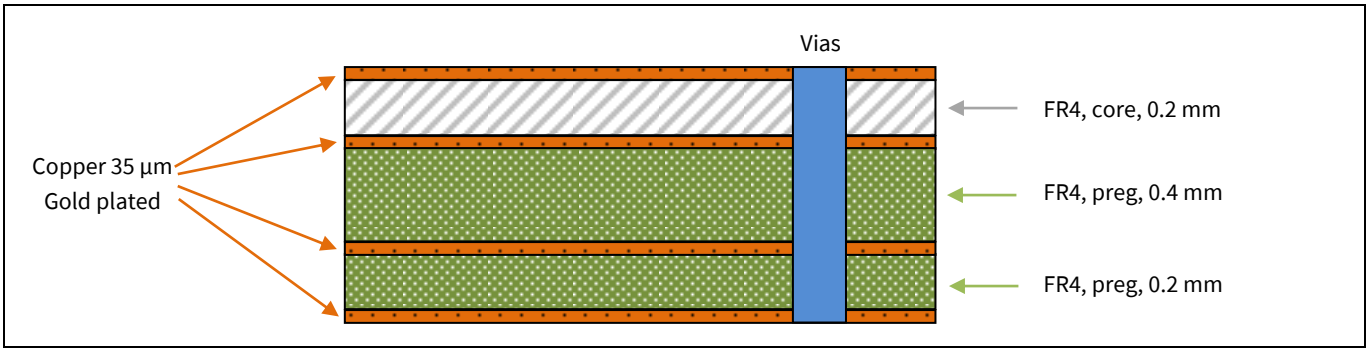

Figure 6 PCB stack information of the evaluation board for PIN diode SPST switch

2.1.5 Measurement graphs

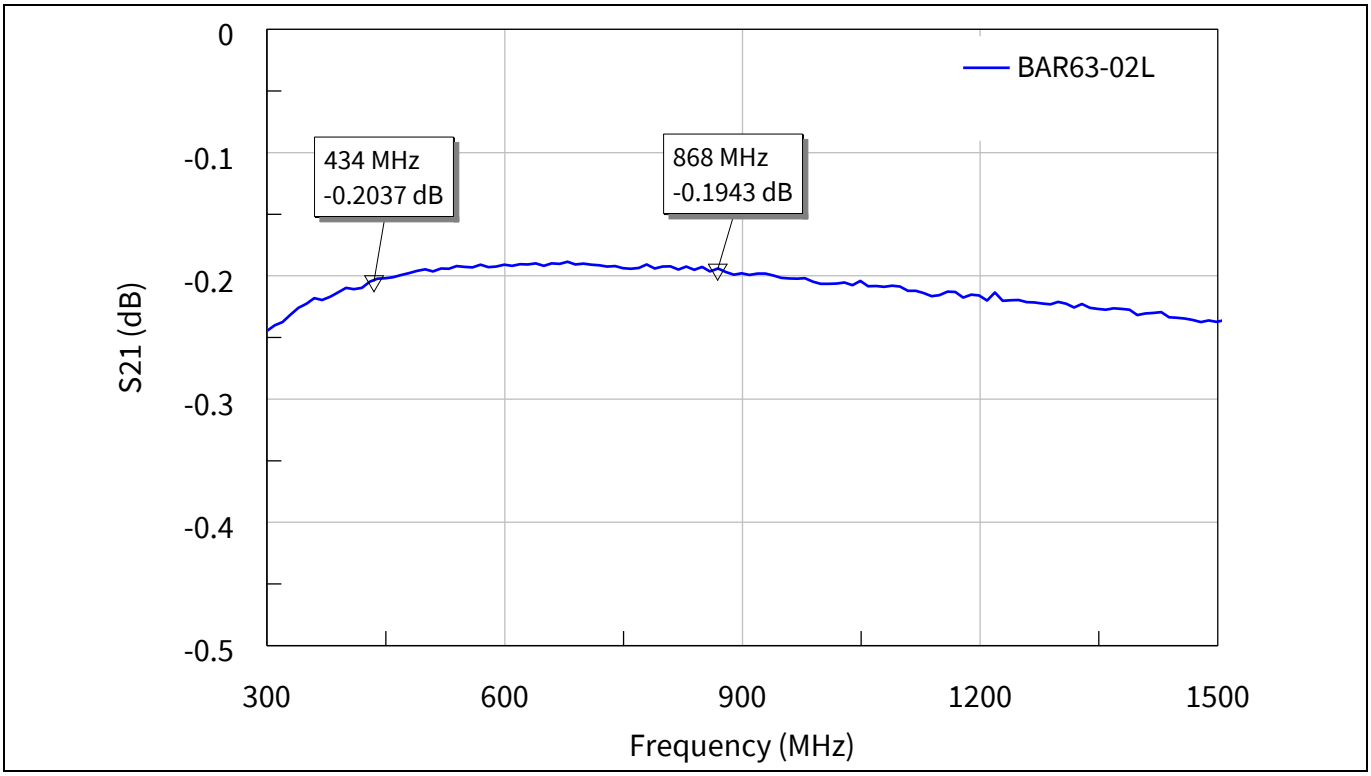

Figure 7 Insertion loss of PIN diode SPST switch with BAR63-02L in on state (I_{bias} = 9.8 mA)

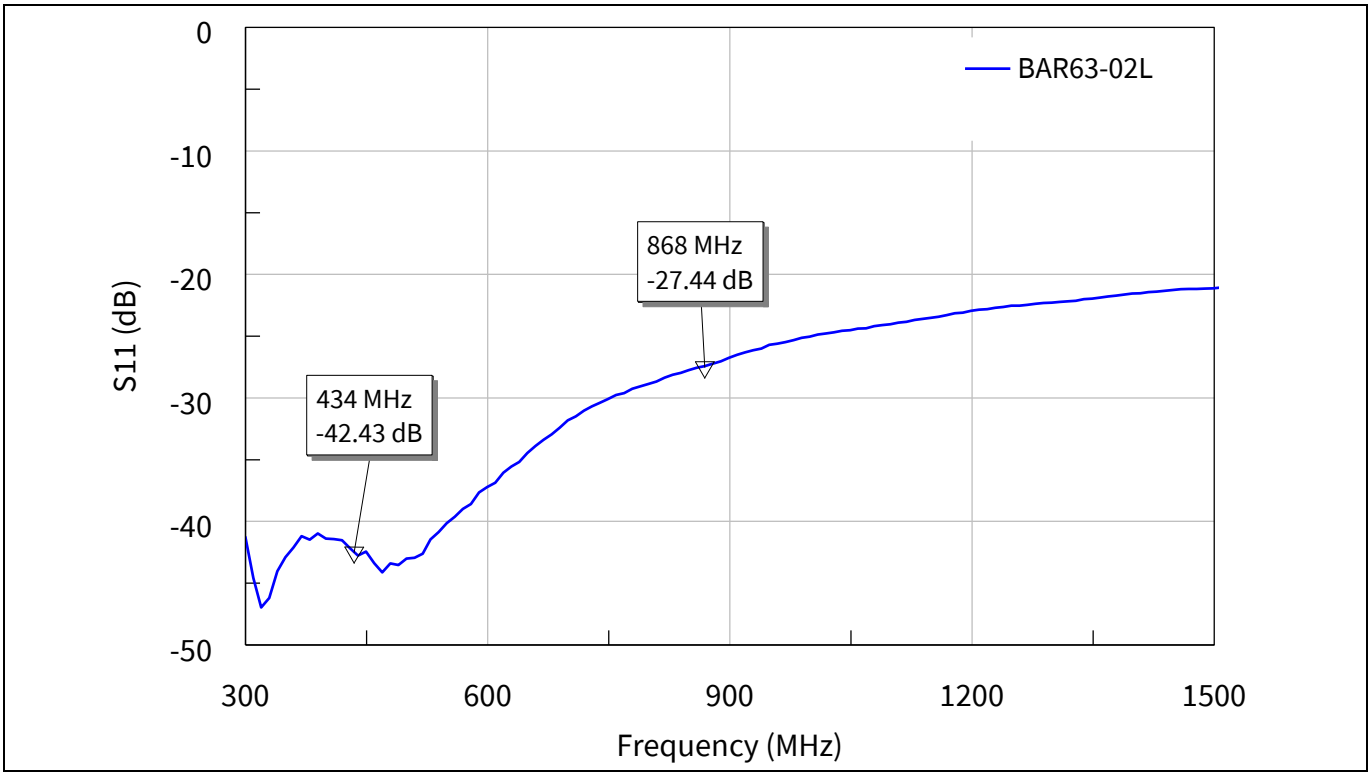

Figure 8 Input return loss of PIN diode SPST switch with BAR63-02L in on state (I_{bias} = 9.8 mA)

Note: The graphs are generated with the AWR electronic design automation (EDA) software Microwave Office®.

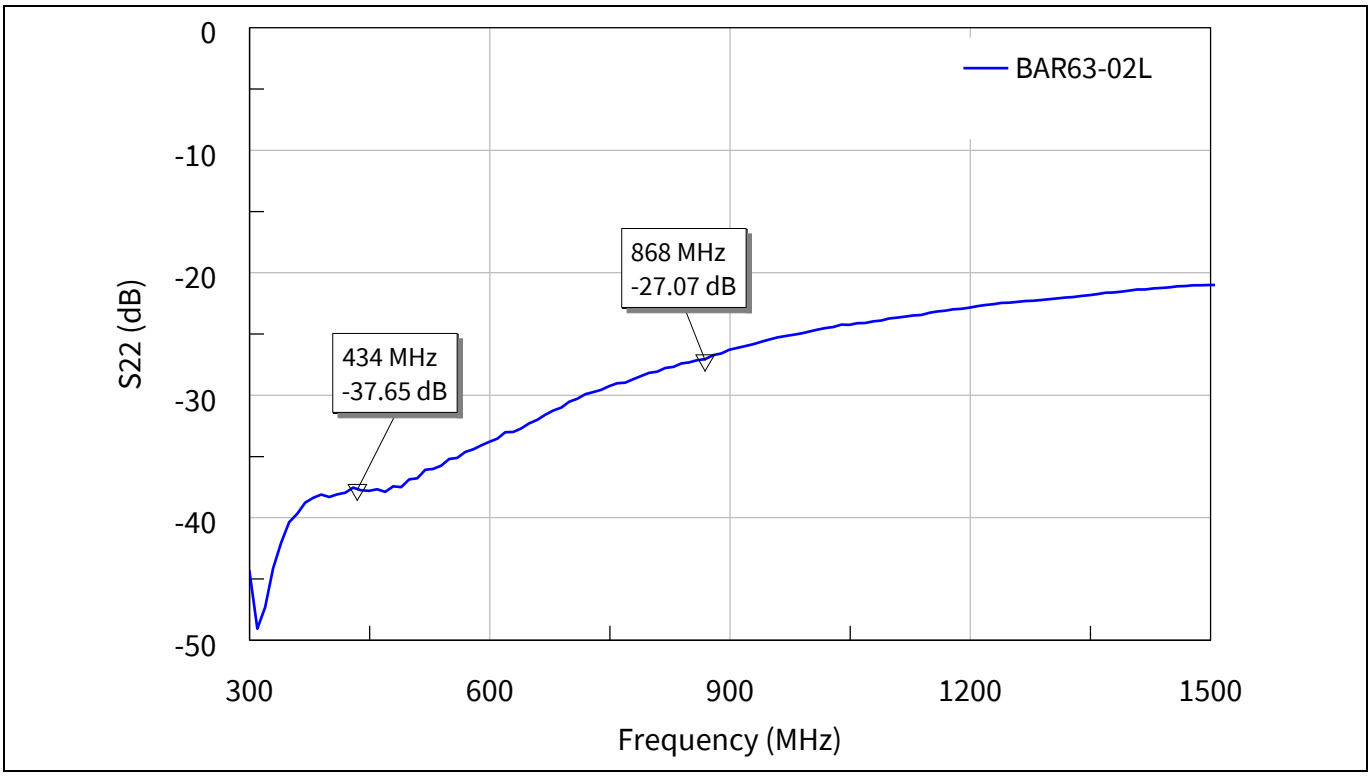

Figure 9 Output return loss of PIN diode SPST switch with BAR63-02L in on state (I_{bias} = 9.8 mA)

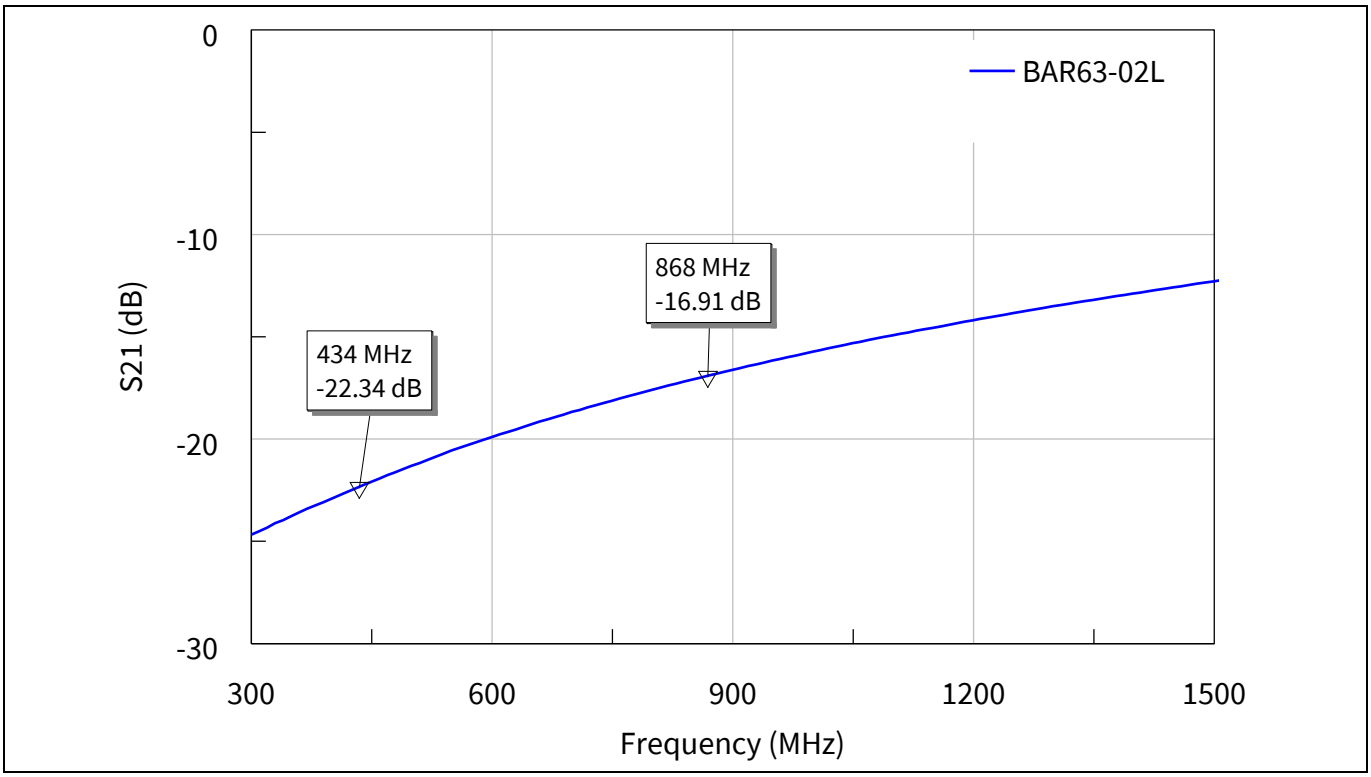

Figure 10 Isolation of PIN diode SPST switch with BAR63-02L in off state (I_{bias} = 0 A)

2.2 S-band range

2.2.1 Performance overview

The following table shows the SPST switch circuit performance with PIN diodes BAR50-02V, BAR64-02V and BAR90-02EL.

Table 4 Summary of measurement results of the SPST switch circuits

Parameter	Symbol	Value			Unit	Notes
Device		BAR50-02V	BAR64-02V	BAR90-02EL		
Bias voltage	V_{bias}	3.3	3.3	3.3	V	On state
Bias current	I_{bias}	10	10.1	10	mA	On state
Frequency	f	1.5 to 3.7	1.5 to 3.7	1.5 to 3.7	GHz	
Insertion loss (on state)	IL	0.33[1)] 0.35[2)] 0.39[3)]	0.29[1)] 0.30[2)] 0.37[3)]	0.21[1)] 0.22[2)] 0.27[3)]	dB	SMA and PCB losses subtracted 1) Measured at 1.9 GHz (losses = 0.21 dB) 2) Measured at 2.4 GHz (losses = 0.27 dB) 3) Measured at 3.5 GHz (losses = 0.39 dB)
Input return loss	RL_{in}	>29	>20	>20	dB	
Output return loss	RL_{out}	>28	>19	>19.5	dB	
Isolation (off state)	ISO_{off}	16.8[4)] 14.8[5)] 11.9[6)]	15.6[4)] 13.8[5)] 10.5[6)]	13.9[4)] 12.1[5)] 9.1[6)]	dB	Off state (I_{bias} = 0 A) 4) Measured at 1.9 GHz 5) Measured at 2.4 GHz 6) Measured at 3.5 GHz
Input third order intercept point	IIP_3	> 45	> 45	> 45	dBm	Measured at P_{IN} = 5 dBm
Third order intermodulation distortion	IMD3	> 85	> 85	> 85	dBc	

2.2.2 Schematic

The following figure shows the schematic of the SPST switch. In the schematic, the resistor R1 is used to set the bias current. The inductor L2 provides the DC return path for the bias current. The capacitor C2 serves as the RF bypass. The input matching is achieved by the capacitor C1 and the inductor L1. The output matching network is formed by the capacitor C3 and the inductor L2.

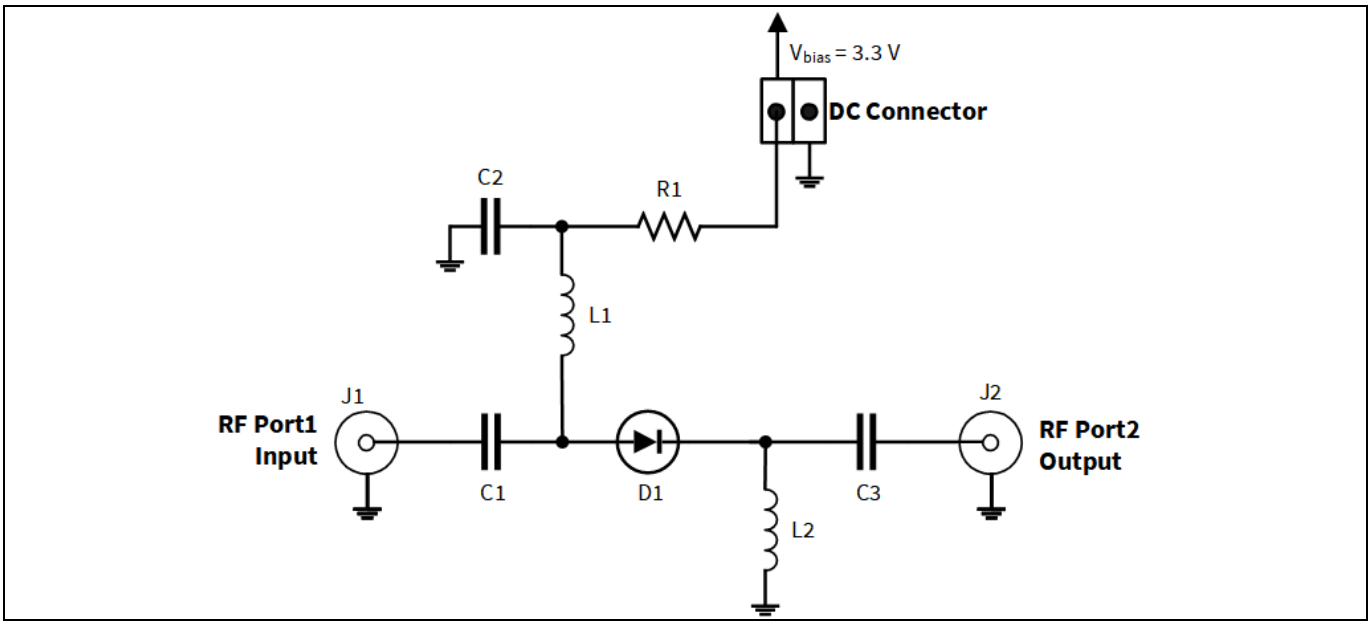

Figure 11 The SPST switch schematic

2.2.3 BOM

Table 5 BOM of the SPST switch circuits with BAR50-02V, BAR64-02V and BAR90-02EL

Symbol	Value			Unit	Size	Manufacturer	Comment
D1	BAR50-02V (TSLP-2)	BAR64-02V (SC79)	BAR90-02EL (TSLP-2)	–	–	Infineon	PIN diode
C1	12	8.2	8.2	pF	0402	Various	DC block and input matching
C2	220	220	220	nF	0402	Various	RF bypass
C3	12	8.2	8.2	pF	0402	Various	DC block and output matching
L1	68	68	68	nH	0402	Murata LQW	RF choke
L2	68	68	68	nH	0402	Murata LQW	DC return
R1	240	240	240	Ω	0402	Various	DC bias

2.2.4 Evaluation board and layout information

The evaluation board information for the SPST switch circuit with BAR50-02V, BAR64-02V and BAR90-02EL:

- PCB material: FR4
- PCB marking: M180629 RF Diode 3

Images of the evaluation board and the PCB stack information are shown in the following figures.

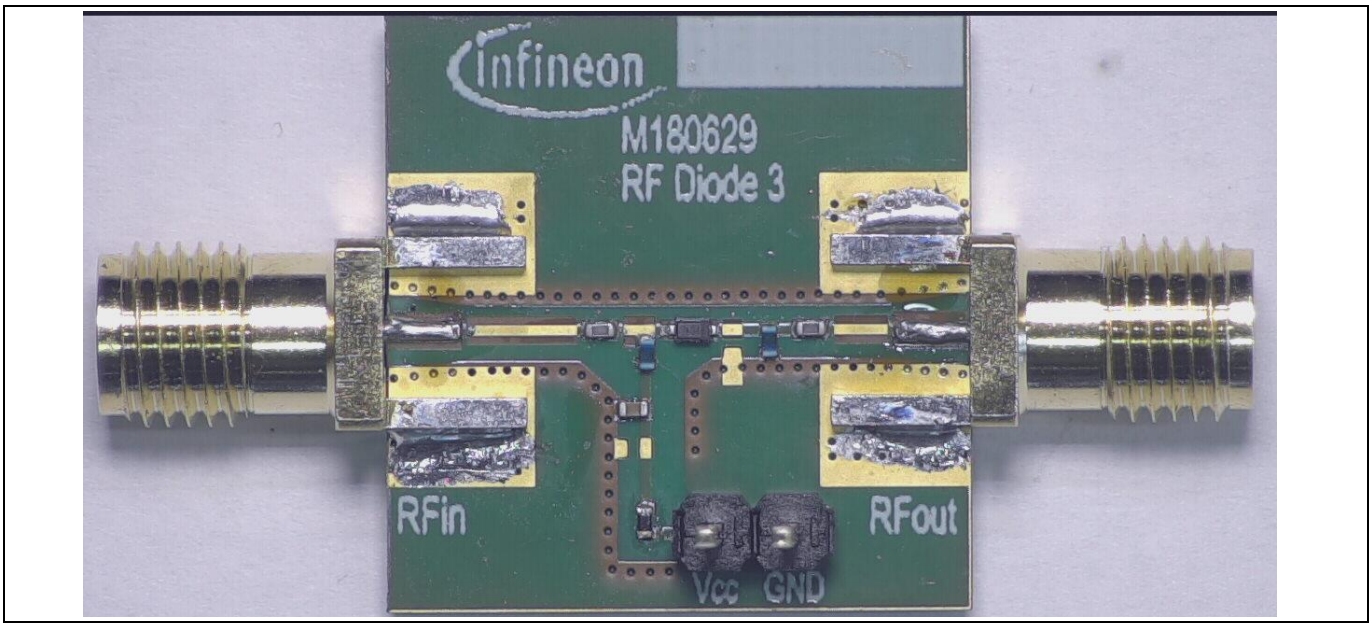

Figure 12 Photo of the evaluation board for PIN diode SPST switch with BAR50-02V, BAR64-02V and BAR90-02EL

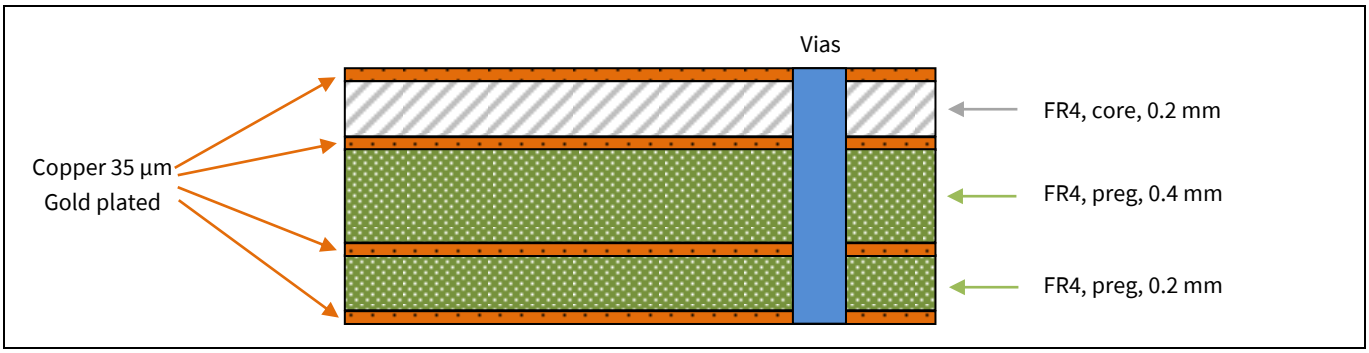

Figure 13 PCB stack information of the evaluation board for PIN diode SPST switch

2.2.5 Measurement graphs

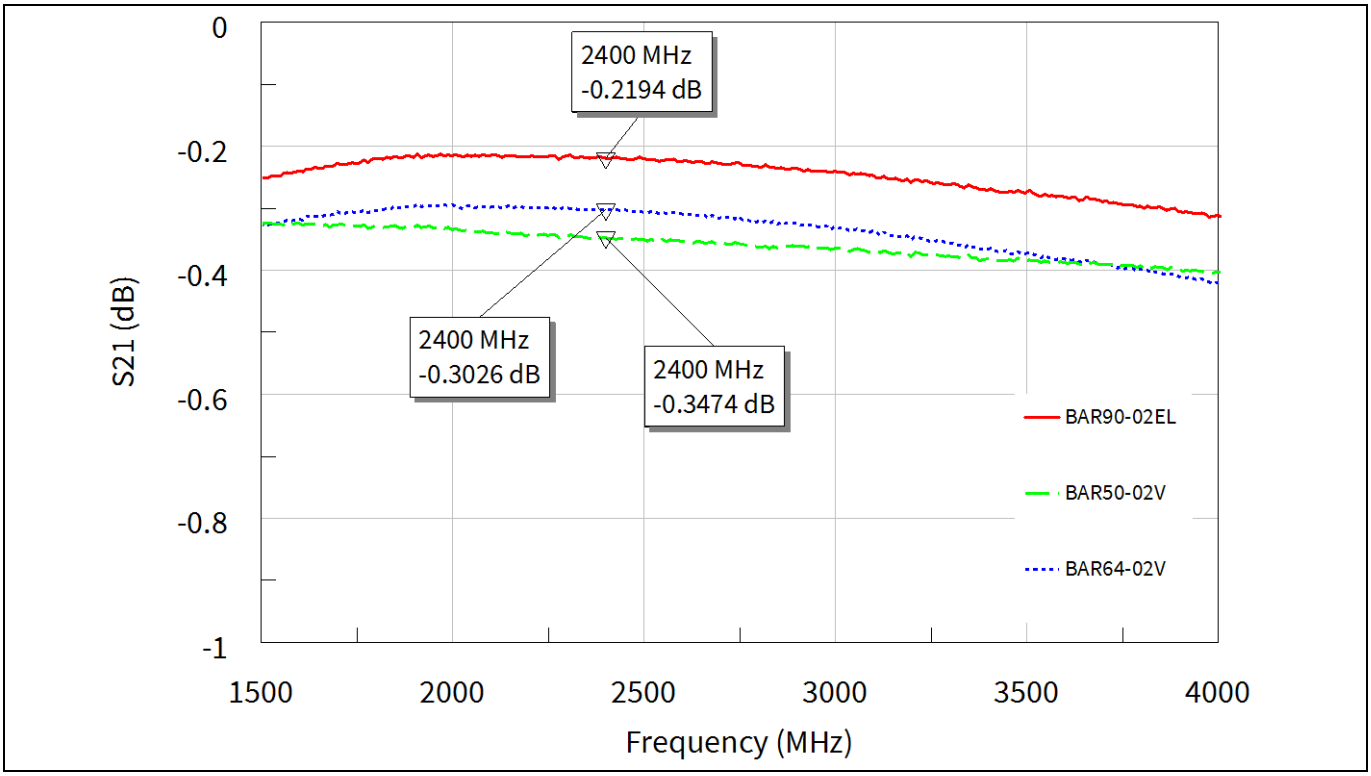

Figure 14 Insertion loss of PIN diode SPST switch with BAR50-02V, BAR64-02V and BAR90-02EL in on state (I_{bias} = 10 mA)

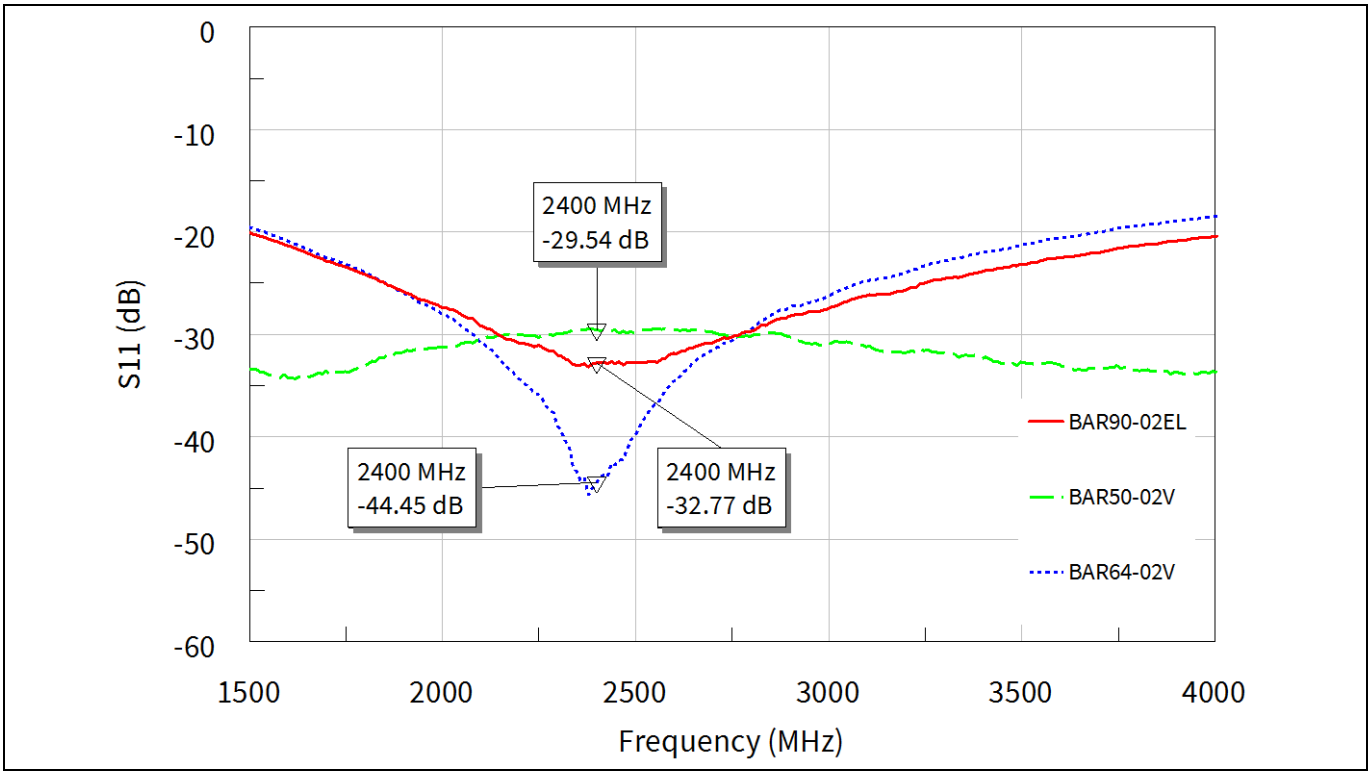

Figure 15 Input return loss of PIN diode SPST switch with BAR50-02V, BAR64-02V and BAR90-02EL in on state (I_{bias} = 10 mA)

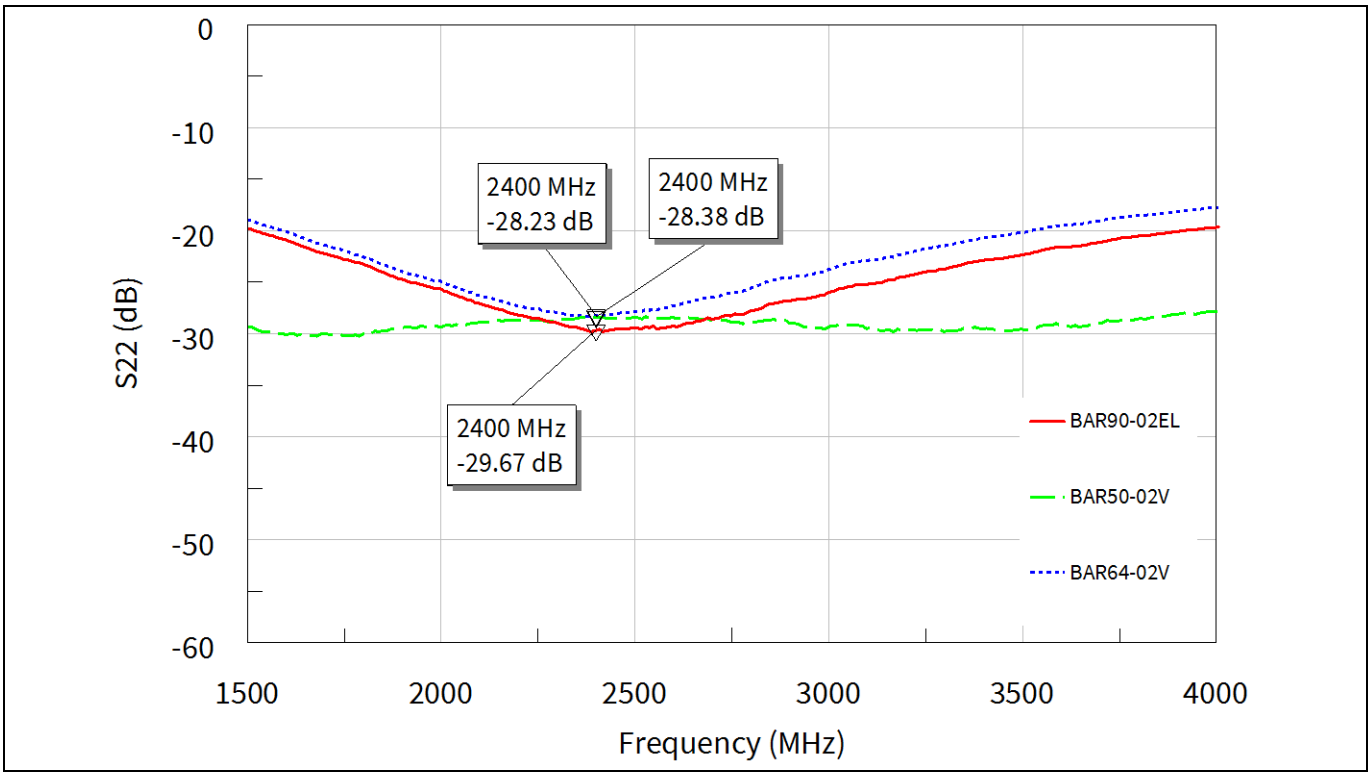

Figure 16 Output return loss of PIN diode SPST switch with BAR50-02V, BAR64-02V and BAR90-02EL in on state (I_{bias} = 10 mA)

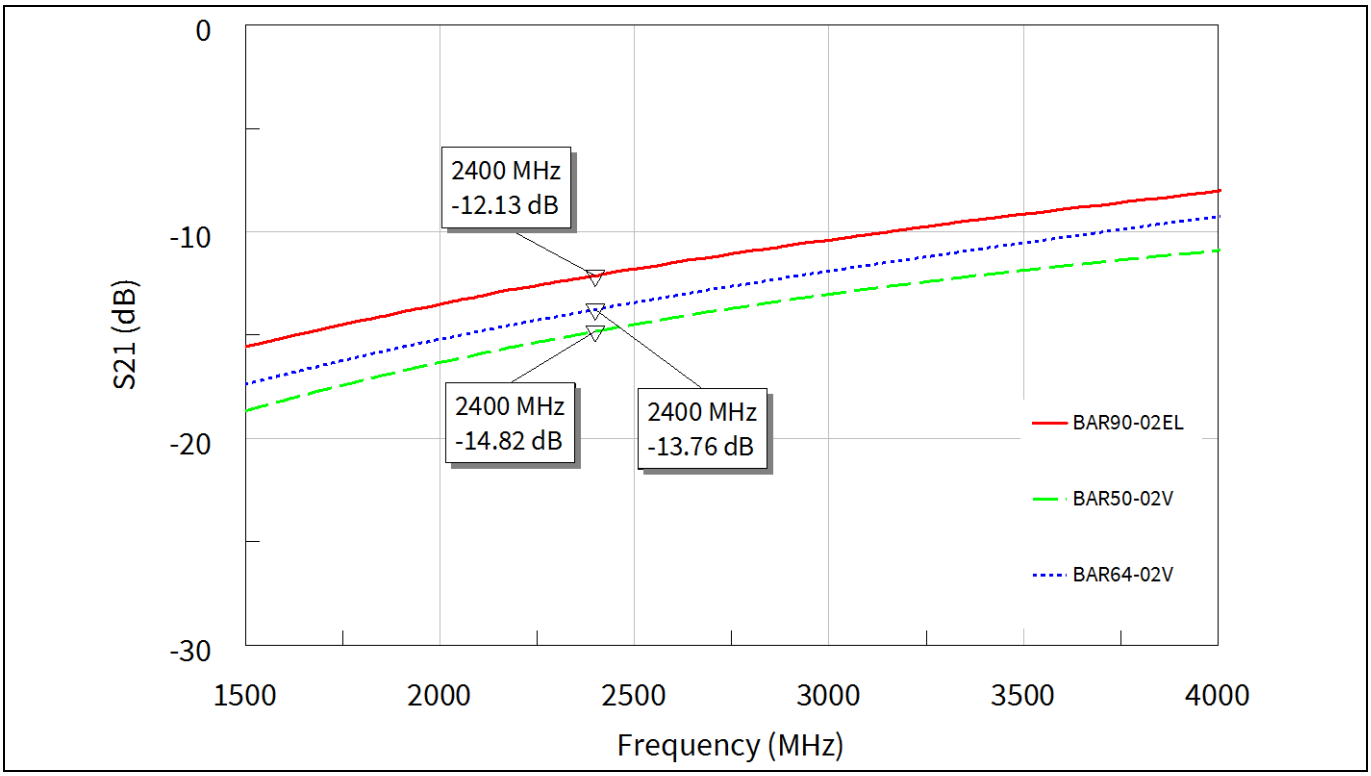

Figure 17 Isolation of PIN diode SPST switch with BAR50-02V, BAR64-02V and BAR90-02EL in off state (I_{bias} = 0 A)

3 PIN diode SPDT series switches

3.1 Sub-GHz range

3.1.1 Performance overview

The following tables show the SPDT series switch performance with PIN diode BAR63-02L.

Table 6 Summary of measurement results of the SPDT series switch circuit for ANT-Tx mode

Parameter	Symbol	Value	Unit	Notes
Device		BAR63-02L		
Bias voltage	V_{bias1}	3.3	V	Mode: ANT-Tx (V_{bias2} = 0 V)
Bias current	I_{bias1}	9.8	mA	Mode: ANT-Tx (I_{bias2} = 0 A)
Frequency	f	300 to 1000	MHz	
Input return loss	RL_{in}	>15.7	dB	
Output return loss	RL_{out}	>16.4	dB	
Insertion loss	IL	0.28[1)] 0.24[2)] 0.32[3)]	dB	SMA and PCB losses subtracted 1) Measured at 315 MHz (losses = 0.05 dB) 2) Measured at 434 MHz (losses = 0.06 dB) 3) Measured at 868 MHz (losses = 0.12 dB)
Isolation Tx-Rx	ISO_{Tx-Rx}	30.5[4)] 28.1[5)] 22.1[6)]	dB	4) Measured at 315 MHz 5) Measured at 434 MHz 6) Measured at 868 MHz
Isolation ANT-Rx	ISO_{ANT-Rx}	29.7[4)] 27.6[5)] 21.9[6)]	dB	
Input third order intercept point	IIP_3	>45	dBm	Measured at P_{IN} = 5 dBm
Third order intermodulation distortion	IMD3	>85	dBc	

Table 7 Summary of measurement results of the SPDT series switch circuit for ANT-Rx mode

Parameter	Symbol	Value	Unit	Notes
Device		BAR63-02L		
Bias voltage	V_{bias2}	3.3	V	Mode: ANT-Rx (V_{bias1} = 0 V)
Bias current	I_{bias2}	9.7	mA	Mode: ANT-Rx (I_{bias1} = 0 A)
Frequency	f	300 to 1000	MHz	
Input return loss	RL_{in}	>15.2	dB	
Output return loss	RL_{out}	>16.6	dB	
Insertion loss	IL	0.28[1)] 0.25[2)] 0.36[3)]	dB	SMA and PCB losses subtracted 1) Measured at 315 MHz (losses = 0.05 dB) 2) Measured at 434 MHz (losses = 0.06 dB) 3) Measured at 868 MHz (losses = 0.12 dB)
Isolation Tx-Rx	ISO_{Tx-Rx}	28.5[4)] 26.1[5)] 20.7[6)]	dB	4) Measured at 315 MHz 5) Measured at 434 MHz 6) Measured at 868 MHz
Isolation ANT-Tx	ISO_{ANT-Tx}	27.8[4)] 25.6[5)] 20.4[6)]	dB	
Input third order intercept point	IIP_3	>45	dBm	Measured at P_{IN} = 5 dBm
Third order intermodulation distortion	IMD3	>85	dBc	

3.1.2 Schematic

The following figure shows the schematic of the SPDT series switch. In the schematic, each branch of the switch contains one series connected PIN diode. The resistors R1 and R2 are used to set the bias current for each branch of the switch respectively. The inductors L1 and L4 provide the DC return path for the bias current. The capacitors C2 and C5 serve as the RF bypass. The capacitors C3 and C4 provide the DC block and the matching at the common input port. The matching network at the output port one is formed by the capacitor C1 and the inductor L1, and the matching network at output two is formed by the capacitor C6 and the inductor L4.

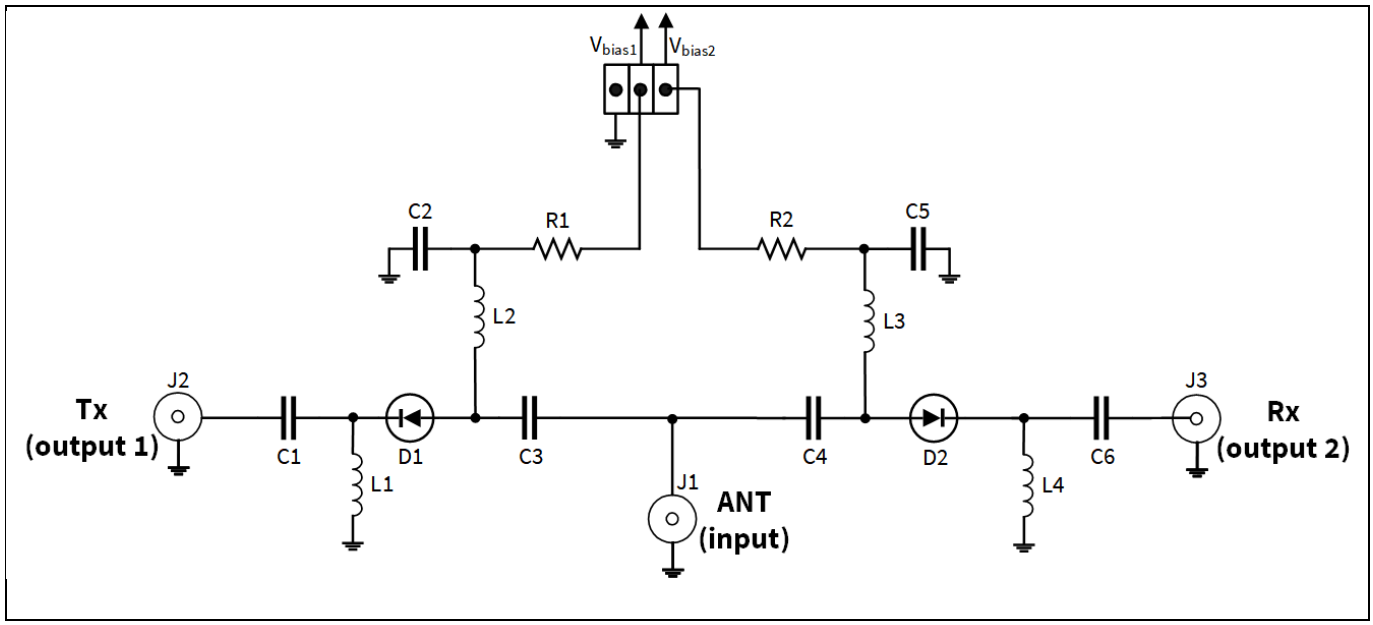

Figure 18 The SPDT series switch schematic

3.1.3 BOM

Table 8 BOM of the SPDT series switch circuit with BAR63-02L

Symbol	Value	Unit	Size	Manufacturer	Comment
D1, D2	BAR63-02L	–	TSLP-2	Infineon	PIN diode
C1	33	pF	0402	Various	DC block and Tx matching
C2	220	nF	0402	Various	RF bypass
C3	33	pF	0402	Various	DC block and input matching
C4	33	pF	0402	Various	DC block and input matching
C5	220	nF	0402	Various	RF bypass
C6	33	pF	0402	Various	DC block and Rx matching
L1	150	nH	0402	Murata LQG	DC return, Tx branch
L2	150	nH	0402	Murata LQG	RF choke
L3	150	nH	0402	Murata LQG	RF choke
L4	150	nH	0402	Murata LQG	DC return, Rx branch
R1	240	Ω	0402	Various	DC bias
R2	240	Ω	0402	Various	DC bias

3.1.4 Evaluation board and layout information

The evaluation board information for the SPDT switch circuit with BAR63-02L:

- PCB material: FR4
- PCB marking: M180629 RF Diode 4

Images of the evaluation board and the PCB stack information are shown in the following figures.

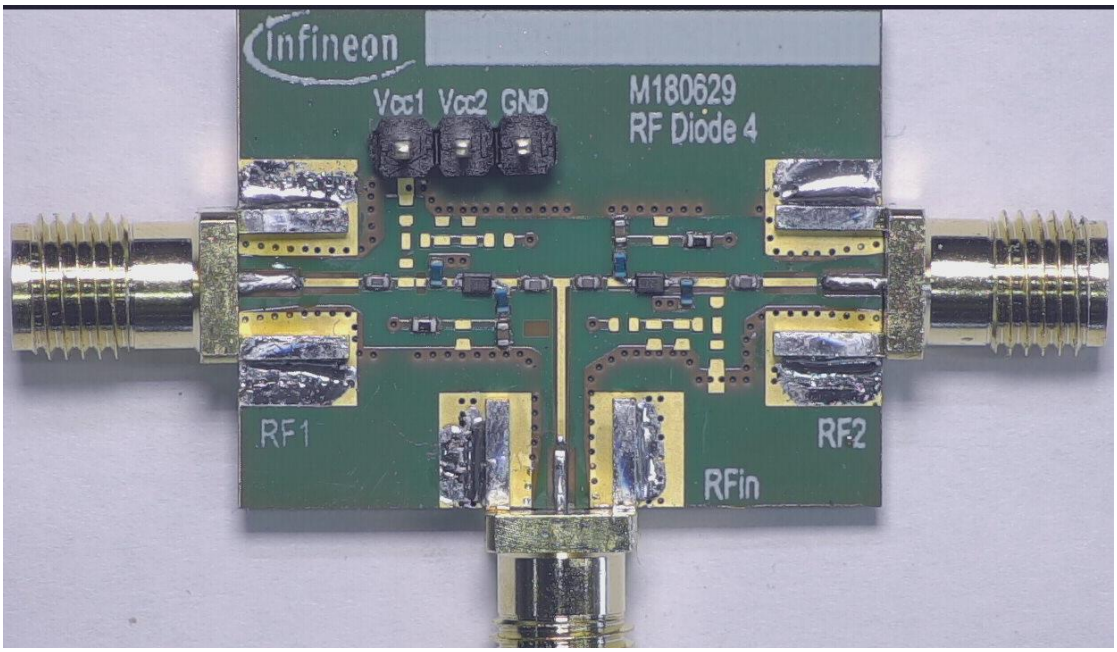

Figure 19 Photo of the evaluation board for PIN diode SPDT switch with BAR63-02L

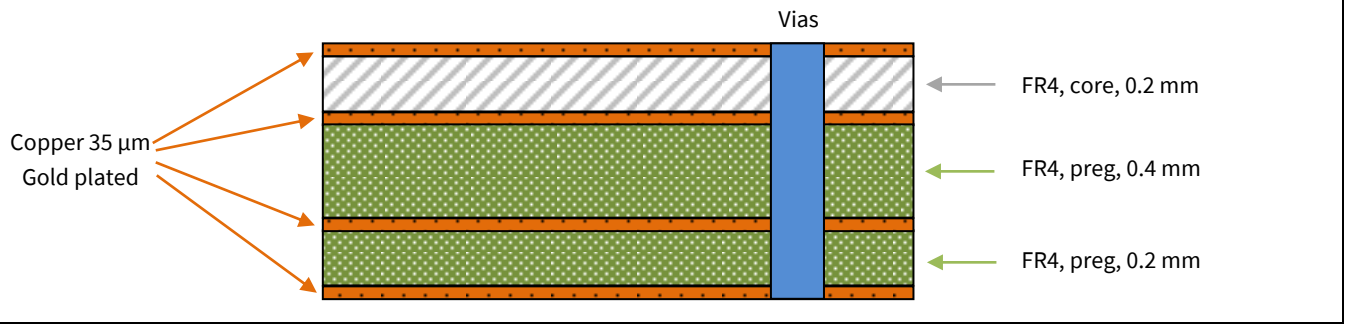

Figure 20 PCB stack information of the evaluation board for PIN diode SPDT switch

3.1.5 Measurement graphs

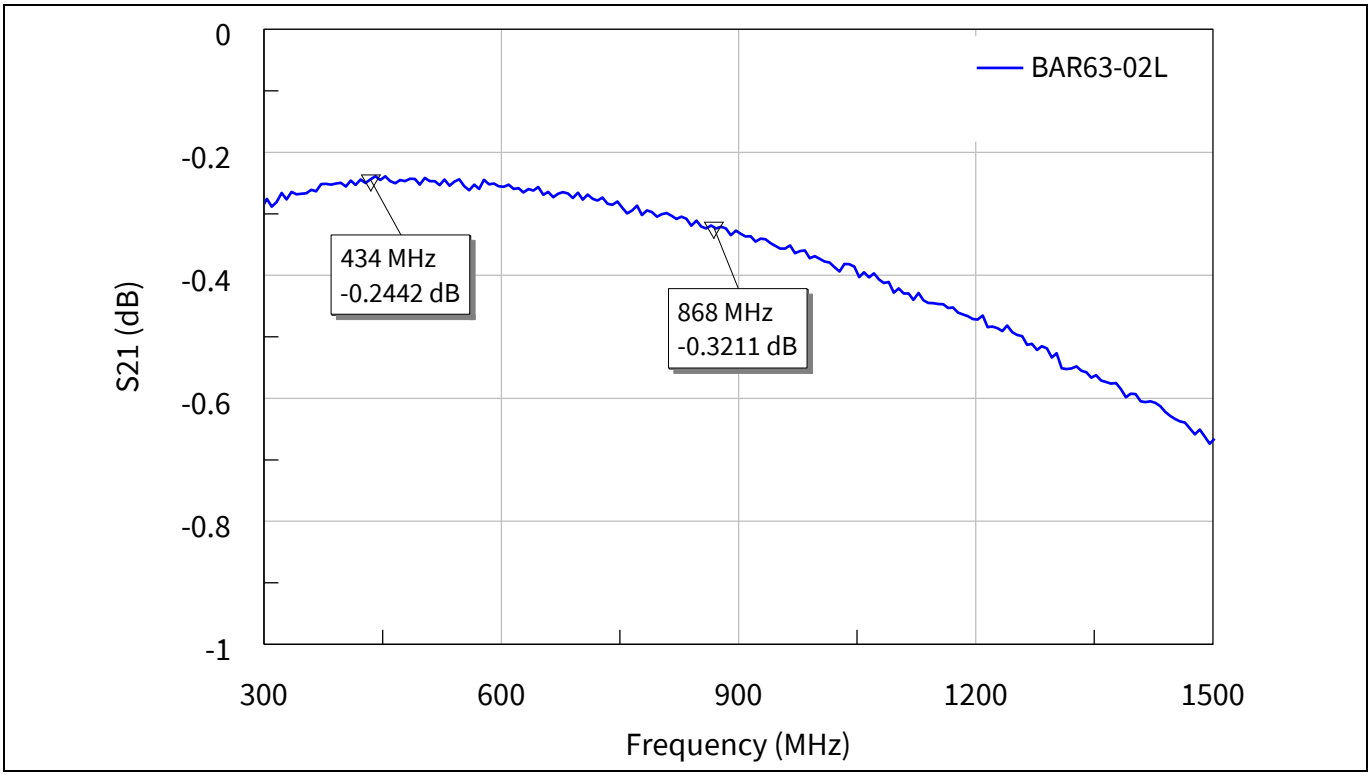

Figure 21 Insertion loss of the SPDT series switch with BAR63-02L in ANT-Tx mode (I_{bias1} = 9.8 mA)

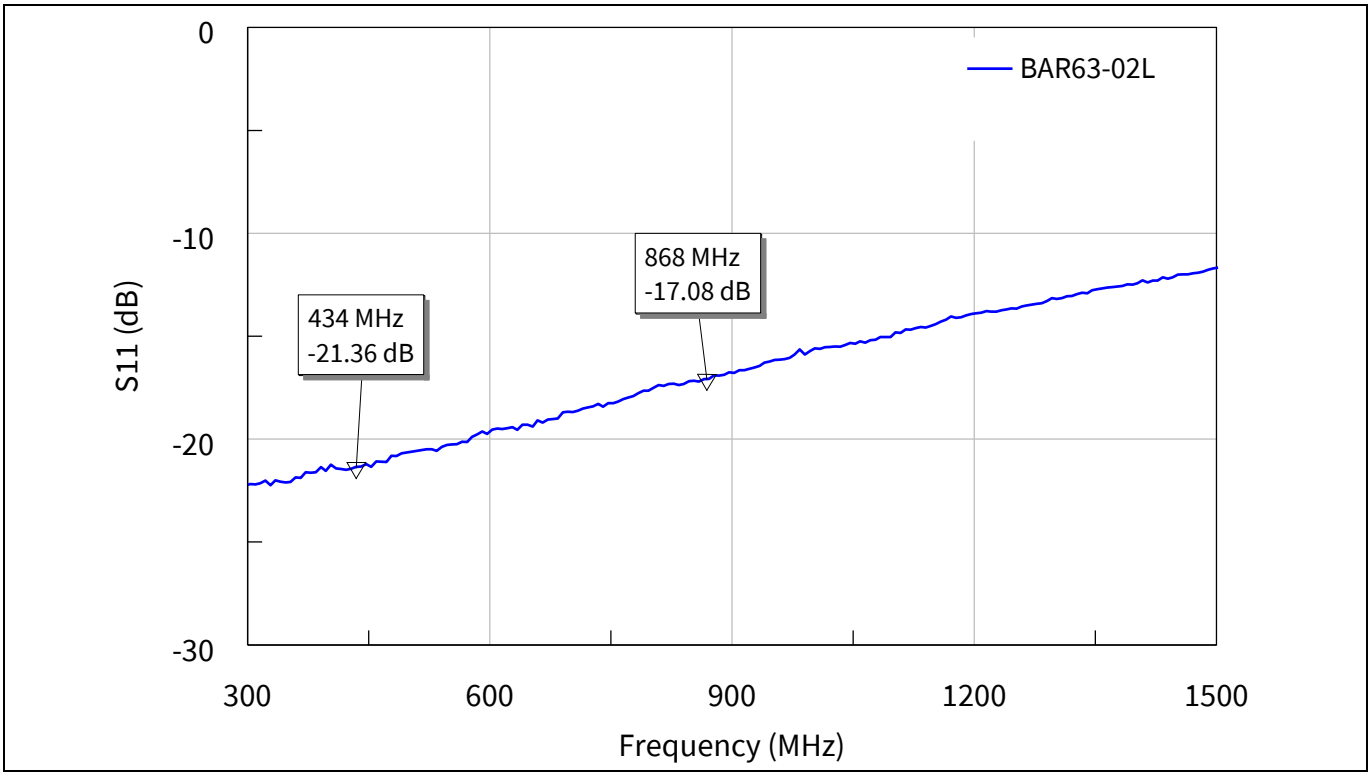

Figure 22 Input return loss of the SPDT series switch with BAR63-02L in ANT-Tx mode (I_{bias1} = 9.8 mA)

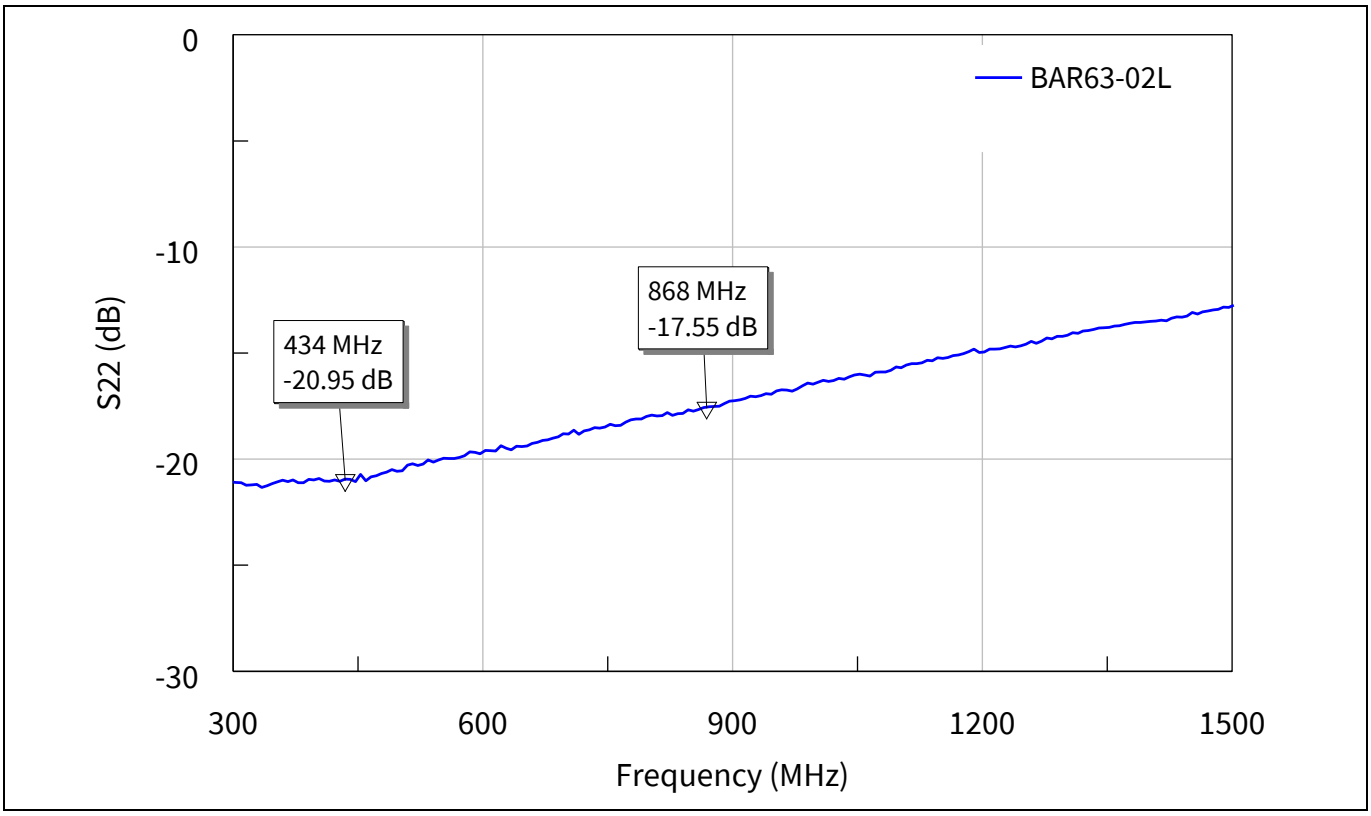

Figure 23 Output return loss of the SPDT series switch with BAR63-02L in ANT-Tx mode (I_{bias1} = 9.8 mA)

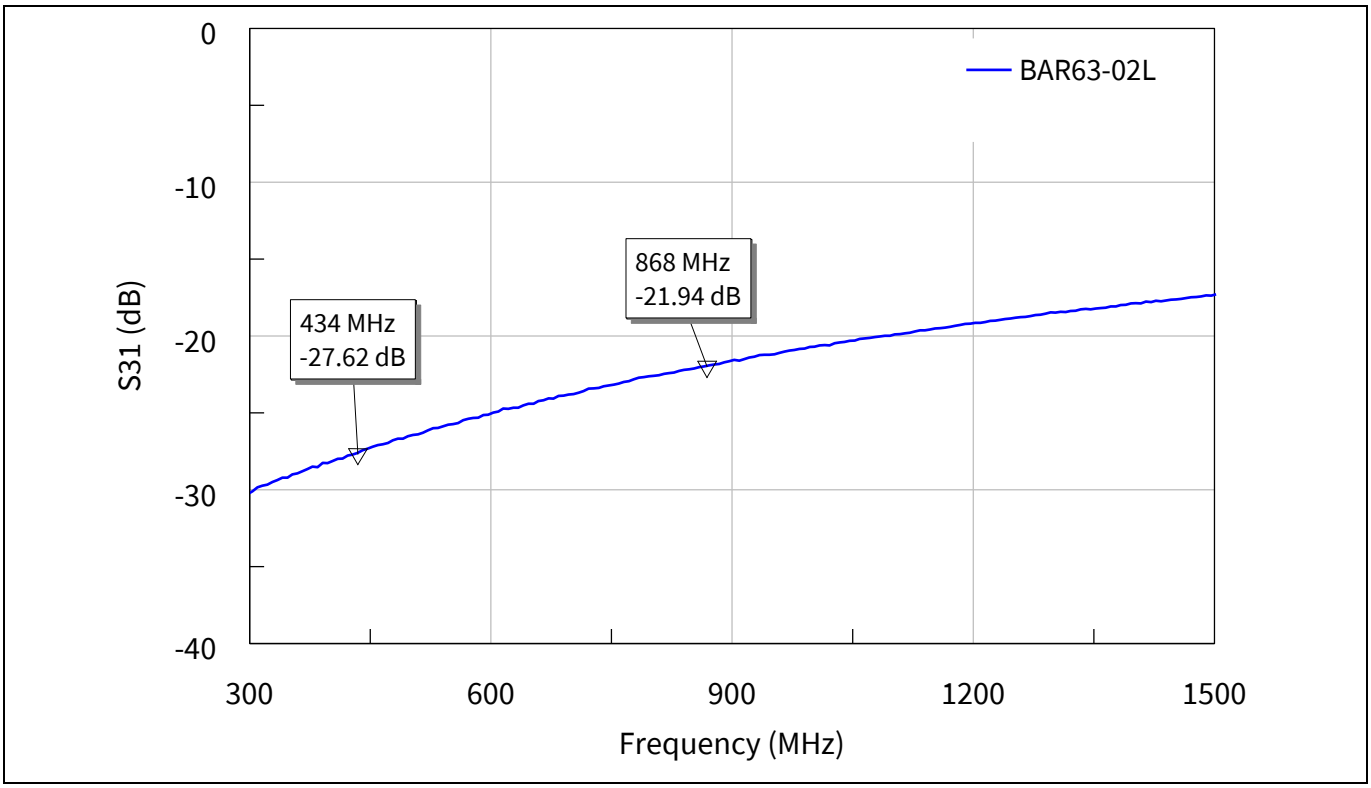

Figure 24 ANT-Rx isolation of the SPDT series switch with BAR63-02L in ANT-Tx mode (I_{bias1} = 9.8 mA)

PIN diode SPDT series switches

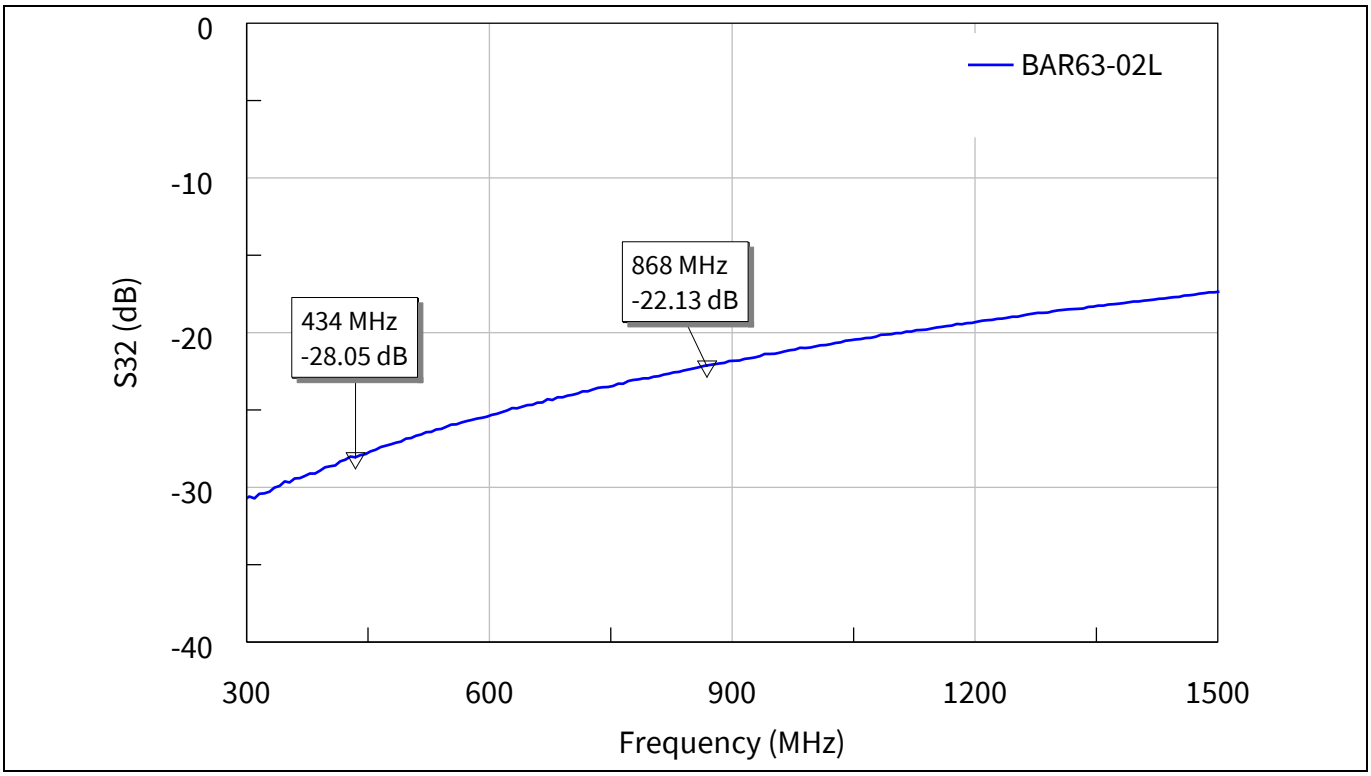

Figure 25 Tx-Rx isolation of the SPDT series switch with BAR63-02L in ANT-Tx mode (I_{bias1} = 9.8 mA)

3.2 S-band range

3.2.1 Performance overview

The following tables show the SPDT series switch performance with PIN diodes BAR50-02V, BAR64-02V and BAR90-02EL.

Table 9 Summary of measurement results of the SPDT series switch circuits for ANT-Tx mode

Parameter	Symbol	Value			Unit	Notes
Device		BAR50-02V	BAR64-02V	BAR90-02EL		
Bias voltage	V_{bias1}	3.3	3.3	3.3	V	Mode: ANT-Tx (V_{bias2} = 0 V)
Bias current	I_{bias1}	10	10.1	10.1	mA	Mode: ANT-Tx (I_{bias2} = 0 A)
Frequency	f	1.5 to 3.7	1.5 to 3.7	1.5 to 3.7	GHz	
Input return loss	RL_{in}	>8.4	>10.1	>10.6	dB	
Output return loss	RL_{out}	>9.9	>11.8	>11.8	dB	
Insertion loss	IL	0.74[1)] 0.64[2)] 1.20[3)]	0.67[1)] 0.67[2)] 0.96[3)]	0.67[1)] 0.72[2)] 0.90[3)]	dB	SMA and PCB losses subtracted 1) Measured at 1.9 GHz (losses = 0.27 dB) 2) Measured at 2.4 GHz (losses = 0.36 dB) 3) Measured at 3.5 GHz (losses = 0.50 dB)
Isolation Tx-Rx	ISO_{Tx-Rx}	19.9[4)] 18.3[5)] 14.9[6)]	18.2[4)] 18.1[5)] 15.2[6)]	16.7[4)] 17.8[5)] 15.8[6)]	dB	4) Measured at 1.9 GHz 5) Measured at 2.4 GHz 6) Measured at 3.5 GHz
Isolation ANT-Rx	ISO_{ANT-Rx}	19.9[4)] 18.3[5)] 14.8[6)]	18.2[4)] 18.1[5)] 15.2[6)]	16.7[4)] 17.8[5)] 15.8[6)]	dB	
Input third order intercept point	IIP_3	>45	>45	>45	dBm	Measured at P_{IN} = 5 dBm
Third order intermodulation distortion	IMD3	>85	>85	>85	dBc	

Table 10 Summary of measurement results of the SPDT series switch circuits for ANT-Rx mode

Parameter	Symbol	Value			Unit	Notes
Device		BAR50-02V	BAR64-02V	BAR90-02EL		
Bias voltage	V_{bias2}	3.3	3.3	3.3	V	Mode: ANT-Rx (V_{bias1} = 0 V)
Bias current	I_{bias2}	10	10	10.1	mA	Mode: ANT-Rx (I_{bias1} = 0 A)
Frequency	f	1.5 to 3.7	1.5 to 3.7	1.5 to 3.7	GHz	
Input return loss	RL_{in}	>8	>9.2	>10.7	dB	
Output return loss	RL_{out}	>9.1	>10.8	>11.2	dB	
Insertion loss	IL	0.77[1)] 0.58[2)] 1.07[3)]	0.72[1)] 0.62[2)] 1.0[3)]	0.68[1)] 0.67[2)] 0.87[3)]	dB	SMA and PCB losses subtracted 1) Measured at 1.9 GHz (losses = 0.27 dB) 2) Measured at 2.4 GHz (losses = 0.36 dB) 3) Measured at 3.5 GHz (losses = 0.50 dB)
Isolation Tx-Rx	ISO_{Tx-Rx}	21.5[4)] 19.9[5)] 16.4[6)]	17.6[4)] 17.4[5)] 14.4[6)]	16.7[4)] 17.8[5)] 15.7[6)]	dB	4) Measured at 1.9 GHz 5) Measured at 2.4 GHz 6) Measured at 3.5 GHz
Isolation ANT-Tx	ISO_{ANT-Tx}	21.8[4)] 20.2[5)] 16.8[6)]	17.7[4)] 17.5[5)] 14.6[6)]	17.6[4)] 18.0[5)] 15.1[6)]	dB	
Input third order intercept point	IIP_3	>45	>45	>45	dBm	Measured at P_{IN} = 5 dBm
Third order intermodulation distortion	IMD3	>85	>85	>85	dBc	

3.2.2 Schematic

The following figure shows the schematic of the SPDT series switch. In the schematic, each branch of the switch contains one series-connected PIN diode. The resistors R1 and R2 are used to set the bias current for the branch one and the branch two of the switch respectively. The inductors L1 and L4 provide the DC return path for the bias current. The capacitors C2 and C5 serve as the RF bypass. The capacitors C3 and C4 provide the DC block and the matching at the common input port. The matching network at output port one is formed by the capacitor C1 and the inductor L1, and the matching network at output two is formed by the capacitor C6 and the inductor L4.

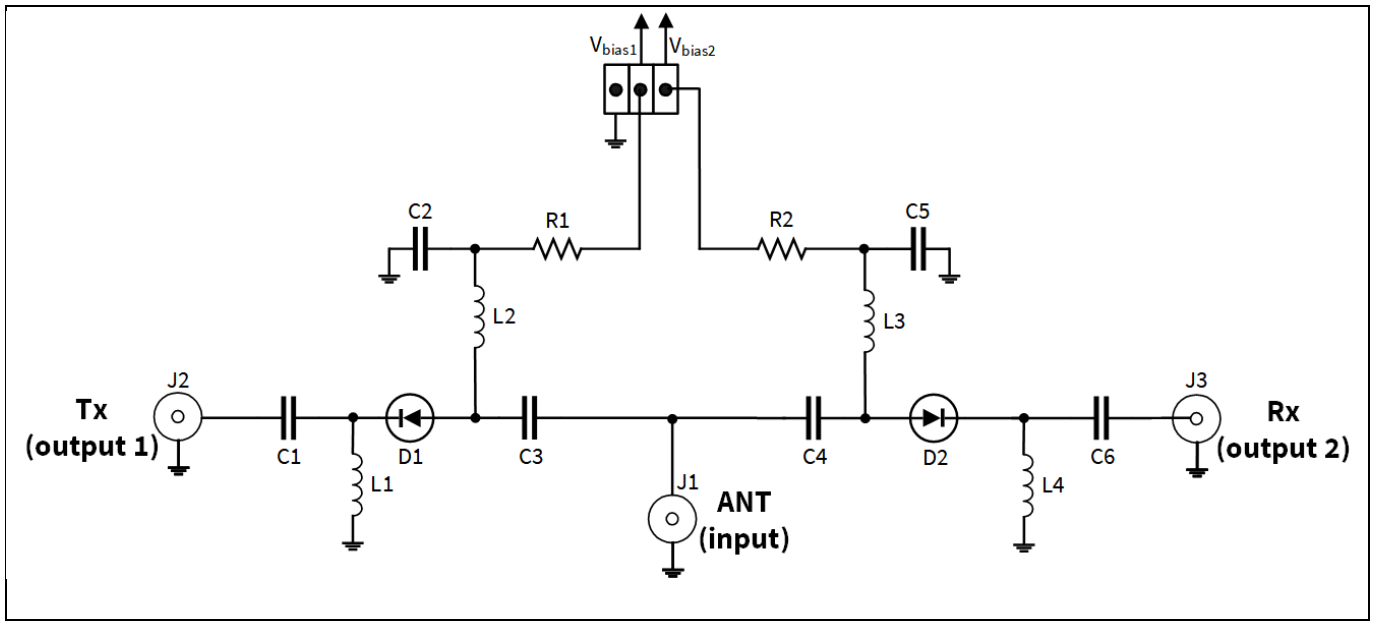

Figure 26 The SPDT series switch schematic

3.2.3 BOM

Table 11 BOM of the SPDT series switch circuits with BAR50-02V, BAR64-02V and BAR90-02EL

Symbol	Value			Unit	Size	Manufacturer	Comment
D1, D2	BAR50-02V (SC79)	BAR64-02V (SC79)	BAR90-02EL (TSLP-2)	–	–	Infineon	PIN diode
C1	2.7	2.2	1.8	pF	0402	Various	DC block and Tx matching
C2	220	220	220	nF	0402	Various	RF bypass
C3	3.9	2.2	1.8	pF	0402	Various	DC block and input matching
C4	3.9	2.2	1.8	pF	0402	Various	DC block and input matching
C5	220	220	220	nF	0402	Various	RF bypass
C6	2.7	2.2	1.8	pF	0402	Various	DC block and Rx matching
L1	7.5	6.8	6.8	nH	0402	Murata LQG	DC return, Tx branch
L2	7.5	6.8	6.8	nH	0402	Murata LQG	RF choke
L3	7.5	6.8	6.8	nH	0402	Murata LQG	RF choke
L4	7.5	6.8	6.8	nH	0402	Murata LQG	DC return, Rx branch
R1	240	240	240	Ω	0402	Various	DC bias
R2	240	240	240	Ω	0402	Various	DC bias

3.2.4 Evaluation board and layout information

The evaluation board information for the SPST switch circuit with BAR50-02V, BAR64-02V and BAR90-02EL:

- PCB material: FR4
- PCB marking: M180629 RF Diode 4

Images of the evaluation board and the PCB stack information are shown in the following figures.

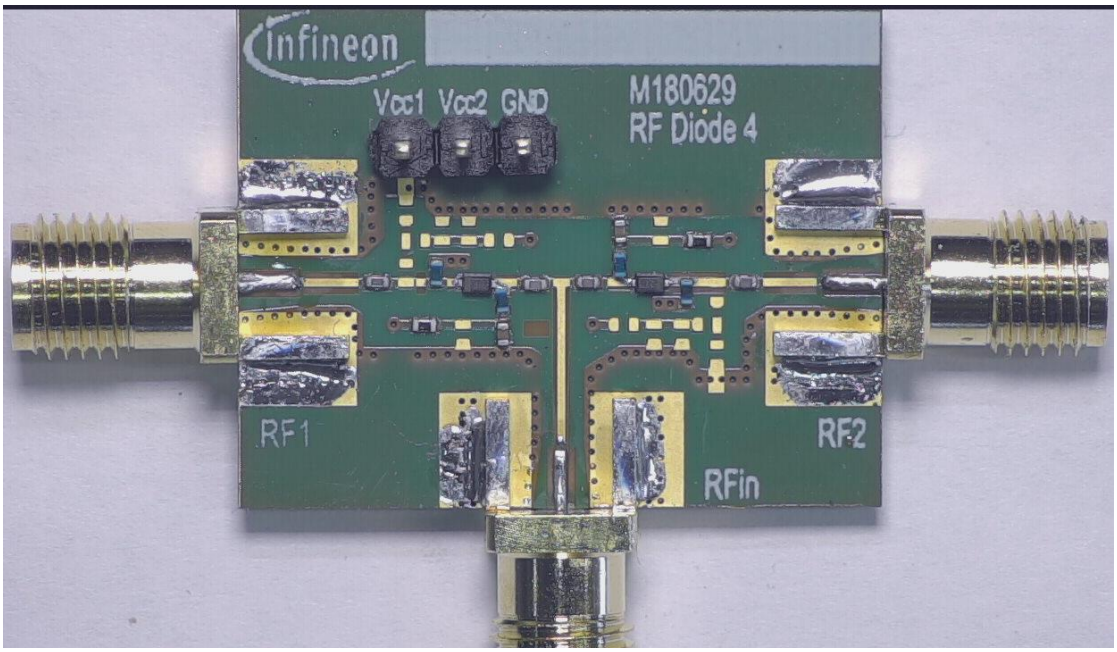

Figure 27 Photo of the evaluation board for the PIN diode SPDT switch with BAR50-02V, BAR64-02V and BAR90-02EL

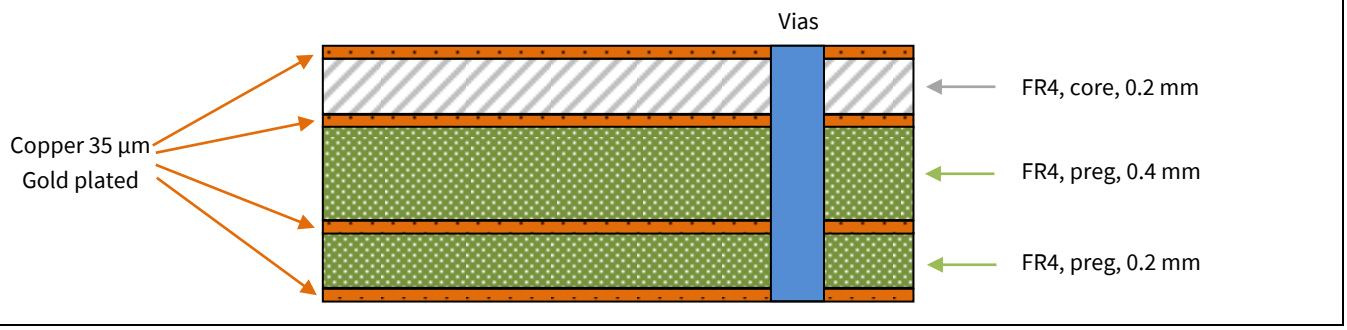

Figure 28 PCB stack information of the evaluation board for the PIN diode SPDT switch

3.2.5 Measurement graphs

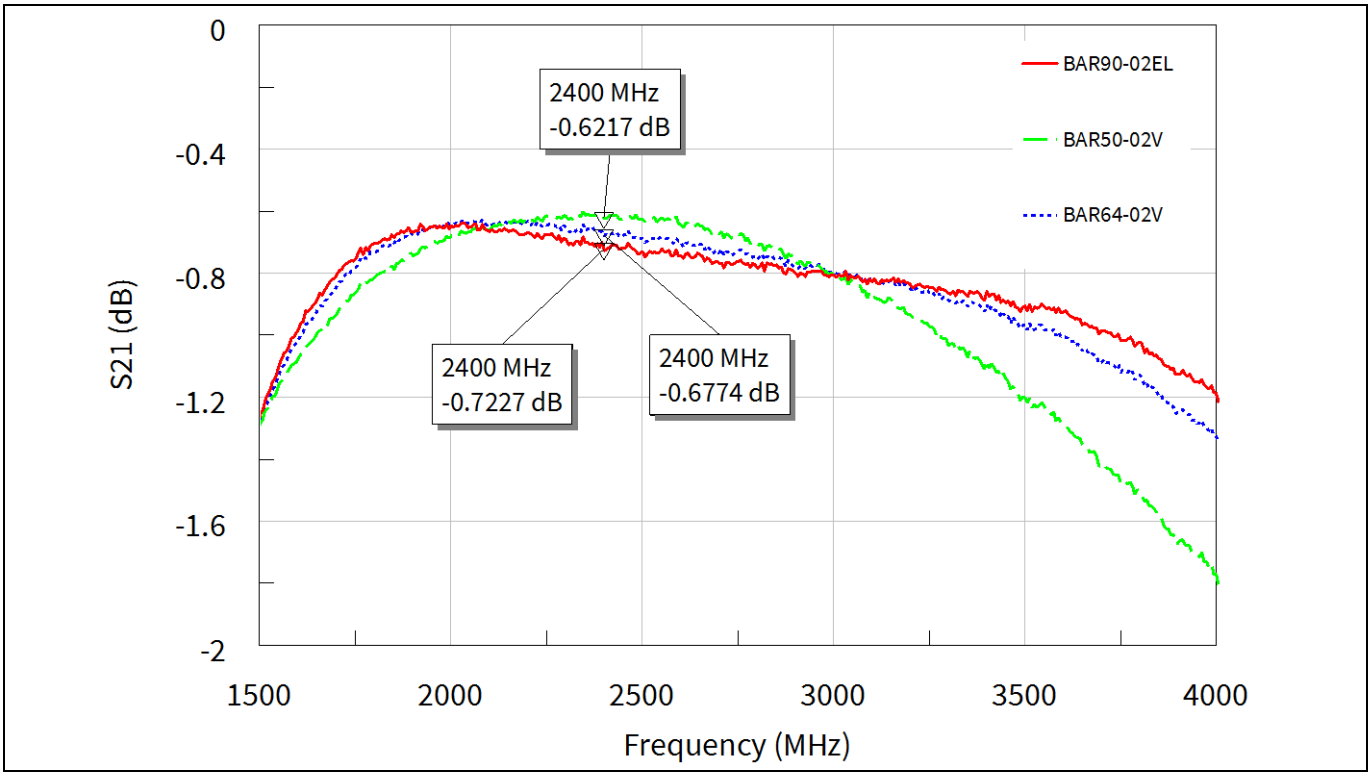

Figure 29 Insertion loss of the SPDT series switch with BAR50-02V, BAR64-02V and BAR90-02EL in ANT-Tx mode (I_{bias1} = 10 mA)

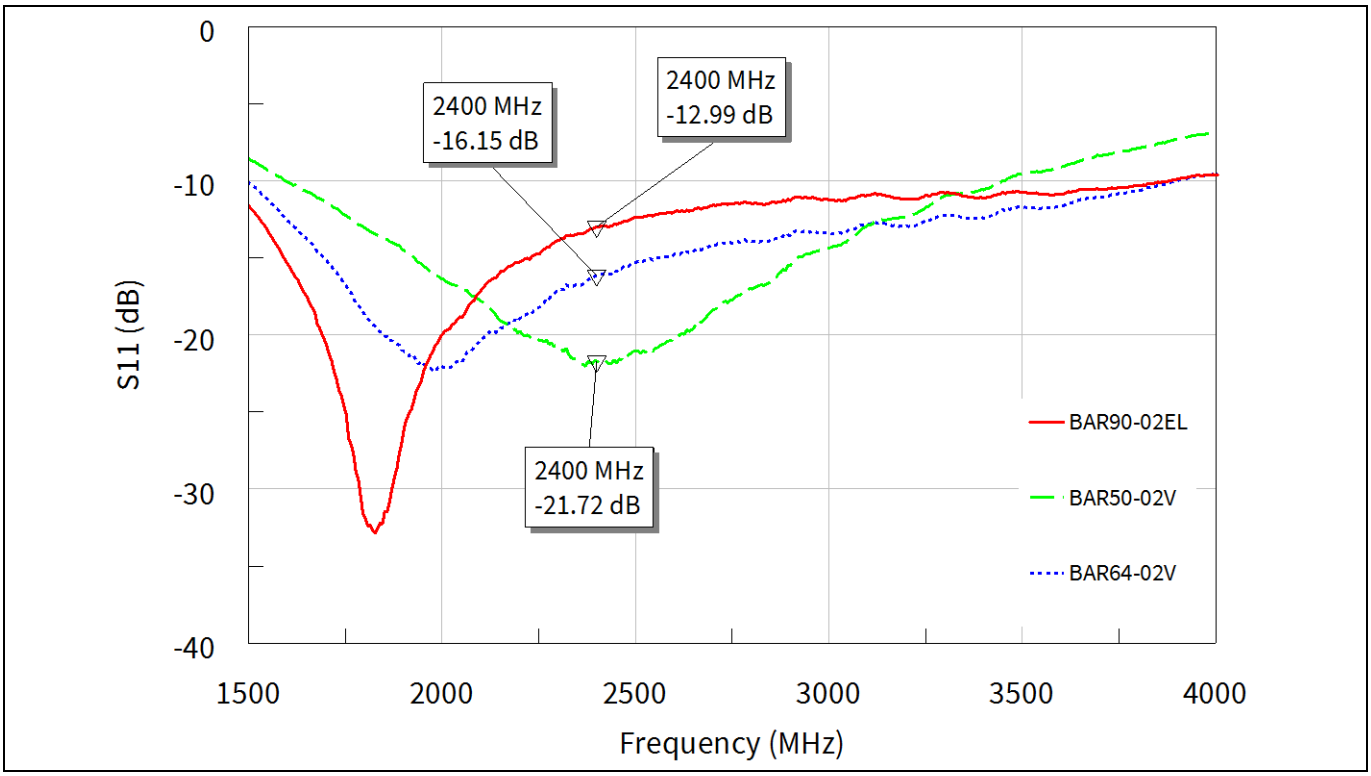

Figure 30 Input return loss of the SPDT series switch with BAR50-02V, BAR64-02V and BAR90-02EL in ANT-Tx mode (I_{bias1} = 10 mA)

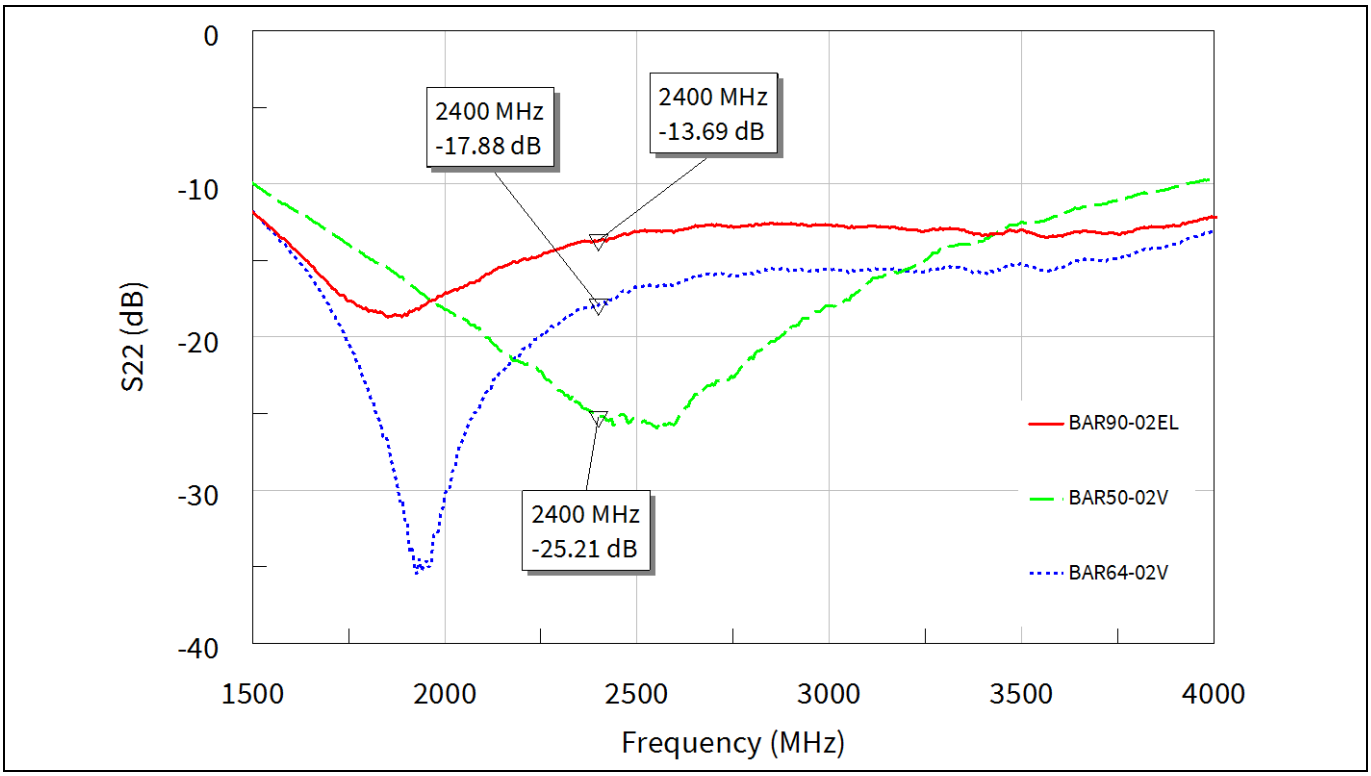

Figure 31 Output return loss of the SPDT series switch with BAR50-02V, BAR64-02V and BAR90-02EL in ANT-Tx mode (I_{bias1} = 10 mA)

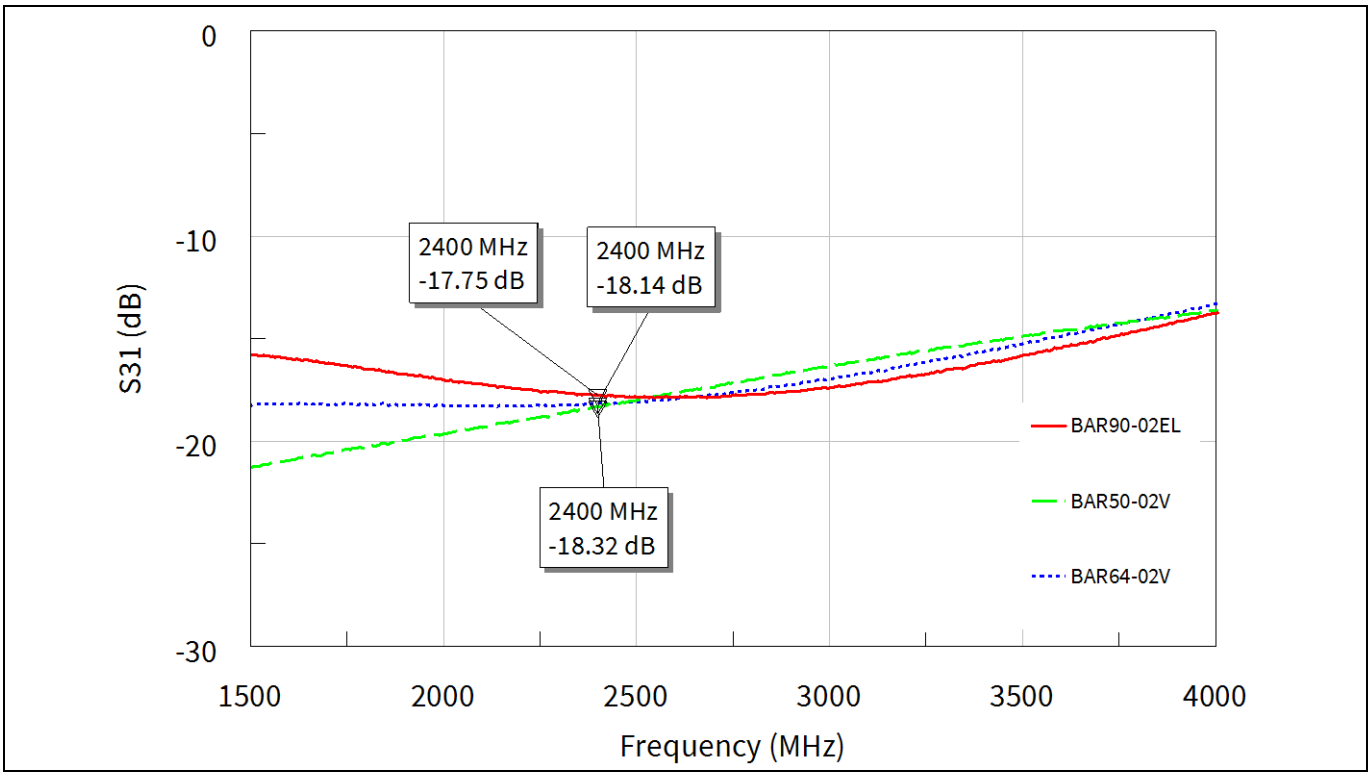

Figure 32 ANT-Rx isolation of the SPDT series switch with BAR50-02V, BAR64-02V and BAR90-02EL in ANT-Tx mode (I_{bias1} = 10 mA)

PIN diode SPDT series switches

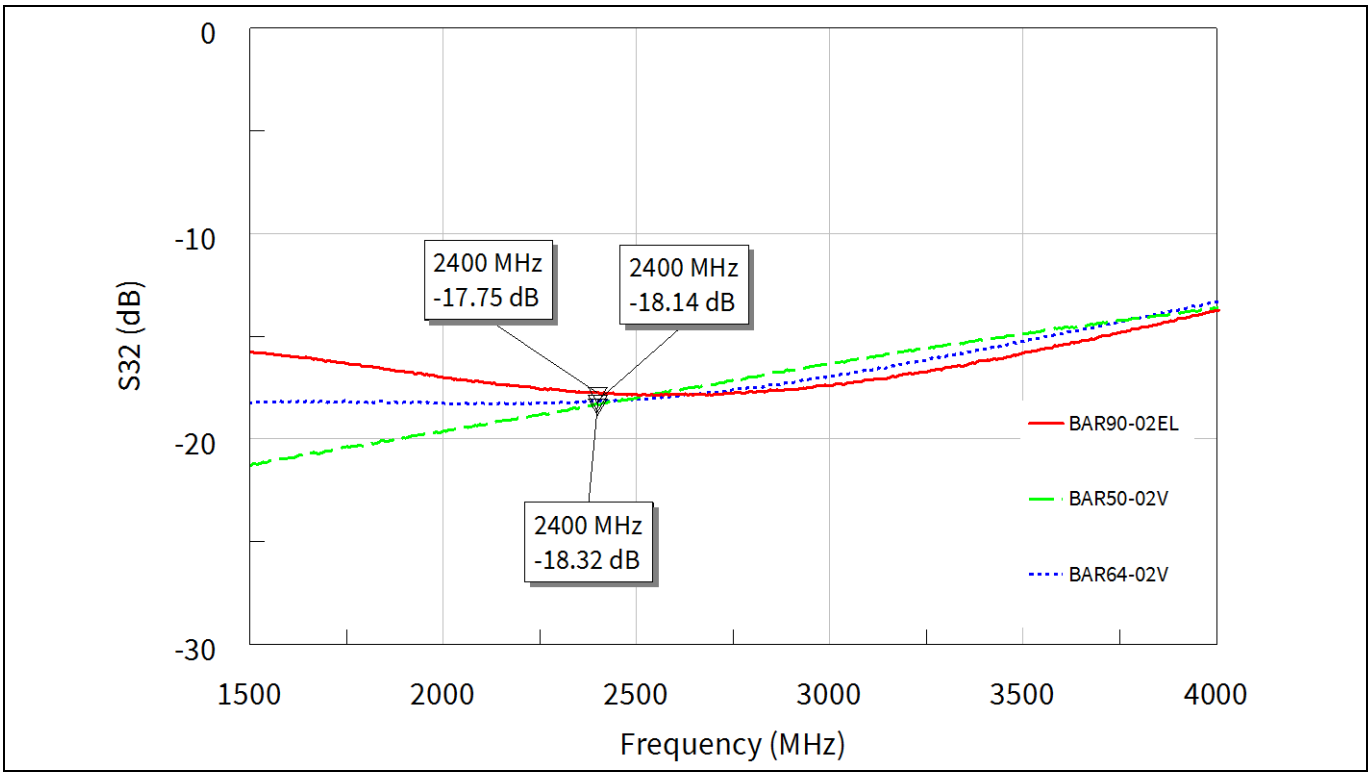

Figure 33 **Tx-Rx isolation of the SPDT series switch with BAR50-02V, BAR64-02V and BAR90-02EL in ANT-Tx mode (I_{bias1} = 10 mA)**

4 PIN diode SPDT series and shunt switches

4.1 Sub-GHz range

4.1.1 Performance overview

The following tables show the SPDT series and shunt switch performance with PIN diode BAR63-02L.

Table 12 Summary of measurement results of the SPDT series switch circuit for ANT-Tx mode

Parameter	Symbol	Value	Unit	Notes
Device		BAR63-02L		
Bias voltage	V_{bias1}	3.3	V	Mode: ANT-Tx (V_{bias2} = 0 V)
Bias current	I_{bias1}	9.8	mA	Mode: ANT-Tx (I_{bias2} = 0 A)
Frequency	f	300 to 1000	MHz	
Input return loss	RL_{in}	>14.8	dB	
Output return loss	RL_{out}	>15.5	dB	
Insertion loss	IL	0.48[1)] 0.28[2)] 0.33[3)]	dB	SMA and PCB losses subtracted 1) Measured at 315 MHz (losses = 0.05 dB) 2) Measured at 434 MHz (losses = 0.06 dB) 3) Measured at 868 MHz (losses = 0.12 dB)
Isolation Tx-Rx	ISO_{Tx-Rx}	39.2[4)] 38.8[5)] 47.2[6)]	dB	4) Measured at 315 MHz 5) Measured at 434 MHz 6) Measured at 868 MHz
Isolation ANT-Rx	ISO_{ANT-Rx}	38.8[4)] 38.5[5)] 47.9[6)]	dB	
Input third order intercept point	IIP_3	>45	dBm	Measured at P_{IN} = 5 dBm
Third order intermodulation distortion	IMD3	>85	dBc	

Table 13 Summary of measurement results of the SPDT series switch circuit for ANT-Rx mode

Parameter	Symbol	Value	Unit	Notes
Device		BAR63-02L		
Bias voltage	V_{bias2}	3.3	V	Mode: ANT-Rx (V_{bias1} = 0 V)
Bias current	I_{bias2}	9.8	mA	Mode: ANT-Rx (I_{bias1} = 0 A)
Frequency	f	300 to 1000	MHz	
Input return loss	RL_{in}	>14.7	dB	
Output return loss	RL_{out}	>14.5	dB	
Insertion loss	IL	0.49[1)] 0.28[2)] 0.34[3)]	dB	SMA and PCB losses subtracted 1) Measured at 315 MHz (losses = 0.05 dB) 2) Measured at 434 MHz (losses = 0.06 dB) 3) Measured at 868 MHz (losses = 0.12 dB)
Isolation Tx-Rx	ISO_{Tx-Rx}	38.7[4)] 38.6[5)] 46.5[6)]	dB	4) Measured at 315 MHz 5) Measured at 434 MHz 6) Measured at 868 MHz
Isolation ANT-Tx	ISO_{ANT-Tx}	38.7[4)] 38.4[5)] 46.8[6)]	dB	
Input third order intercept point	IIP_3	>45	dBm	Measured at P_{IN} = 5 dBm
Third order intermodulation distortion	IMD3	>85	dBc	

4.1.2 Schematic

The following figure shows the schematic of the SPDT series and shunt switch. In the schematic, each branch of the switch contains one series and one shunt-connected PIN diode. The resistors R2 and R3 are used to set the bias current for series-connected diodes in the branch one and the branch two of the switch respectively, while the resistors R1 and R4 are used to set the bias current for shunt-connected diodes in each branch. The inductors L2 and L5 provide the DC return path for the bias current of the series-connected diodes. The capacitors C3, C5, C6 and C9 serve as the RF bypass. The capacitors C4 and C7 provide the DC block and the matching at the common input port. The matching network at output port one is formed by the capacitors C1 and C2 and the inductor L2, and the matching network at output two is formed by the capacitors C8 and C10 and the inductor L5.

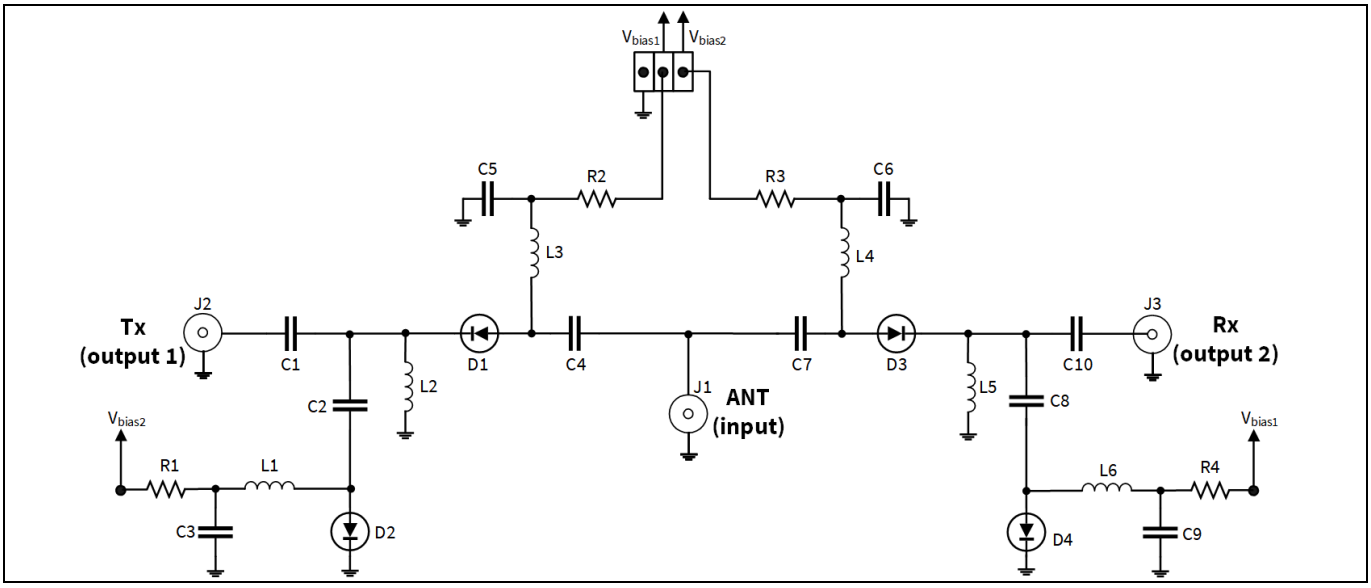

Figure 34 The SPDT series and shunt switch schematic

4.1.3 BOM

Table 14 BOM of the SPDT series and shunt switch circuit with BAR63-02L

Symbol	Value	Unit	Size	Manufacturer	Comment
D1–D4	BAR63-02L	–	TSLP-2	Infineon	PIN diode
C1	39	pF	0402	Various	DC block and Tx matching
C2	15	pF	0402	Various	DC block and Tx matching
C3	220	nF	0402	Various	RF bypass
C4	39	pF	0402	Various	DC block and input matching
C5	220	nF	0402	Various	RF bypass
C6	220	nF	0402	Various	RF bypass
C7	39	pF	0402	Various	DC block and input matching
C8	15	pF	0402	Various	DC block and Rx matching
C9	220	nF	0402	Various	RF bypass
C10	39	pF	0402	Various	DC block and Rx matching
L1	68	nH	0402	Murata LQW	RF choke
L2	150	nH	0402	Murata LQG	DC return, Tx branch
L3	150	nH	0402	Murata LQG	RF choke

PIN diode SPDT series and shunt switches

Symbol	Value	Unit	Size	Manufacturer	Comment
L4	150	nH	0402	Murata LQG	RF choke
L5	150	nH	0402	Murata LQG	DC return, Rx branch
L6	68	nH	0402	Murata LQW	RF choke
R1	470	Ω	0402	Various	DC bias
R2	510	Ω	0402	Various	DC bias
R3	510	Ω	0402	Various	DC bias
R4	470	Ω	0402	Various	DC bias

4.1.4 Evaluation board and layout information

The evaluation board information for the SPDT series and shunt switch circuit with BAR63-02L:

- PCB material: FR4
- PCB marking: M180629 RF Diode 4

Images of the evaluation board and the PCB stack information are shown in the following figures.

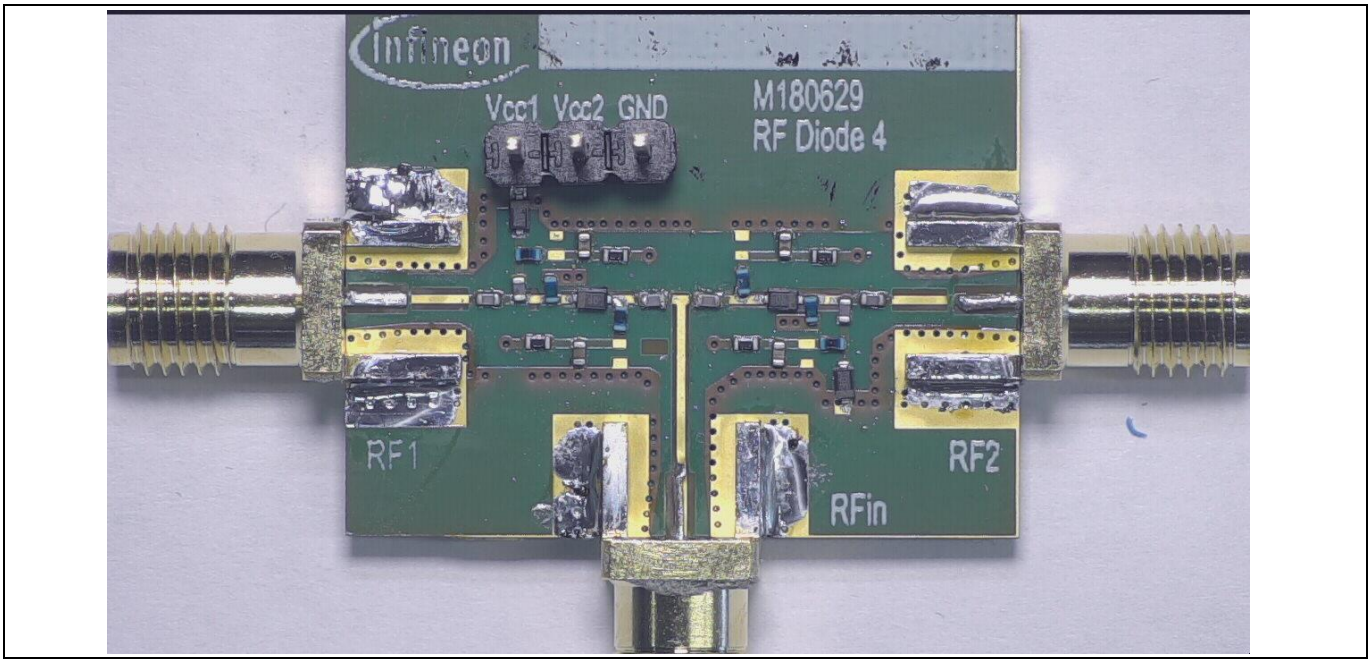

Figure 35 Photo of the evaluation board for PIN diode SPDT series and shunt switch with BAR63-02L

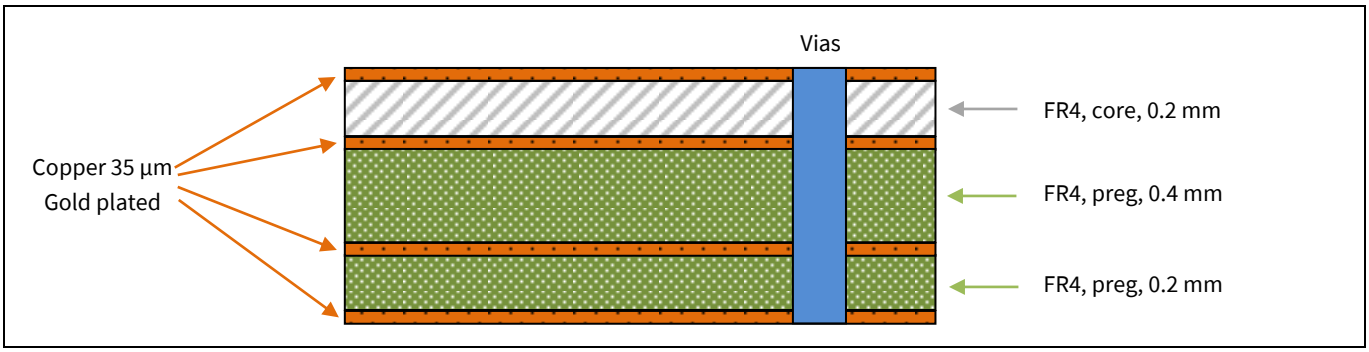

Figure 36 PCB stack information of the evaluation board for PIN diode SPDT switch

4.1.5 Measurement graphs

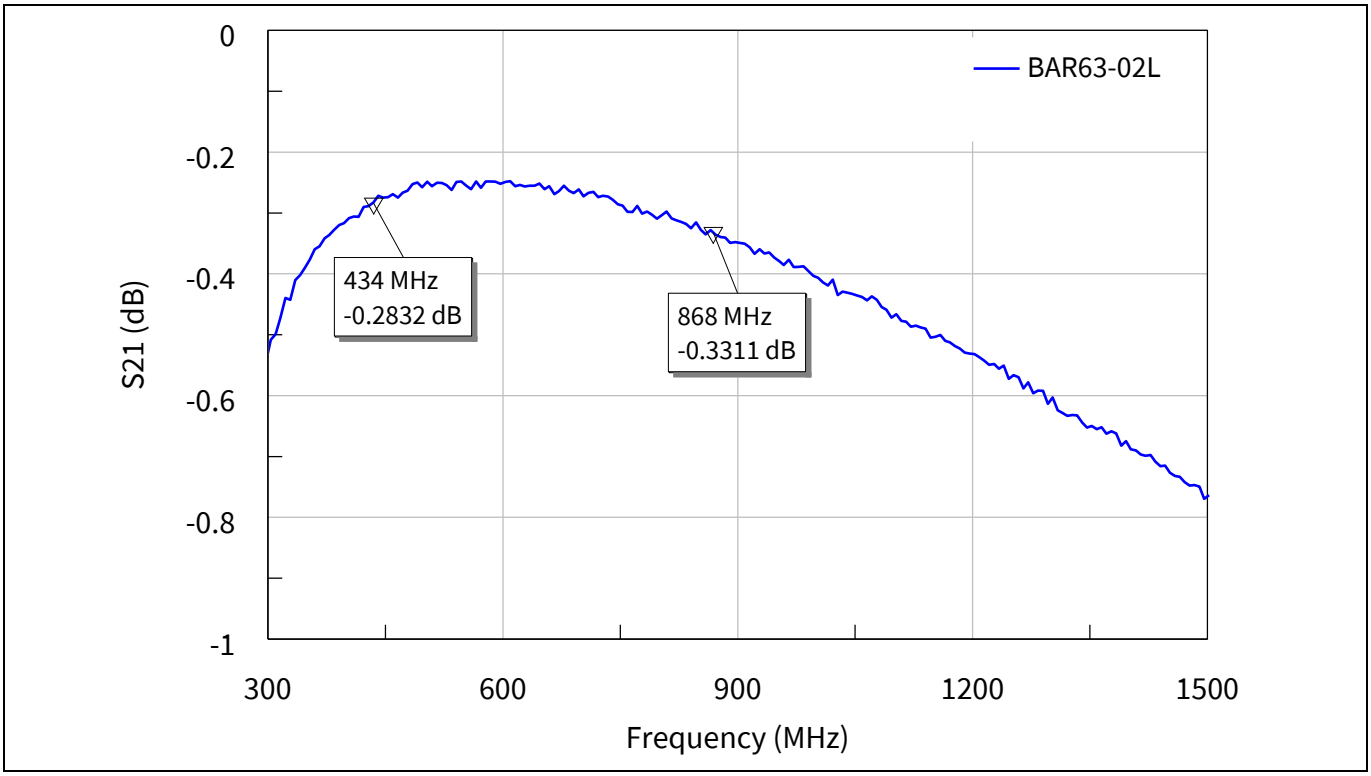

Figure 37 Insertion loss of the SPDT series and shunt switch with BAR63-02L in ANT-Tx mode (I_{bias1} = 9.8 mA)

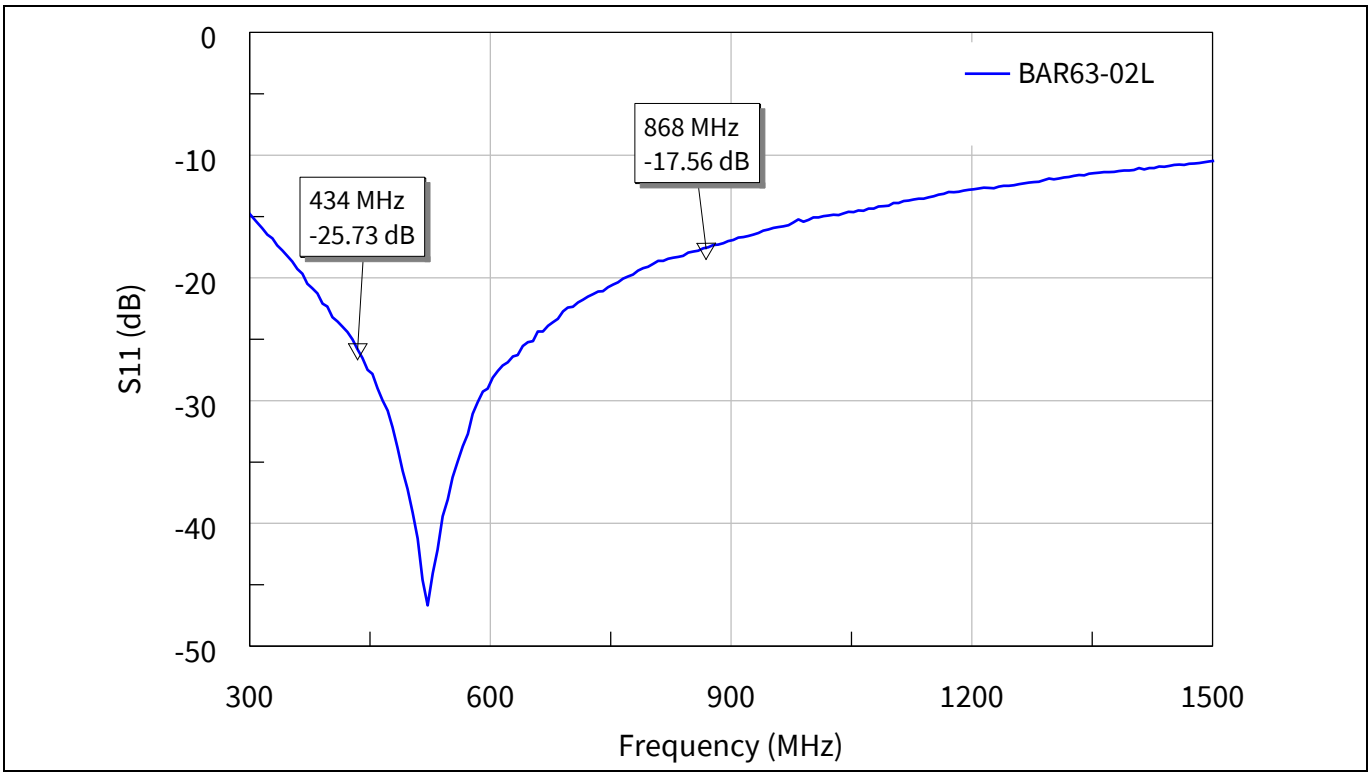

Figure 38 Input return loss of the SPDT series and shunt switch with BAR63-02L in ANT-Tx mode (I_{bias1} = 9.8 mA)

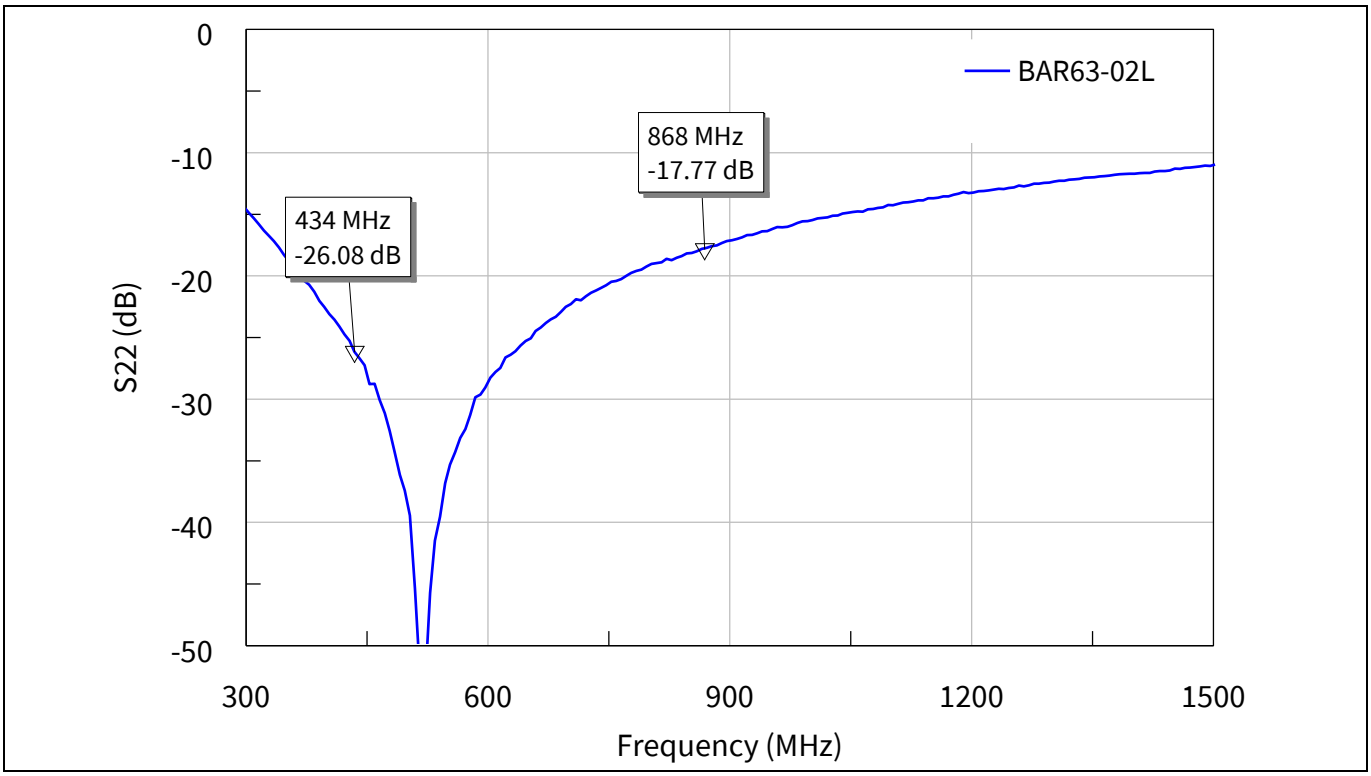

Figure 39 Output return loss of the SPDT series and shunt switch with BAR63-02L in ANT-Tx mode (I_{bias1} = 9.8 mA)

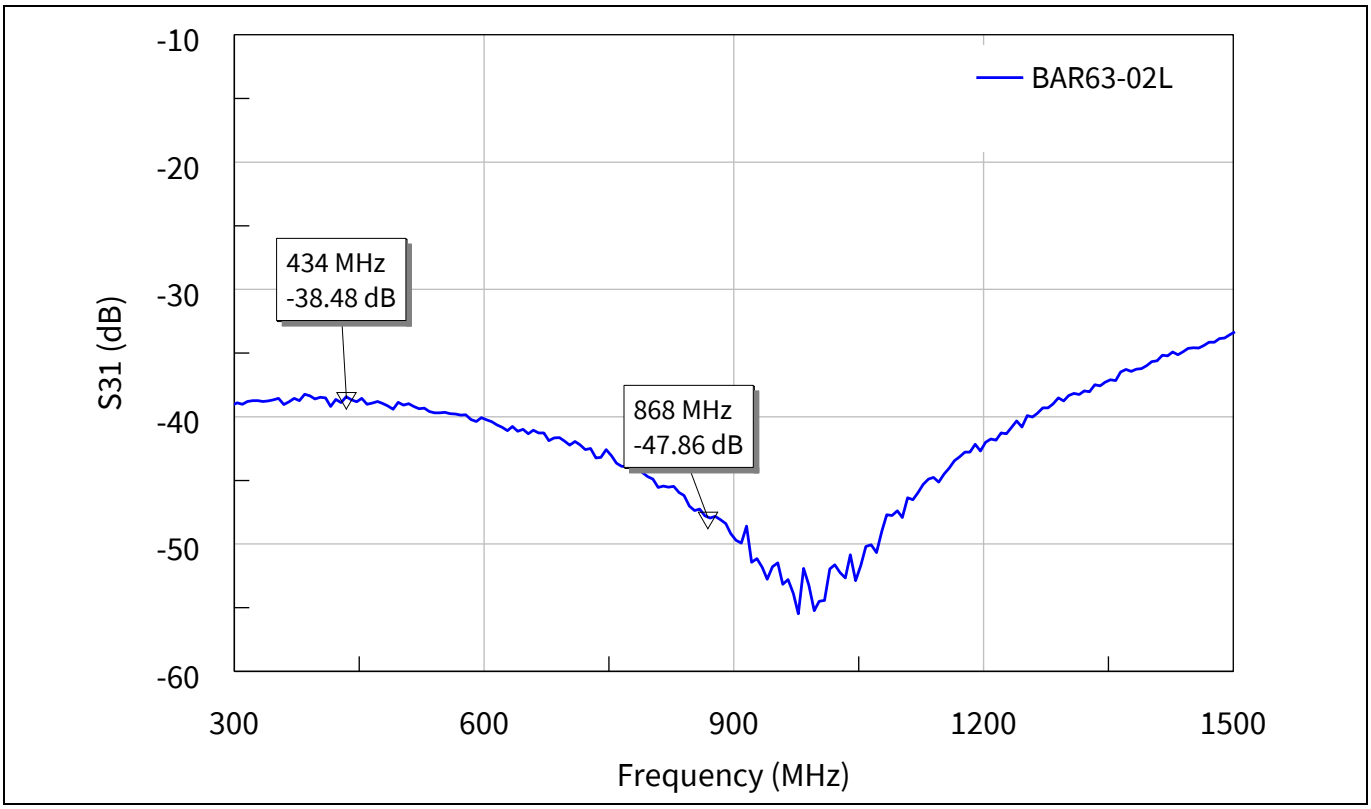

Figure 40 ANT-Rx isolation of the SPDT series and shunt switch with BAR63-02L in ANT-Tx mode (I_{bias1} = 9.8 mA)

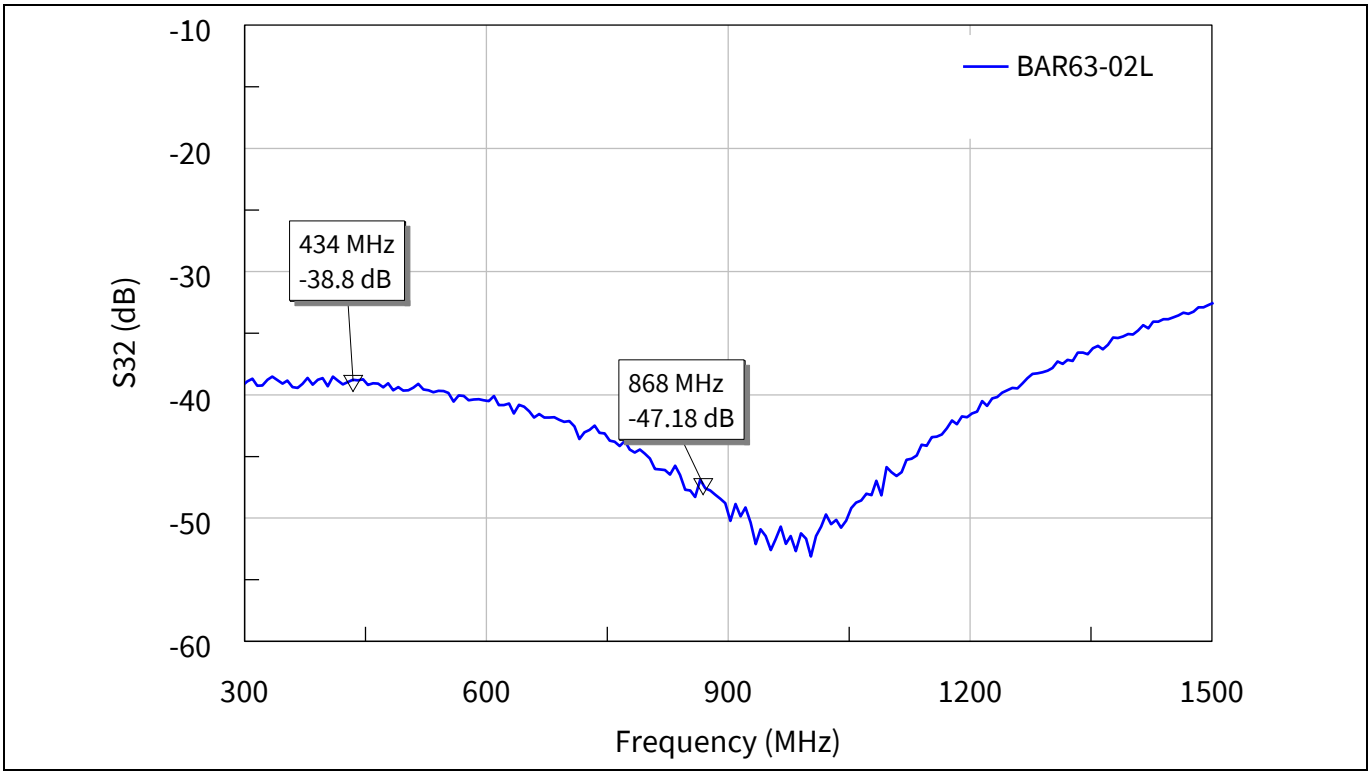

Figure 41 Tx-Rx isolation of the SPDT series and shunt switch with BAR63-02L in ANT-Tx mode (I_{bias1} = 9.8 mA)

4.2 S-band range

4.2.1 Performance overview

The following tables show the SPDT series and shunt switch performance with PIN diodes BAR50-02V, BAR64-02V and BAR90-02EL.

Table 15 Summary of measurement results of the SPDT series and shunt switch circuits for ANT-Tx mode

Parameter	Symbol	Value			Unit	Notes
Device		BAR50-02V	BAR64-02V	BAR90-02EL		
Bias voltage	V_{bias1}	3.3	3.3	3.3	V	Mode: ANT-Tx (V_{bias2} = 0 V)
Bias current	I_{bias1}	10	10	10	mA	Mode: ANT-Tx (I_{bias2} = 0 A)
Frequency	f	1.5 to 3.7	1.5 to 3.7	1.5 to 3.7	GHz	
Input return loss	RL_{in}	>9.7	>9.5	>10.4	dB	
Output return loss	RL_{out}	>11.1	>11.2	>11.7	dB	
Insertion loss	IL	1.04[1)] 1.15[2)] 1.47[3)]	0.79[1)] 0.79[2)] 1.22[3)]	0.66[1)] 0.77[2)] 1.10[3)]	dB	SMA and PCB losses subtracted 1) Measured at 1.9 GHz (losses = 0.27 dB) 2) Measured at 2.4 GHz (losses = 0.36 dB) 3) Measured at 3.5 GHz (losses = 0.50 dB)
Isolation Tx-Rx	ISO_{Tx-Rx}	33.9[4)] 39.4[5)] 22.7[6)]	32.3[4)] 40.1[5)] 21.5[6)]	29.3[4)] 38.1[5)] 19.2[6)]	dB	4) Measured at 1.9 GHz 5) Measured at 2.4 GHz 6) Measured at 3.5 GHz
Isolation ANT-Rx	ISO_{ANT-Rx}	34.2[4)] 40.3[5)] 23.5[6)]	32.4[4)] 40.4[5)] 22.4[6)]	29.7[4)] 39.2[5)] 20.5[6)]	dB	
Input third order intercept point	IIP_3	>45	>45	>45	dBm	Measured at P_{IN} = 5 dBm
Third order intermodulation distortion	IMD3	>85	>85	>85	dBc	

Table 16 Summary of measurement results of the SPDT series and shunt switch circuits for ANT-Rx mode

Parameter	Symbol	Value			Unit	Notes
Device		BAR50-02V	BAR64-02V	BAR90-02EL		
Bias voltage	V_{bias2}	3.3	3.3	3.3	V	Mode: ANT-Rx (V_{bias1} = 0 V)
Bias current	I_{bias2}	10.1	10	10	mA	Mode: ANT-Rx (I_{bias1} = 0 A)
Frequency	f	1.5 to 3.7	1.5 to 3.7	1.5 to 3.7	GHz	
Input return loss	RL_{in}	>9.8	>10.1	>10.5	dB	
Output return loss	RL_{out}	>11.4	>12	>11.6	dB	
Insertion loss	IL	1.02[1)] 1.08[2)] 1.47[3)]	0.78[1)] 0.81[2)] 1.27[3)]	0.73[1)] 0.79[2)] 1.14[3)]	dB	SMA and PCB losses subtracted 1) Measured at 1.9 GHz (losses = 0.27 dB) 2) Measured at 2.4 GHz (losses = 0.36 dB) 3) Measured at 3.5 GHz (losses = 0.50 dB)
Isolation Tx-Rx	ISO_{Tx-Rx}	34.2[4)] 39.7[5)] 22.7[6)]	30.3[4)] 39.2[5)] 19.6[6)]	30.2[4)] 39.9[5)] 20.8[6)]	dB	4) Measured at 1.9 GHz 5) Measured at 2.4 GHz 6) Measured at 3.5 GHz
Isolation ANT-Tx	ISO_{ANT-Tx}	34.1[4)] 40.2[5)] 22.1[6)]	30.3[4)] 39.8[5)] 18.8[6)]	29.7[4)] 39.3[5)] 19.6[6)]	dB	
Input third order intercept point	IIP_3	>45	>45	>45	dBm	Measured at P_{IN} = 5 dBm
Third order intermodulation distortion	IMD3	>85	>85	>85	dBc	

4.2.2 Schematic

The following figure shows the schematic of the SPDT series and shunt switch. In the schematic, each branch of the switch contains one series- and one shunt-connected PIN diode. The resistors R2 and R3 are used to set the bias current for series-connected diodes in branches one and two of the switch respectively, while the resistors R1 and R4 are used to set the bias current for shunt-connected diodes in each branch. The inductors L2 and L5 provide the DC return path for the bias current of the series-connected diodes. The capacitors C3, C5, C6 and C9 serve as the RF bypass. The capacitors C4 and C7 provide the DC block and the matching at the common input port. The matching network at output port one is formed by the capacitors C1 and C2 and the inductor L2. The matching network at output two is formed by the capacitors C8 and C10 and the inductor L5.

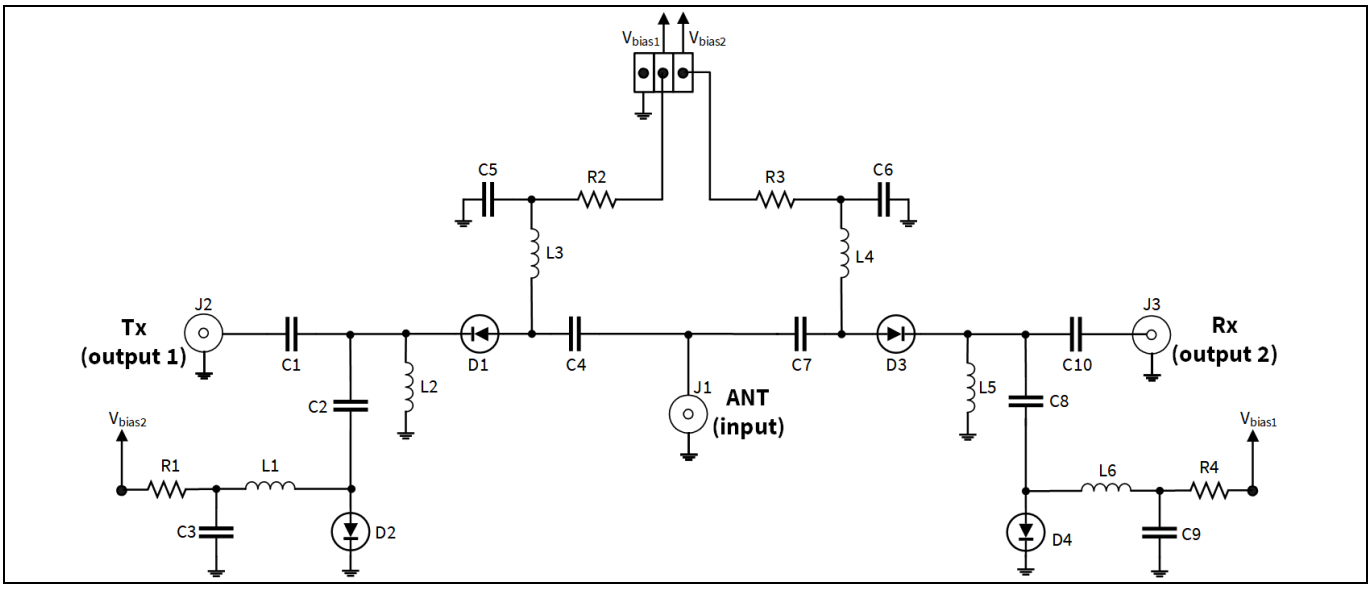

Figure 42 The SPDT series and shunt switch schematic

4.2.3 BOM

Table 17 BOM of the SPDT series and shunt switch circuits with BAR50-02V, BAR64-02V and BAR90-02EL

Symbol	Value			Unit	Size	Manufacturer	Comment
D1 – D4	BAR50-02V (SC79)	BAR64-02V (SC79)	BAR90-02EL (TSLP-2)	–	–	Infineon	PIN diode
C1	6.8	3.3	2.7	pF	0402	Various	DC block and Tx matching
C2	2.2	2.2	2.2	pF	0402	Various	DC block and Tx matching
C3	220	220	220	nF	0402	Various	RF bypass
C4	6.8	3.3	2.7	pF	0402	Various	DC block and input matching
C5	220	220	220	nF	0402	Various	RF bypass
C6	220	220	220	nF	0402	Various	RF bypass
C7	6.8	3.3	2.7	pF	0402	Various	DC block and input matching
C8	2.2	2.2	2.2	pF	0402	Various	DC block and Rx matching
C9	220	220	220	nF	0402	Various	RF bypass
C10	6.8	3.3	2.7	pF	0402	Various	DC block and Rx matching
L1	68	68	68	nH	0402	Murata LQW	RF choke
L2	68	6.8	6.8	nH	0402	Various	DC return, Tx branch

PIN diode SPDT series and shunt switches

Symbol	Value			Unit	Size	Manufacturer	Comment
L3	68	6.8	6.8	nH	0402	Various	RF choke
L4	68	6.8	6.8	nH	0402	Various	RF choke
L5	68	6.8	6.8	nH	0402	Various	DC return, Rx branch
L6	68	68	68	nH	0402	Murata LQW	RF choke
R1	560	560	560	Ω	0402	Various	DC bias
R2	560	560	560	Ω	0402	Various	DC bias
R3	560	560	560	Ω	0402	Various	DC bias
R4	560	560	560	Ω	0402	Various	DC bias

4.2.4 Evaluation board and layout information

The evaluation board information for the SPDT series and shunt switch circuit with BAR50-02V, BAR64-02V and BAR90-02EL:

- PCB material: FR4
- PCB marking: M180629 RF Diode 4

Images of the evaluation board and the PCB stack information are shown in the following figures.

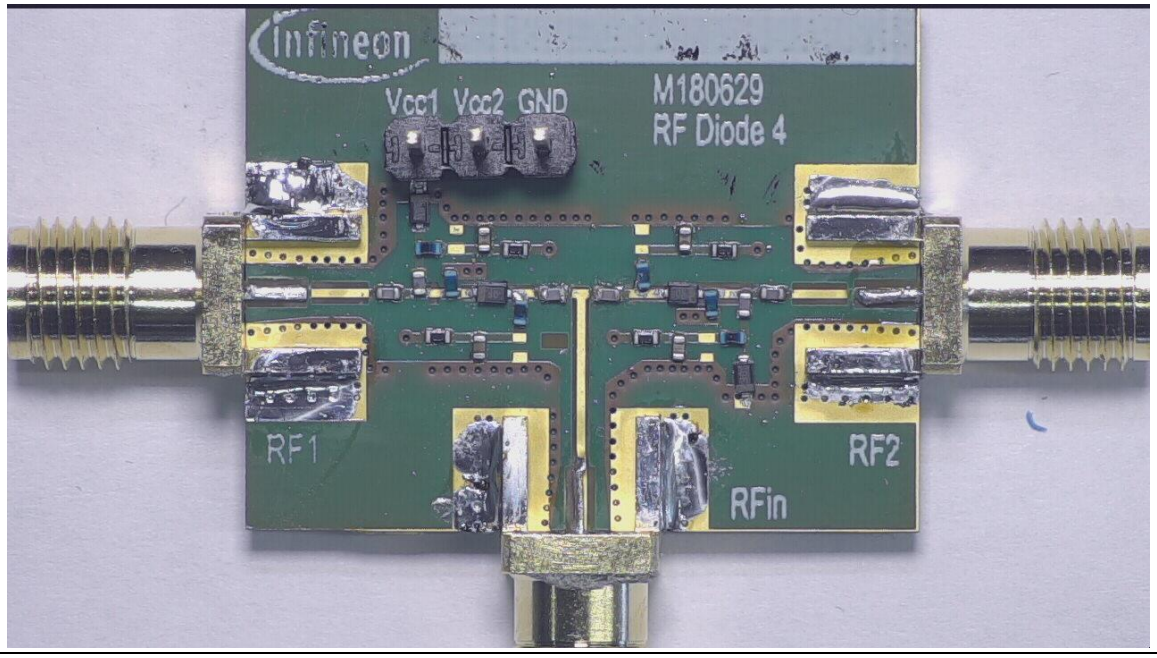

Figure 43 Photo of the evaluation board for the PIN diode SPDT series and shunt switch with BAR50-02V, BAR64-02V and BAR90-02EL

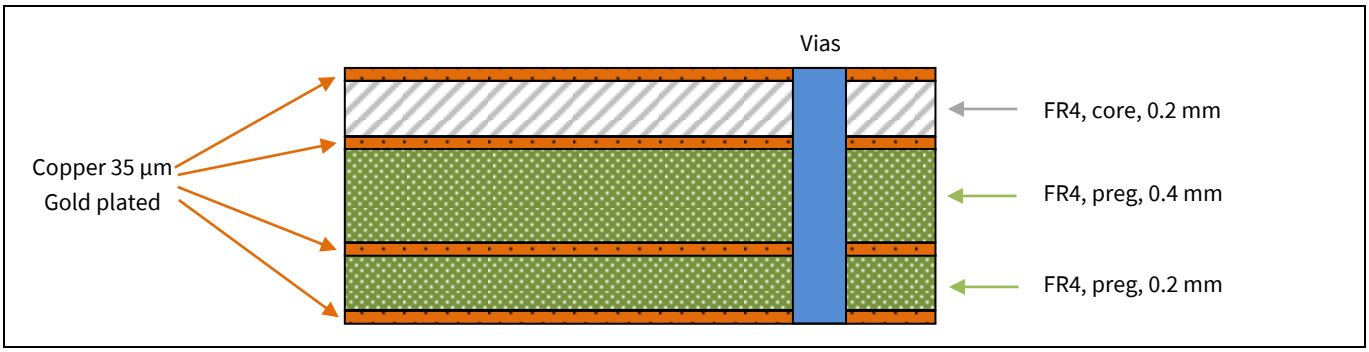

Figure 44 PCB stack information of the evaluation board for the PIN diode SPDT switch

4.2.5 Measurement graphs

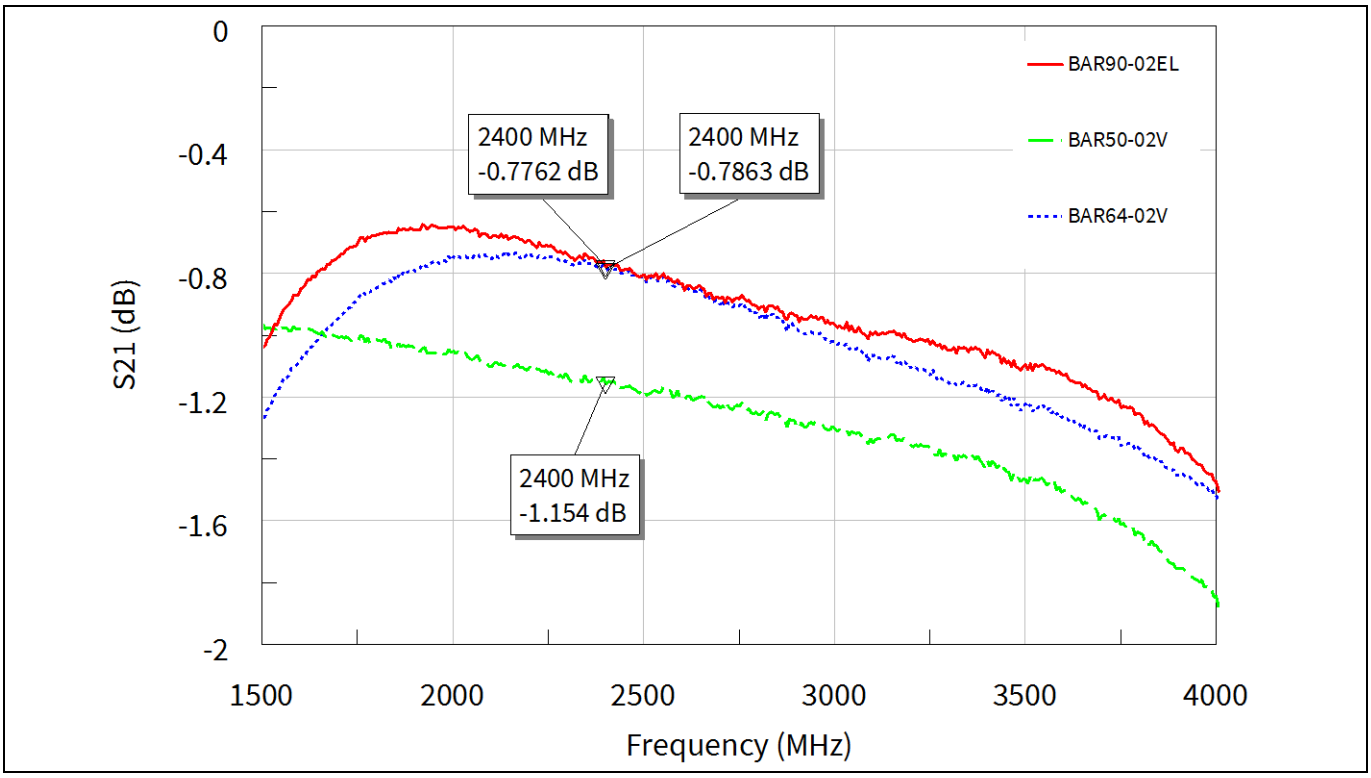

Figure 45 Insertion loss of the SPDT series and shunt switch with BAR50-02V, BAR64-02V and BAR90-02EL in ANT-Tx mode (I_{bias1} = 10 mA)

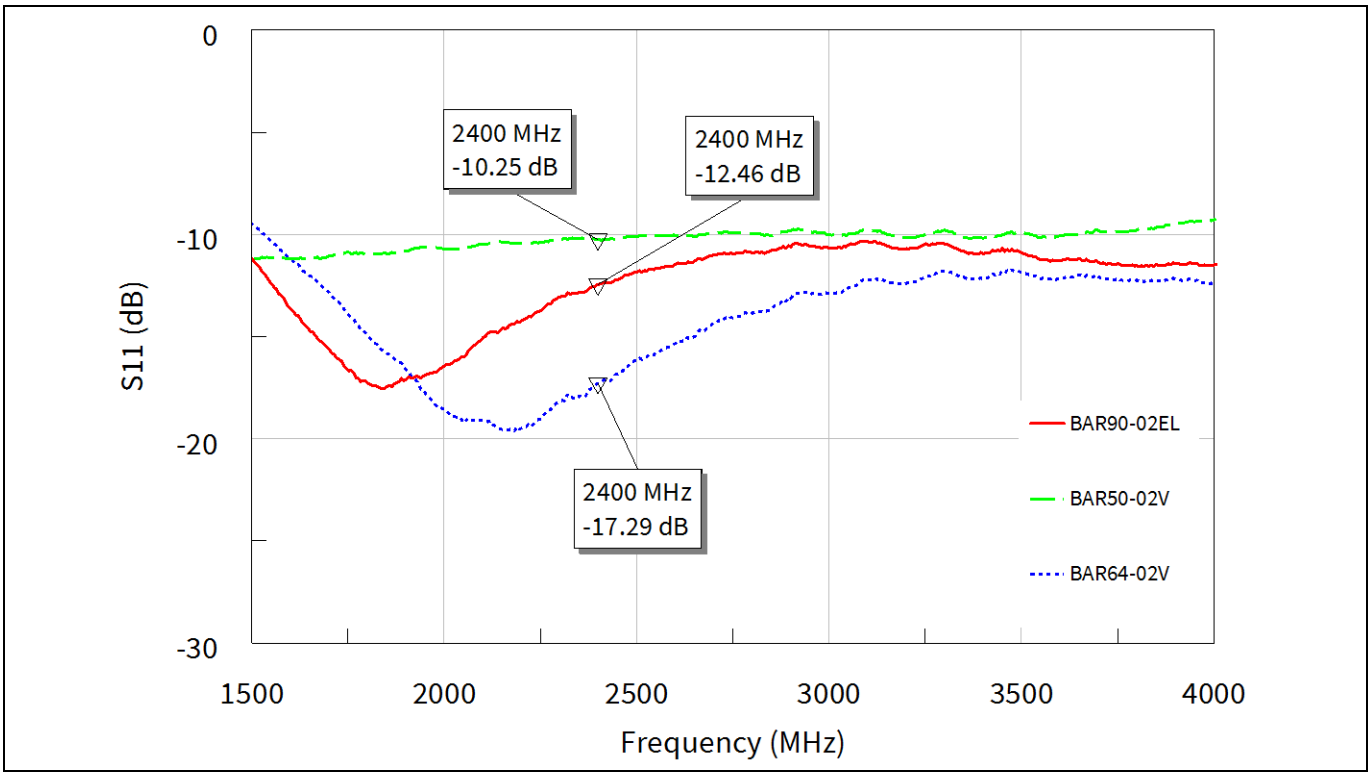

Figure 46 Input return loss of the SPDT series and shunt switch with BAR50-02V, BAR64-02V and BAR90-02EL in ANT-Tx mode (I_{bias1} = 10 mA)

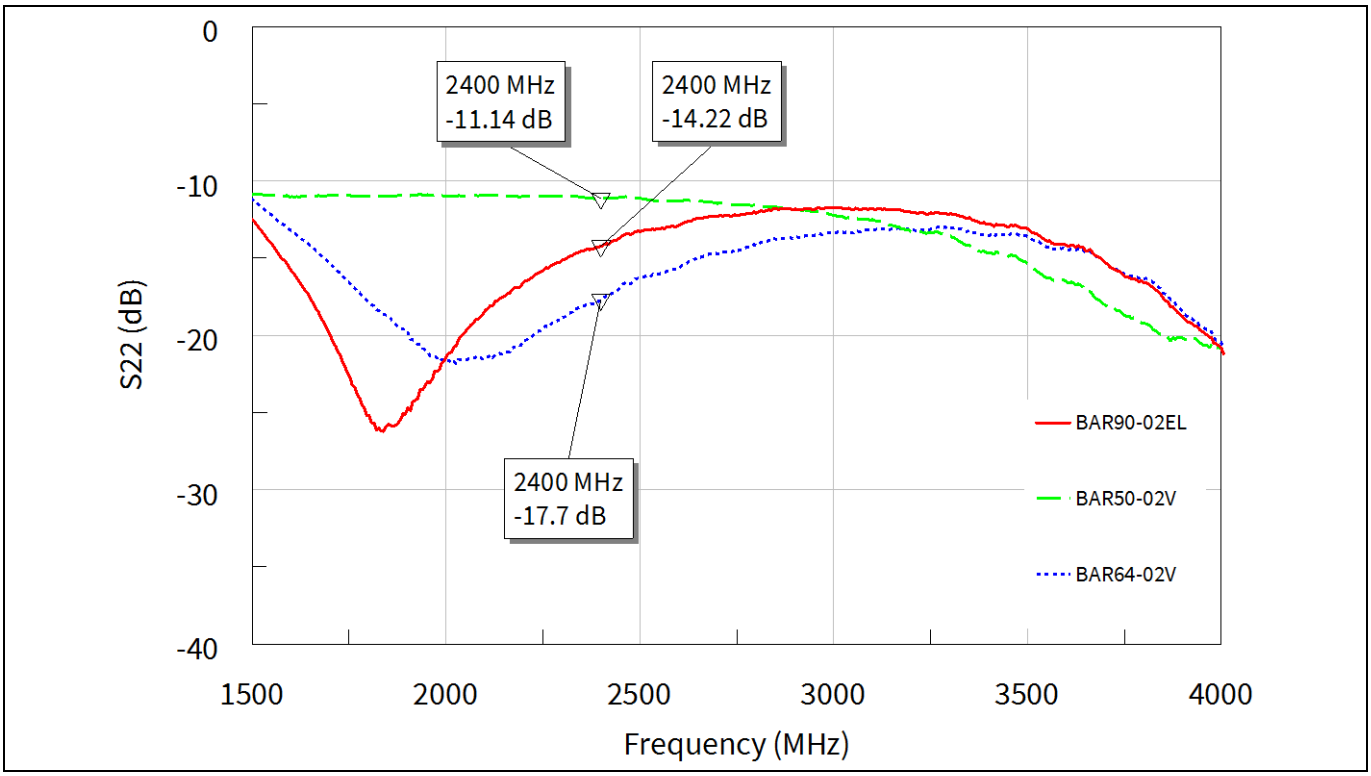

Figure 47 Output return loss of the SPDT series and shunt switch with BAR50-02V, BAR64-02V and BAR90-02EL in ANT-Tx mode (I_{bias1} = 10 mA)

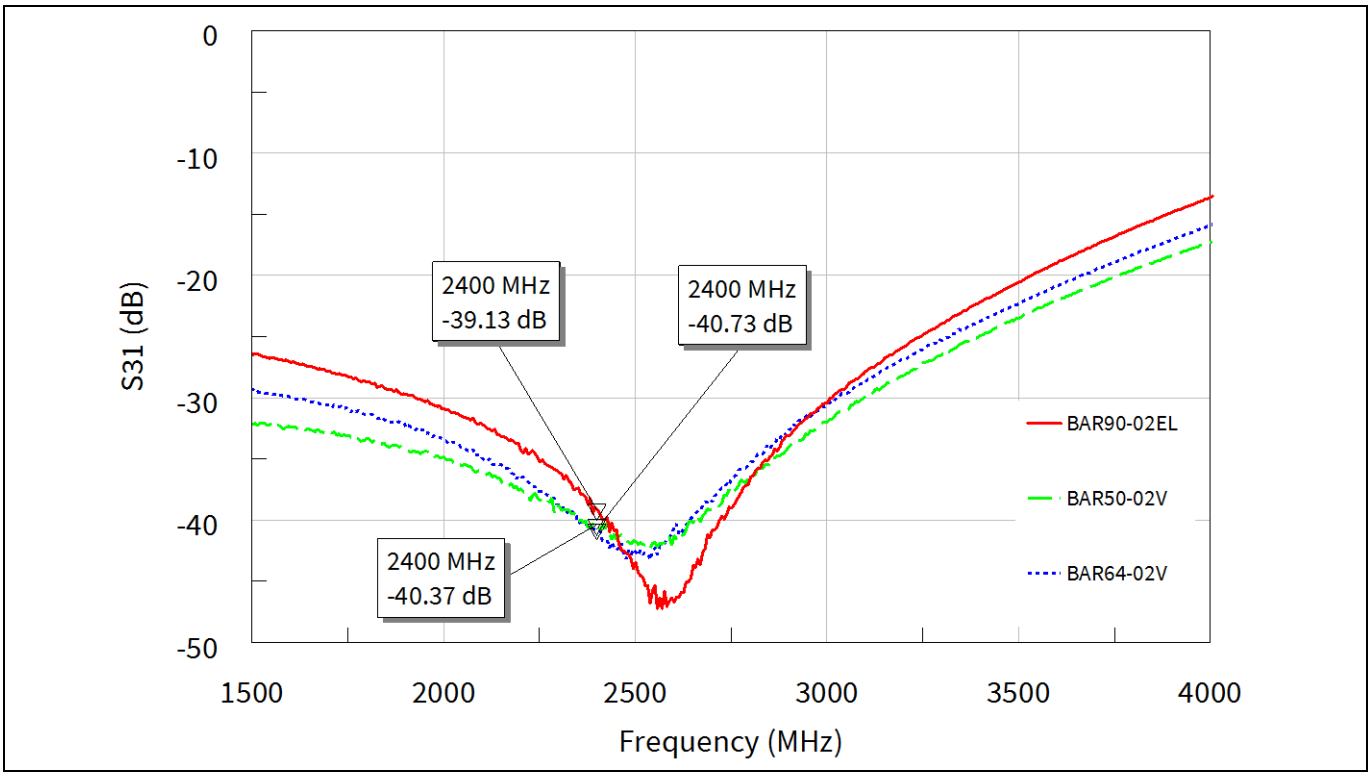

Figure 48 ANT-R_x isolation of the SPDT series and shunt switch with BAR50-02V, BAR64-02V and BAR90-02EL in ANT-Tx mode (I_{bias1} = 10 mA)

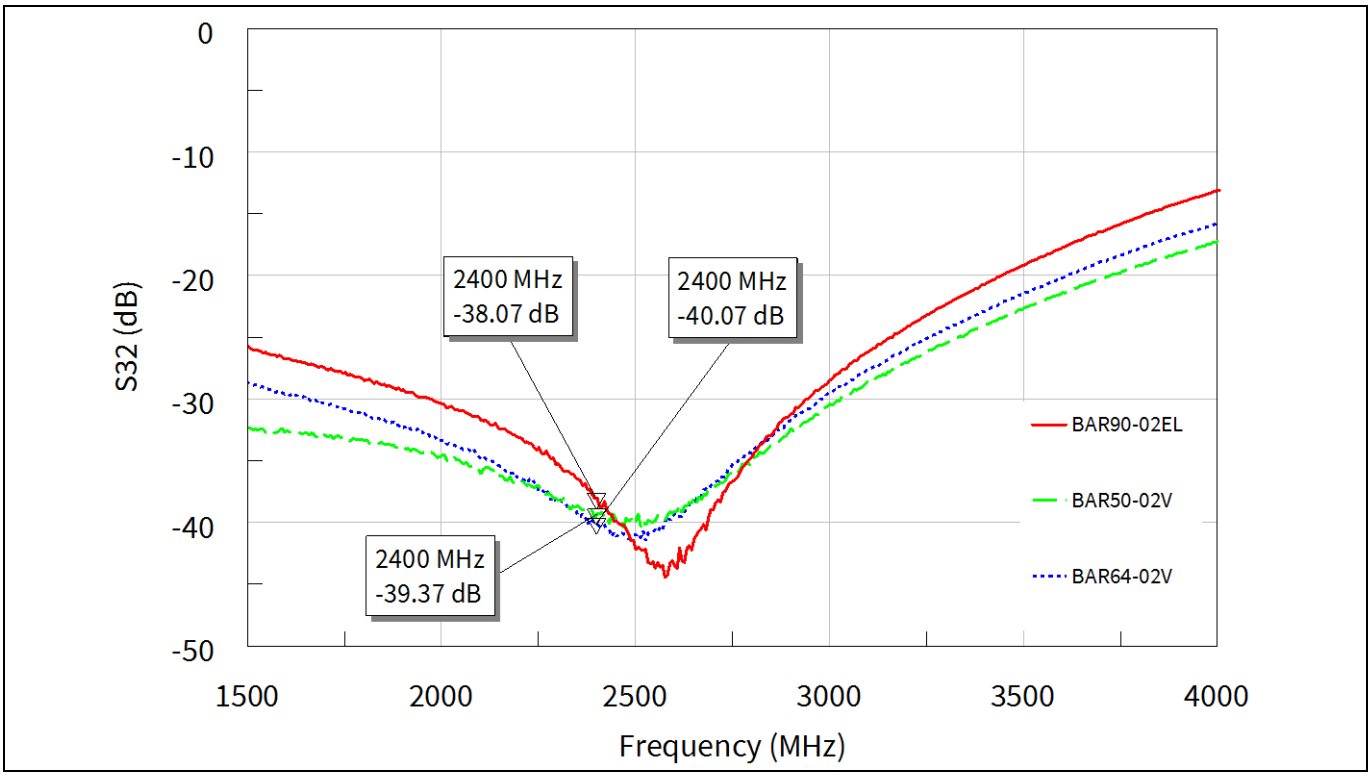

Figure 49 Tx-Rx isolation of the SPDT series and shunt switch with BAR50-02V, BAR64-02V and BAR90-02EL in ANT-Tx mode (I_{bias1} = 10 mA)

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