FOUR SECRETS TO

Mastering Millimeter-Wave Communications Circuit Design

KEYSIGHT
TECHNOLOGIES

INTRODUCTION

Millimeter-Wave Frequencies Meet Broadband Data

Keysight has seen dramatic changes in mobile network devices and infrastructure design, development, and deployment in the transition from 4G to 5G. One substantial challenge affecting circuit design is frequencies extending into the 70 GHz millimeter-wave (mmWave) band. High millimeter-wave frequencies and the drive towards miniaturization directly impact the design of the circuits and systems.

These design trends increase the density and complexity of system integration because they include mixed fabrication technologies and phased array antennas in RF modules. Engineers must assemble multi-technology structures and perform the circuit, electromagnetic (EM), and electrothermal analysis across technology boundaries.

Sophisticated digital modulation schemes are enabling millimeter-wave broadband data transmission. This process impacts the design of components and systems because it now requires new figures of merit like error vector magnitude (EVM) for RF, microwave, and mmWave applications. Your existing RF and microwave electronic design automation tool may not fulfill these new critical requirements to assemble, simulate, and verify multi-technology RF modules.

In this eBook, you will learn four EDA secrets to mastering mmWave communications circuit design and how to streamline your design workflow to achieve first-pass success. We will cover assembly and EM /circuit co-simulation of RF modules, designing for digitally modulated RF signals, and guaranteeing nonlinear amplifier stability modulated in a multi-technology 3D structure.

Contents

SECRET 1

Packaging for Multi-Technology mmWave Designs

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Packaging for Multi-Technology mmWave Designs

Challenge: packaging for multi-technology mmwave designs

The move to mmWave frequencies is the single most significant technology driver impacting multi-technology multilayer assembly. The higher the frequency, the more data you can transmit. 5G applications are creating a massive demand for high throughput instant data, as shown in Figure 1. Higher frequencies have a perilous impact on the circuit design, as the circuit interconnects operate on the same frequency wavelengths as the circuit. Once the physical interconnect is about the size of the operating frequency wavelength, the circuit starts radiating, causing coupling and other interference within an integrated package. It is important for the packaging and assembly to be as small as possible to minimize undesired electromagnetic effects. Choosing the right assembly and packaging is critical.

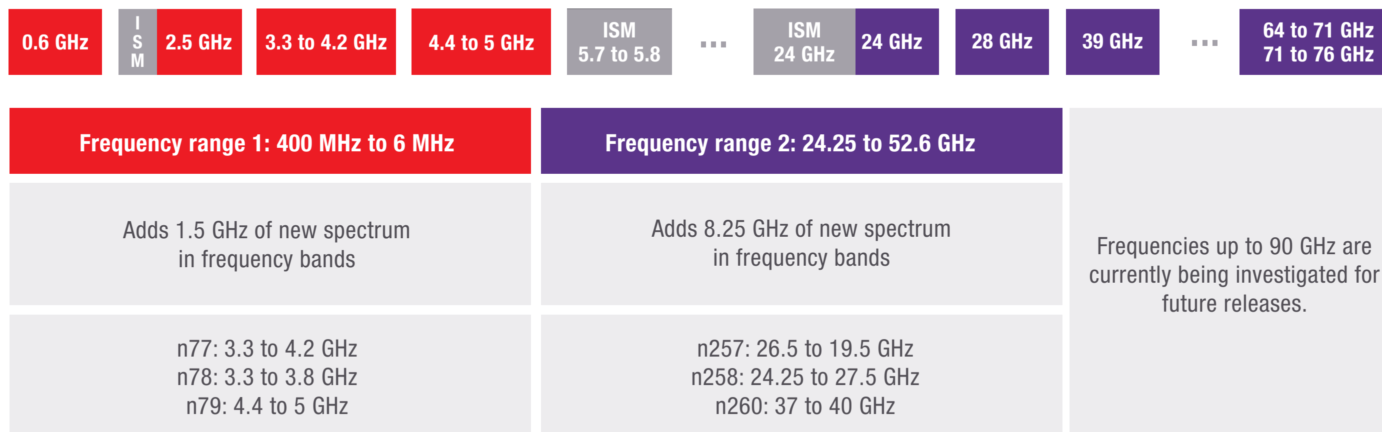

Figure 1. 5G FR2 range is increasing design integration density for future designs

Solution: multi-technology assembly packaging

Choosing the packaging is at the top of the list for integrating a 3D multi-technology assembly. RF modules operating at microwave and mmWave frequencies require low loss, low parasitic interconnects, and packaging. Assembly of complex multi-technology RF modules, or stacking technologies, also accommodates stacked and flipped chips with different technology layer mappings.

Wafer-level packaging (WLP) is a solution for this challenge because it eliminates the use of wire bonds and enables the integration of multiple chips. One version, fan-out wafer-level packaging (FOWLP), replaces traditional wire bonds between the chip and package with a wafer-level redistribution layer (RDL) interconnects, improving isolation, reducing loss, and parasitics shown in Figure 2.

Another consideration when stacking and assembling mixed technologies is design traceability back to the original design databases.

Stacking methods can vary. The designer can use an integrated circuit (IC) and stack, flip, embed into a cavity, or place adjacent to another IC. The assembly must be error-free and efficient to fit into the circuit design process without additional complex steps.

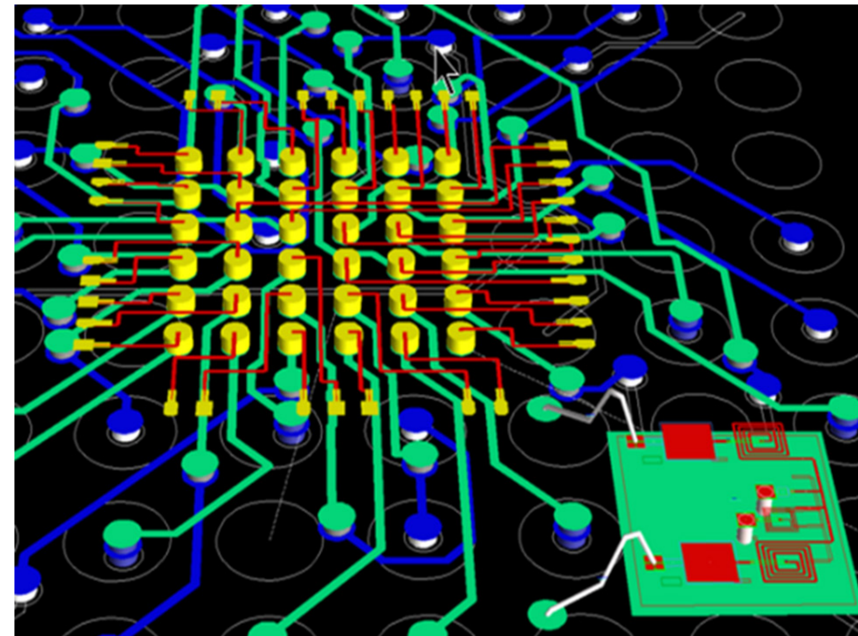

Figure 2. FOWLP packaging with wafer-level redistribution layer interconnects

TECHNICAL BRIEF

RF Module Fan-Out Wafer Level Packaging

Intelligent wafer-level assembly and packaging

Keysight's PathWave advanced design system (ADS) and SmartMount enables a component designed in one technology to work in another technology. The PathWave ADS layout automatically maps the chip technology onto the module technology when placing a SmartMount component (chip) in a top-level design (module).

Unlike other alternatives, which require blending all substrates together in one primary substrate, SmartMount preserves the original substrate integrity without the need for design modification or updates. Figure 3 shows the simplicity of making modifications or adjustments on one IC without having to redo the export and assembly.

Pro Tips

- Create the design, assembly, and 3D EM circuit co-simulation easily, efficiently, and error-free with the Keysight PathWave RFPro design tool.
- Assemble custom mount configurations without having to modify layer mappings or substrate definitions of the assembled components.
- Set up and auto-extract RF electrical nets and components with the Keysight PathWave RFPro design tool.

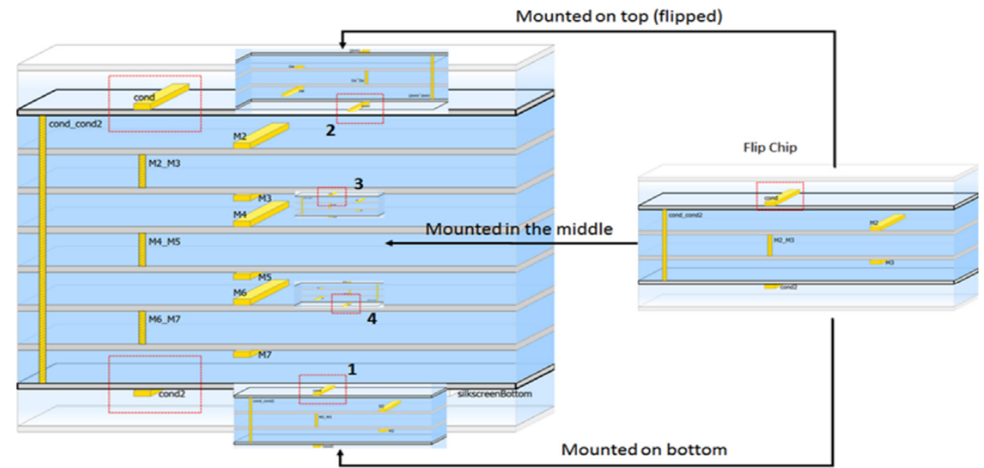

Figure 3. PathWave ADS and SmartMount simplifies multilayer designs and provides traceability for design databases back to the original sources

VIDEO

Layout and Assembly in PathWave ADS

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Designing Wafer-Level RF Chip-Scale Packaging

SECRET 2

Electromagnetic / Circuit Co-Simulation

SECRET 2

Electromagnetic / Circuit Co-Simulation

Challenge: design to account for electromagnetic effects

Dense product functionality in the smallest possible package is the driver for a multi-technology assembly. Figure 4 is an example of mixed microwave and mmWave technologies that include integrating monolithic microwave integrated circuit (MMIC), radio frequency integrated circuit (RFIC), laminate, and antennas together in a compact form factor. The challenge is when the wavelength of the propagating microwave signal is the same wavelength of the interconnect transporting them. This issue causes unwanted electromagnetic (EM) side effects that degrade circuit performance in the form of loss, coupling, and frequency shifts.

Circuit layout and simulation are the first steps in a traditional design flow. A separate EM solver assesses the EM effects as a final step in design validation. The coupling of millimeter-wave frequencies introduces parasitic EM effects, and the design requires updates to include these changes.

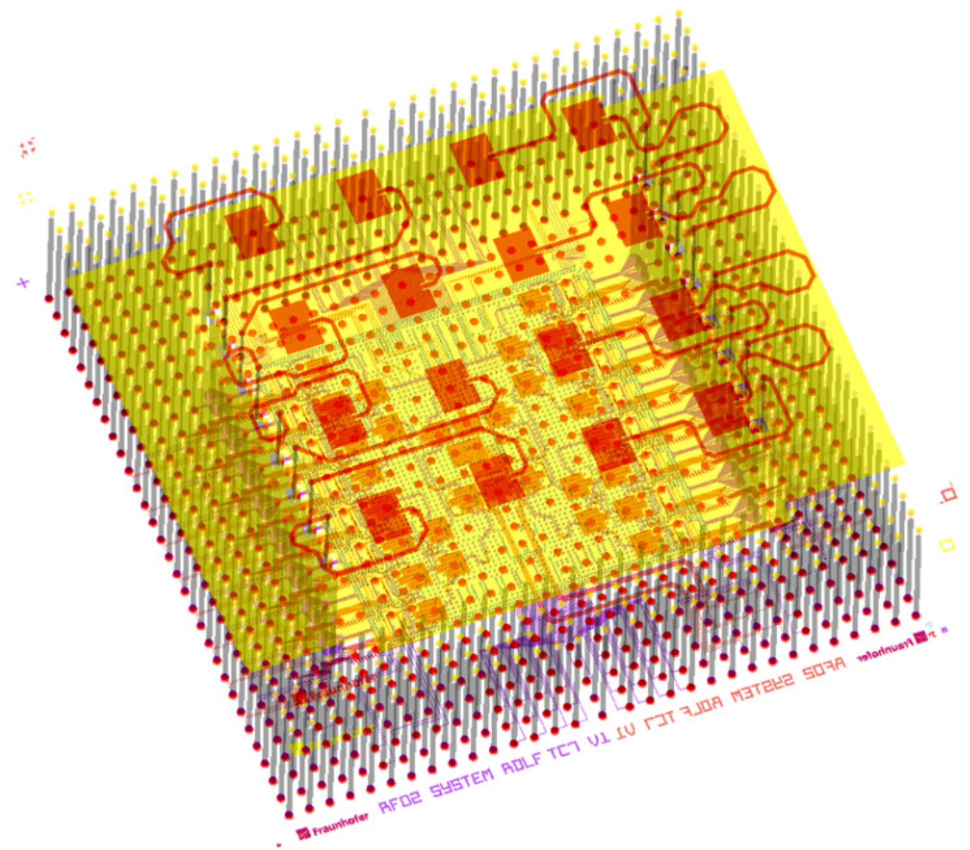

Figure 4

Separate EM / circuit simulation

The interaction between separate circuit simulation and EM simulation tools is complex. Let's look into why this is a lengthy process by following the process flow in Figure 5:

1. Modifying the circuit design using a separate electromagnetic simulator removes the circuit components because the tool does not have a disposition process.

2. At the end of the EM simulation process, the electromagnetic simulator produces a multiport S-parameter file, and the number of ports can number in the hundreds.

3. Each port must now reconnect manually back to the circuit nodes for simulation in a circuit simulator.

Incorrectly connecting one port to one circuit node out of the hundreds of ports that must reconnect to the correct circuit node invalidates the EM / circuit co-simulation results. This additional export / import manual process can take up to two weeks and may introduce errors that cause hardware failures downstream in the design.

Circuit designers need to iteratively include 3D EM effects of packaging and interconnections during design exploration, tuning, and optimization — not just for final verification of the completed design.

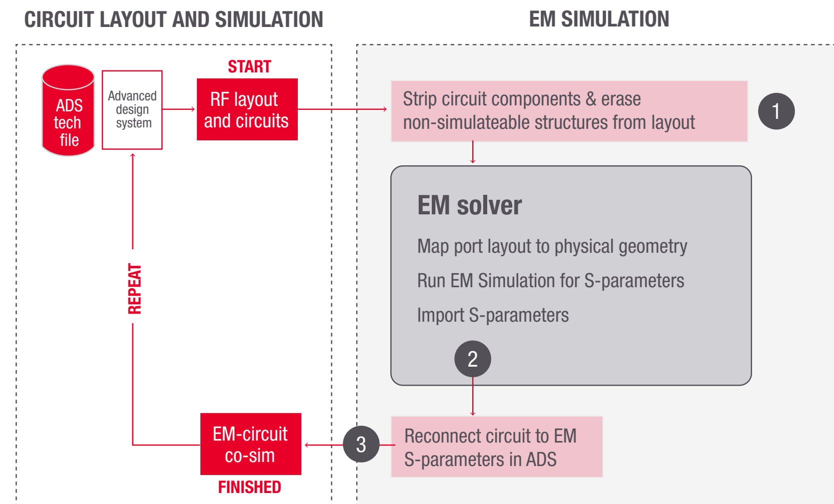

Figure 5. Circuit and EM simulation interaction between two separate software tools

Solution: iterative EM / circuit co-simulation

RFPro in PathWave ADS enables circuit designers to create an electromagnetic system to analyze multi-technology designs with automated setups and configuration. Figures 6 and 7 are examples of how this solution eliminates the delay and potential errors introduced by a separate EM solver. With RFPro integrated into PathWave ADS, a 3D finite element model (FEM) simulation runs automatically in the same environment with easy automated setup and analysis. This process frees the RF circuit designer to perform 3D electromagnetic analysis and EM / circuit co-simulation iteratively in the design phase. This process is without manual setup errors since the electromagnetic analysis uses a separate electromagnetic solver. Figure 7 shows how the 3D EM / circuit co-simulation yields an order of magnitude faster setup giving you time to schedule other test tasks.

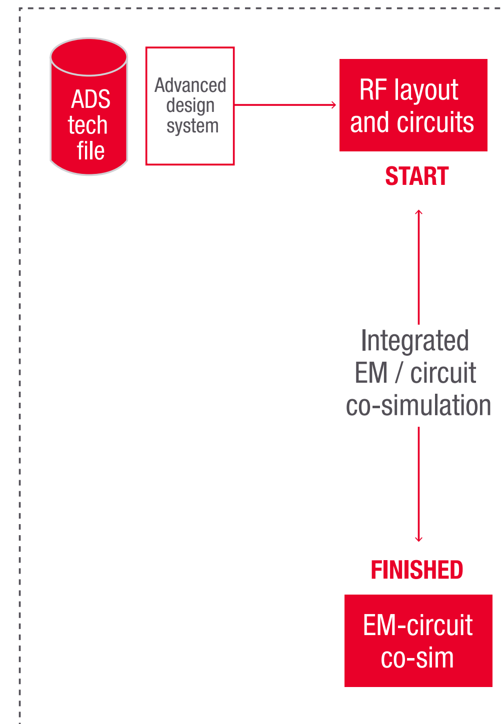

Figure 6. EM / circuit co-simulation integrated workflow

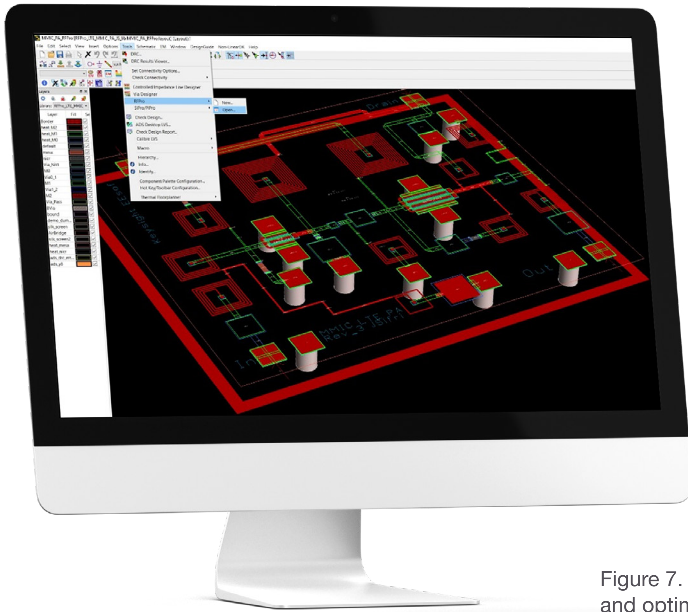

Figure 7. Connection for EM results to circuits is automatic for immediate tuning and optimization to account for EM effects on circuit performance

Pro Tips

- Reduce simulation time and increase accuracy by only modeling what is essential without “cookie cutting” the layout
- Preserve layout integrity by ensuring that the EM simulation performs on multi-technology microwave and millimeter signal paths without cookie cutting

VIDEO

RFPro in ADS for EM-Circuit Co-Simulation Demo Video

KEYSIGHT UNIVERSITY COURSE

Integrated 3D EM-Circuit Co-Simulation for First-Pass Design Win

SECRET 3

Nonlinear Amplifier Stability Analysis

SECRET 3

Nonlinear Amplifier Stability Analysis

Challenge: prevent your amplifier from becoming an oscillator

Using higher frequency transistors complicates the design flow for designing stable circuits. In today's circuits, the gain is higher due to increasing transistor fTs, or the frequency at which unity current gain goes to zero, as shown in Figure 8. The additional gain is necessary at lower frequencies to achieve gain at 30, 60, or 90 GHz. Tight integration along with feedback can cause instability problems at lower frequencies from the significant increases in gain. The undesired output-input feedback is prevalent because circuits are denser and resonate easily with signals that have smaller wavelengths. Electromagnetic (EM) effects such as couplings and reflections can cause instability, especially in today's advanced packaging and assembly approaches.

Figure 9 shows how today's advanced packaging technologies place the circuit structures closer together. The internal circuitry is less accessible, and problems are difficult to resolve later in the lab. High-frequency designers need to master stability by understanding the root causes early in the development process and incorporating this knowledge into all design aspects. Solving stability problems upfront in the design phase is especially critical when designing a high-frequency circuit packaged in compact structures.

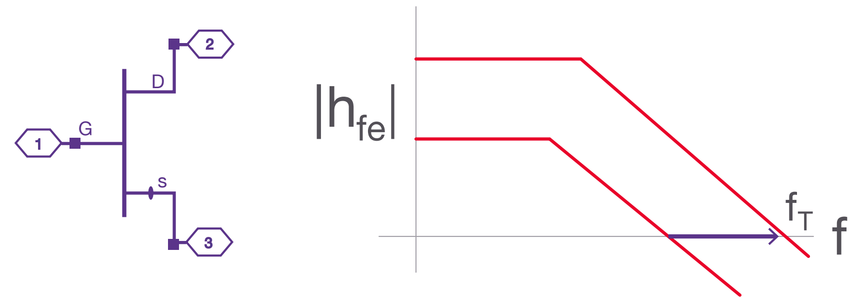

Figure 8. High transistor gain

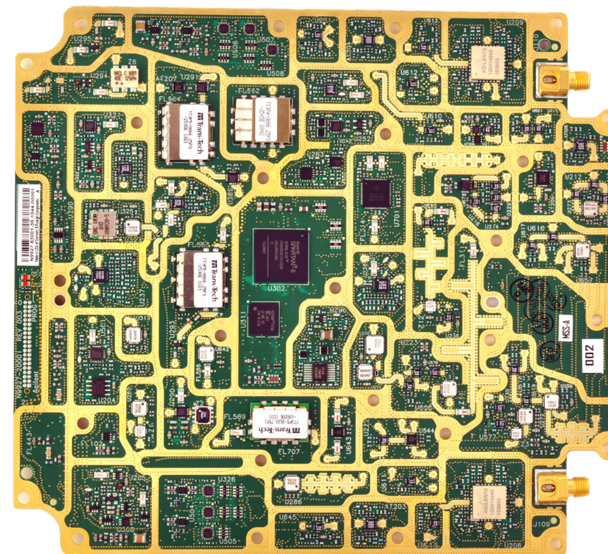

Figure 9. Board-level integration in a signal analyzer

Challenge: modeling amplifier instability

Amplifier designers want to extensively test an amplifier in the design stage to know whether the design is stable under all loading conditions such as linear, nonlinear, small-signal, and large-signal. It is challenging to know which stability analysis approach to use — all have their strengths and weaknesses.

There are as many as 14 simulation approaches and techniques to derive the figure of merit. To learn more about the background of these 14 approaches, read the Keysight application note Designing for Stability in High-Frequency Circuits. Figure 10 is an example of four simulation approaches using an amplifier and a feedback network.

Each approach requires a different kind of setup and stimulus condition to get the answer. What do you do next if you try these four different approaches and receive conflicting results? You need a comprehensive method to run all of the 14 simulation approaches at once. Only then can you confidently identify the source for the instability and begin making circuit-level changes.

APPLICATION NOTE

Designing for Stability in High-Frequency Circuits Application Note

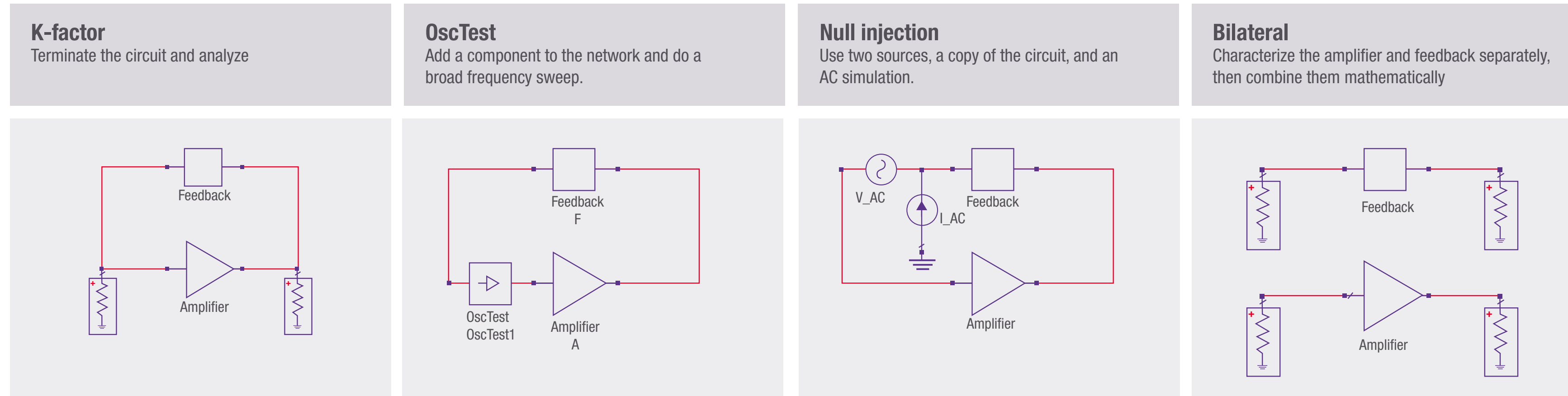

Figure 10. Four different traditional test setups to evaluate an amplifier for stability

Solution: comprehensive stability analysis

The Keysight Winslow stability probe (WS-probe) is an in-circuit probe that replaces the traditional setups for multi-device amplifiers to derive the necessary stability measures quickly and efficiently. Figure 11 shows how WS-probes connect to the input and output of the amplifier model.

The WS-probe detects loop gain, return difference, and other observable behavior in the feedback network for stability analysis. These probe additions allow the application of multiple stability analysis techniques to the circuit post-simulation for both small and large signal analysis without disturbing or altering the fundamental analysis.

The WS-probe accurately outputs bidirectional impedances, even under high levels of feedback. Figure 12 shows how this probe mathematically derives all the stability metrics in post-process from one simple setup, eliminating the need for dozens of additional simulations.

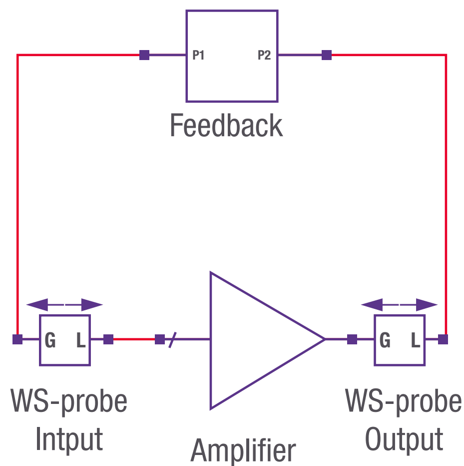

Figure 11. Winslow probes inserted into the circuit post-simulation

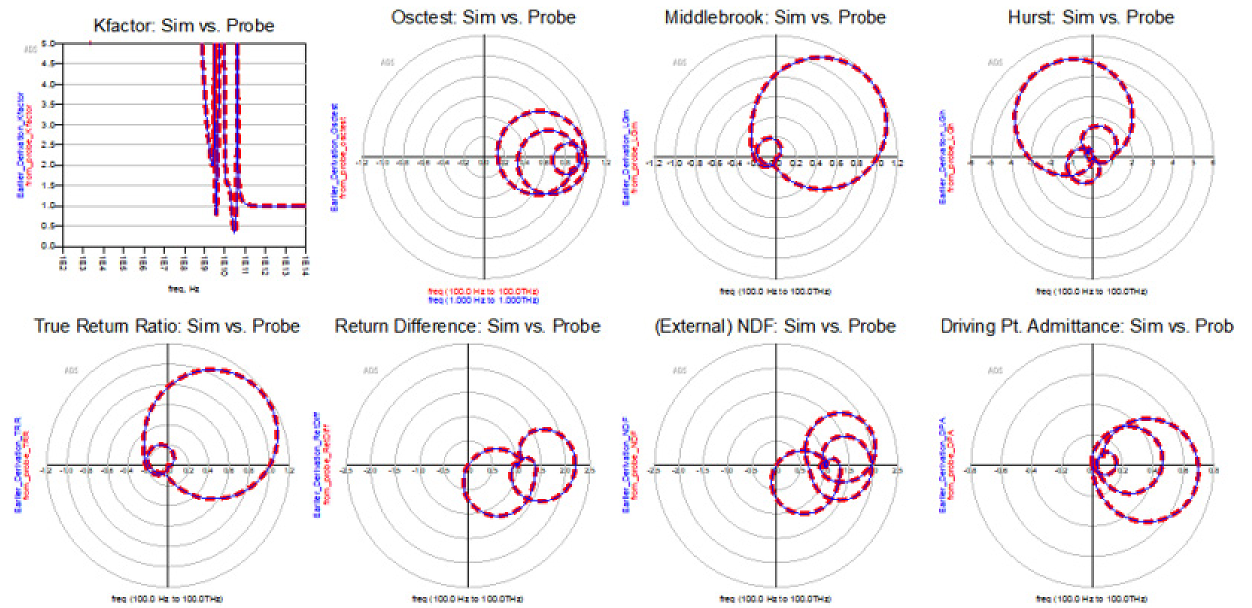

Figure 12. One simulation that applies multiple stability analysis techniques to the circuit post-simulation for both small and large signal analysis.

Pro Tip

A simple, foolproof approach for detecting instabilities in a design is to:

- Place a WS-probe in the advanced design system (ADS) at all active terminals in the design.
- Run an S-parameter or harmonic balance simulation.
- Use the wsp_unstable_freq_kuokawa() function in the data display to review a list of the unstable frequencies to pinpoint what to change.

VIDEO

Stability Analysis in ADS Demo Video

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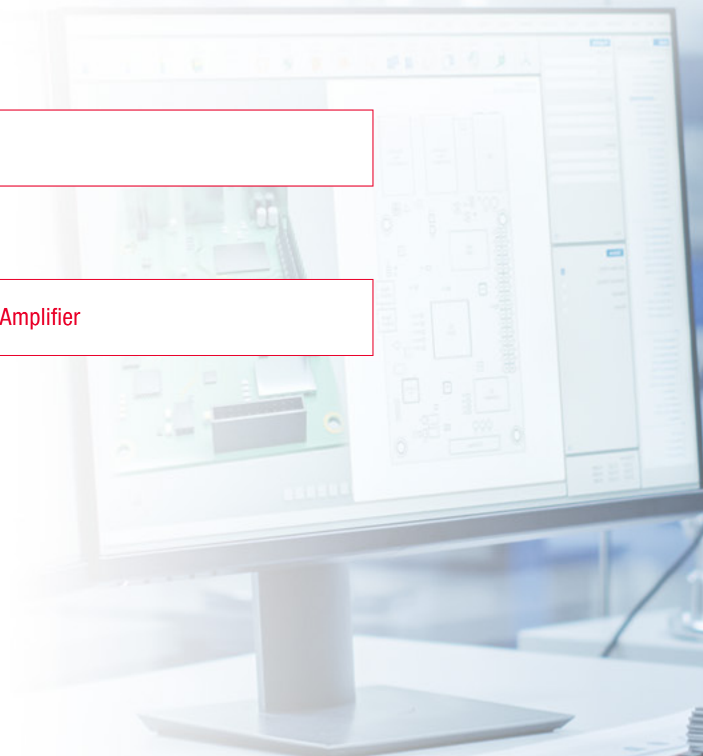
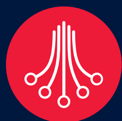
How to Design a Stable High-Frequency Amplifier





SECRET 4

Designing Circuits with Digitally Modulated Signals

SECRET 4

Designing Circuits with Digitally Modulated Signals

Challenge: error vector magnitude at the circuit level

Figure 13 shows digitally modulated RF signals require new figures of merit for circuit design and optimization, the most important of which is error vector magnitude (EVM). Traditional analog measures such as P1dB and IP3 rely on instruments that were adequate for 3G and marginally adequate for 4G. Using analog measurements can create circuits that are off-specification or over-designed circuits for 5G digitally modulated signals.

Measuring EVM can have its challenges — the first task is to determine measurement speed. Distortion EVM estimates the error vector magnitude of nonlinear simulations without the need for an external system simulator. Distortion EVM can help designers quickly assess the EVM during the design phase and speed up simulation time by a factor of 10. Figure 14 shows how the distortion EVM algorithm can compute EVM without the need to demodulate the signal.

The second task requires accurately generating a representative 5G test signal waveform that approximates the signal characteristics. If you can find an accurate representative waveform, you still need to demodulate or demultiplex the signals to arrive at the error vector magnitude. Using these test signals together with distortion EVM measurements shortens the test time for quick verification in circuit design.

EBOOK

Top Considerations for 5G New Radio Device Designers

Modulation scheme for PDSCH	Required EVM
QPSK	17.5 %
16QAM	12.5 %)
64QAM	8 %
256QAM	3.5 %

Figure 13. EVM requirements for different 5G modulation types

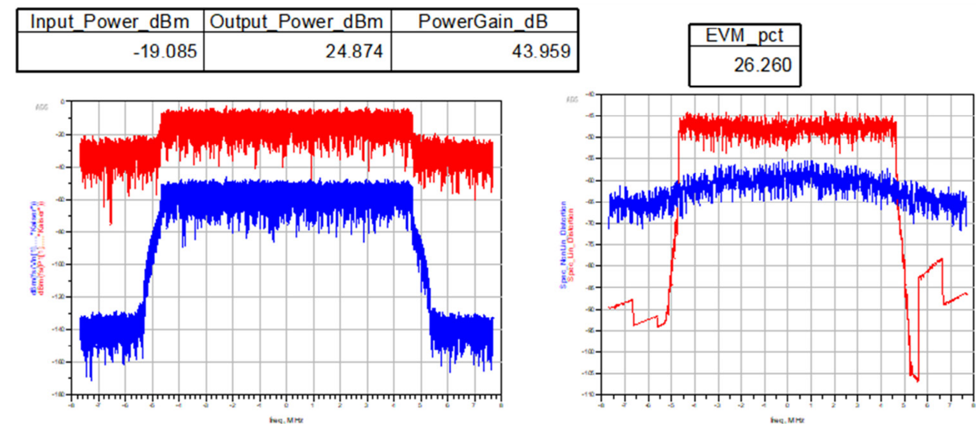


Figure 14. Results of automated distortion EVM measurements

Solution: A Compact Test Signal

The compact test signal (CTS) shortens the test time for quick verification in circuit design. CTS uses a time slice from the overall 5G modulated waveform, representing the same frequency signature and statistical complementary cumulative distribution function (CCDF) as the sampled source signal. You can use the CTS while iterating your circuit designs to obtain a good proxy for EVM performance, as shown in Figure 15.

The CTS provides EVM results quickly so the designer can tweak, tune, and optimize their circuit design. The main advantage of the CTS is an order of magnitude faster simulation speed.

VIDEO

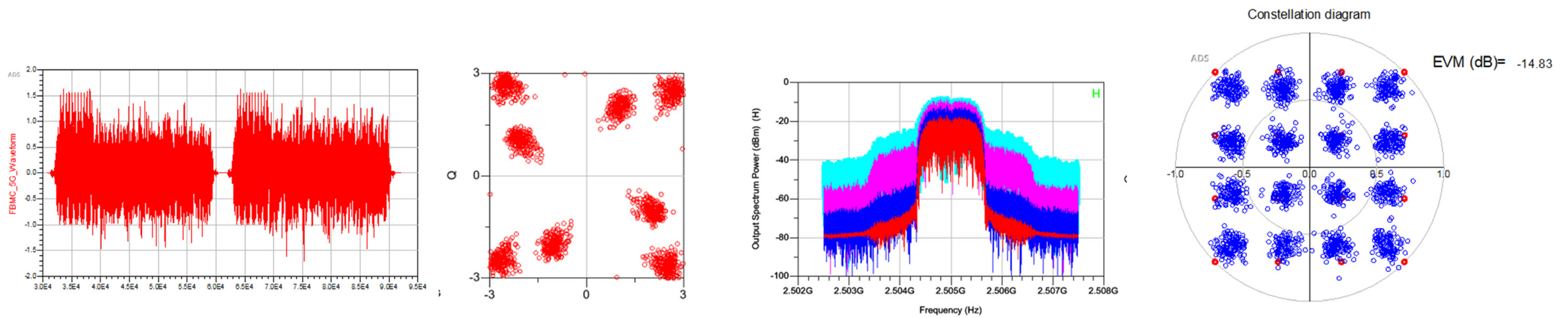


Figure 15. The compact test signal and EVM measurements provide a quick verification of your circuit design

Solution: use 5G industry standards for verification

The final step on the path to achieving a design win with your customer is to verify performance for a modulated signal at a system level against 5G wireless standards. Keysight's PathWave ADS offers 5G standards-based wireless sources and demodulation algorithms derived from Keysight RF instrumentation in a preconfigured verification test bench (VTB). Using a preconfigured VTB eliminates the complicated setup of 5G and other compliance tests, as shown in Figure 16. Using the verification test bench enables accurate verification of RF component designs before building your hardware for 5G. The VTB uses the same highly accurate signal generation and measurements found in Keysight RF instruments.

VIDEO

5GNR Virtual Test Bench for PathWave ADS

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A Cohesive RF Workflow for Designing with Modulated Signals

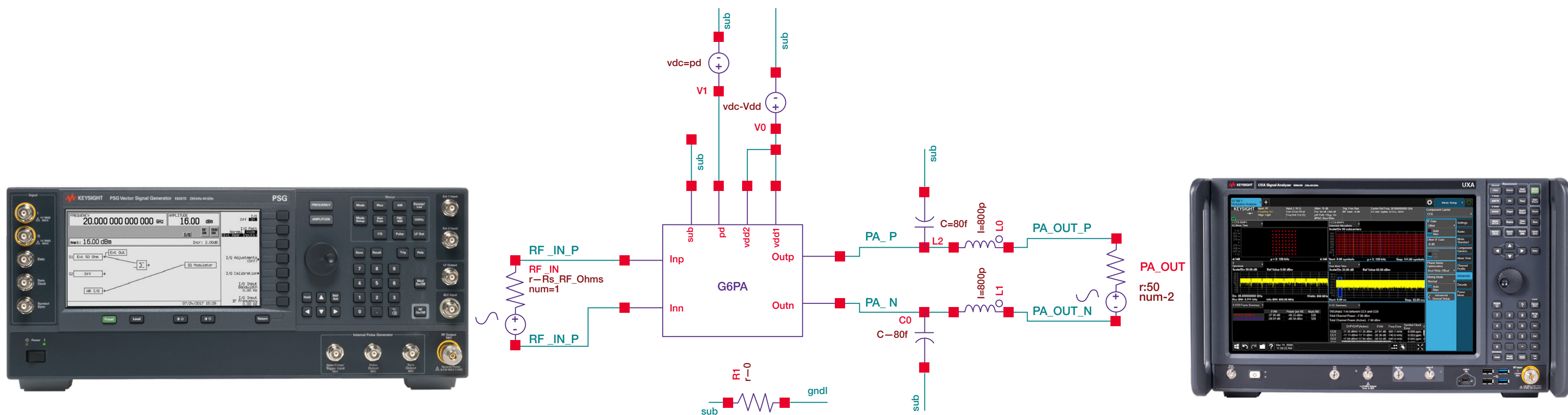

Figure 16. The verification test bench contains pre-configured source and measurement setups using the same Keysight instrument algorithms to verify your design for compliance with 5G standards before building the hardware

SUMMARY

5G millimeter-wave frequency applications have high-density multi-technology integration and complex digital modulation schemes that push the limits of packaging assemblies for EM and circuit simulations. Four of the top RF circuit design challenges for designers are to:

- Assemble and integrate 3D multi-technology RF modules.
- Perform electromagnetic and circuit co-simulation of RF signal paths which is an error-prone and time-consuming process.
- Ensure amplifiers are stable under nonlinear and loading conditions.
- Tune and optimize circuit EVM performance and confirm performance complies with industry 5G standards.

Keysight's PathWave ADS software solution enables 3D layout and assembly for multi-technology RF modules, including RFIC, MMIC, wafer-level packaging, and printed circuit boards (PCBs). The 3D layout avoidance routing and assembly with interactive electromagnetic circuit co-simulation and system analysis accurately accounts for packaging EM effects during the design phase.

The Keysight Winslow probe comprehensively identifies linear / nonlinear amplifier instability to prevent a costly hardware failure. Circuit level EVM analysis and 5G verification test benches enable you to optimize circuit EVM performance for digitally modulated RF signals in compliance with 5G industry standards.

These unique design solutions are examples of how RF EDA technology is evolving to improve the predictability of your RF design process to reduce the complexity of your design cycles. Now is the time to review your RF EDA workflow for these critical challenges and master the four design secrets to help you compete for design wins.

Learn how Keysight solutions can help you with your RF and microwave designs, please visit:

PathWave ADS RFPro, a next generation platform for RF / microwave / millimeter circuit designs.

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