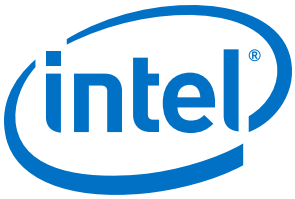

AN 875: Intel® Stratix® 10 E-Tile PCB Design Guidelines

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1. Introduction

The Intel® Stratix® 10 E-Tile PCB design guidelines provided in this document are intended to supplement existing Application Notes on PCB design, and not to provide any contradictory information. Intel recommends that you also read the prerequisite Application Notes listed below:

- AN 766: Intel Stratix 10 Devices, High Speed Signal Interface Layout Design Guideline
- Transceiver Link Design Guidelines for High-Gbps Data Rate Transmission
- PCB Breakout Routing for High-Density Serial Channel Designs Beyond 10 Gbps
- PCB Stackup Design considerations for Intel FPGAs

Note that these design guidelines are not tied to any specific platform, which means:

- These design guidelines do not give specific design parameter values. They only provide examples to illustrate the Signal Integrity (SI) design methodology.
- You have the freedom to choose the optimized materials, stackups, and other elements based on your application needs.

Signal integrity simulations are recommended for the E-Tile platform channel design. You must understand the key points below to reach your simulation targets and achieve an optimal design:

- The design margin for E-Tile channels running at 56 Gbps is much smaller than the margin in the 28 Gbps generation due to the additional -9.5 dB intrinsic loss (1/3 NRZ amplitude).
- Industrial standard organizations like IEEE802.3 already specify the channel checking method Channel Operating Margin (COM) for pass/fail criteria.
- Intel provides the IBIS-AMI model and its user guide for SI simulations with the E-Tile silicon's electrical behavior in your own application systems.

The application note uses 56 Gbps to describe data rates in general because of the baseline established in the Common Electrical Interface (CEI). However, the actual data rate can be up to 57.8 Gbps.

2. Platform Design Strategy for 56G PAM4 Channels

2.1. Intel Stratix 10 E-Tile Transceiver Channel Usage Mode

Intel Stratix 10 E-Tile supports dual-mode PAM4 and NRZ serial transceivers for up to 12 lanes of CEI-56G-LR 56G PAM4 and up to 24 lanes of 28.9G NRZ 802.3-KR/CR. In PAM4 mode, for data rate higher than 40 Gbps, the configuration with the maximum capacity is with every other channel running PAM4 with a maximum data rate of 57.8 Gbps (channels 2n, n=0,1,..11 are for PAM4, channels 2n+1 are unused). Up to 32 Gbps PAM4 can be supported on every channel if all channels are running. In NRZ mode, up to 28.9 Gbps can be supported on every channel if all channels are running.

Figure 1. Intel Stratix 10 E-Tile Transceiver Usage Example: Channels Running at Data Rates > 28.9 Gbps

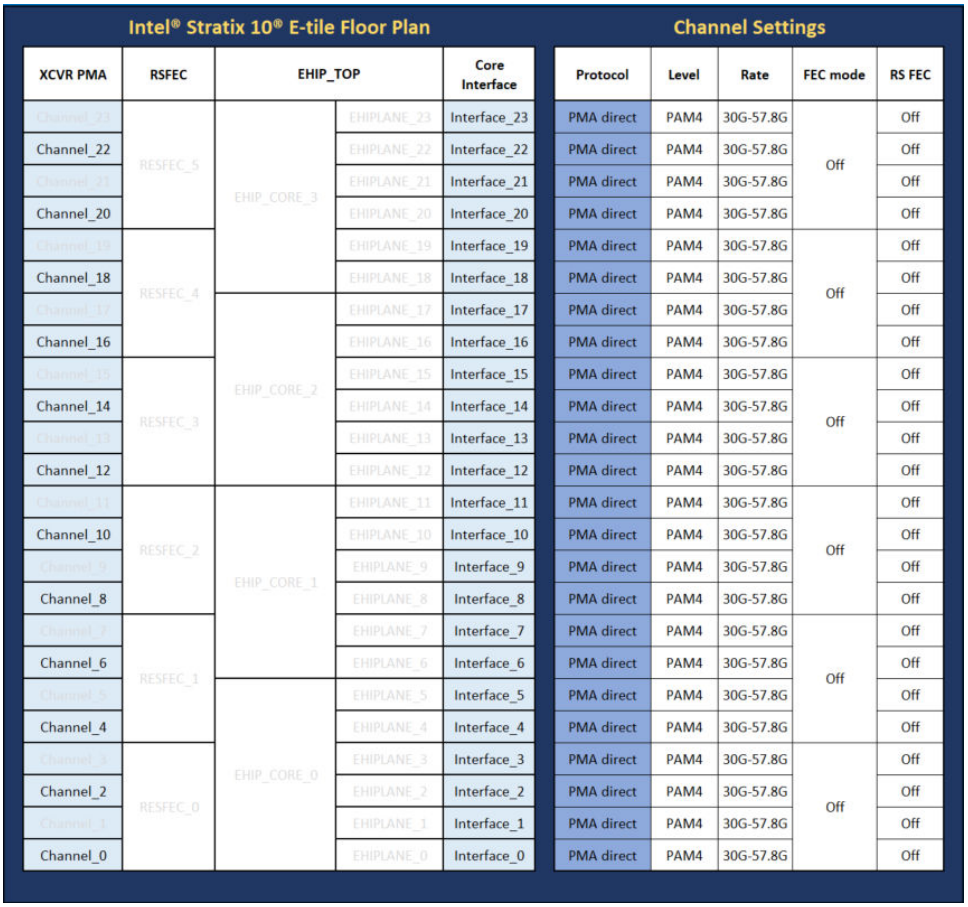


Figure 2. Intel Stratix 10 E-Tile Transceiver Usage Example: Channels Running at Data Rates < 28.9 Gbps

Intel® Stratix 10® E-tile Floor Plan					Channel Settings				
XCVR PMA	RSFEC	EHIP_TOP		Core Interface	Protocol	Level	Rate	FEC mode	RSFEC
Channel_23	RSFEC_5	EHIP_CORE_3	EHIPLANE_23	Interface_23	PMA direct	PAM4low	2G-30G	Off	Off
Channel_22			EHIPLANE_22	Interface_22	PMA direct	PAM4low	2G-30G		Off
Channel_21			EHIPLANE_21	Interface_21	PMA direct	PAM4low	2G-30G		Off
Channel_20			EHIPLANE_20	Interface_20	PMA direct	PAM4low	2G-30G		Off
Channel_19	RSFEC_4		EHIPLANE_19	Interface_19	PMA direct	PAM4low	2G-30G	Off	Off
Channel_18			EHIPLANE_18	Interface_18	PMA direct	PAM4low	2G-30G		Off
Channel_17		EHIP_CORE_2	EHIPLANE_17	Interface_17	PMA direct	PAM4low	2G-30G		Off
Channel_16			EHIPLANE_16	Interface_16	PMA direct	PAM4low	2G-30G		Off
Channel_15	RSFEC_3		EHIPLANE_15	Interface_15	PMA direct	PAM4low	2G-30G	Off	Off
Channel_14			EHIPLANE_14	Interface_14	PMA direct	PAM4low	2G-30G		Off
Channel_13			EHIPLANE_13	Interface_13	PMA direct	PAM4low	2G-30G		Off
Channel_12			EHIPLANE_12	Interface_12	PMA direct	PAM4low	2G-30G		Off
Channel_11	RSFEC_2	EHIP_CORE_1	EHIPLANE_11	Interface_11	PMA direct	NRZ	1G-28.9G	Off	Off
Channel_10			EHIPLANE_10	Interface_10	PMA direct	NRZ	1G-28.9G		Off
Channel_9			EHIPLANE_9	Interface_9	PMA direct	NRZ	1G-28.9G		Off
Channel_8			EHIPLANE_8	Interface_8	PMA direct	NRZ	1G-28.9G		Off
Channel_7	RSFEC_1		EHIPLANE_7	Interface_7	PMA direct	NRZ	1G-28.9G	Off	Off
Channel_6			EHIPLANE_6	Interface_6	PMA direct	NRZ	1G-28.9G		Off
Channel_5		EHIP_CORE_0	EHIPLANE_5	Interface_5	PMA direct	NRZ	1G-28.9G		Off
Channel_4			EHIPLANE_4	Interface_4	PMA direct	NRZ	1G-28.9G		Off
Channel_3	RSFEC_0		EHIPLANE_3	Interface_3	PMA direct	NRZ	1G-28.9G	Off	Off
Channel_2			EHIPLANE_2	Interface_2	PMA direct	NRZ	1G-28.9G		Off
Channel_1			EHIPLANE_1	Interface_1	PMA direct	NRZ	1G-28.9G		Off
Channel_0			EHIPLANE_0	Interface_0	PMA direct	NRZ	1G-28.9G		Off

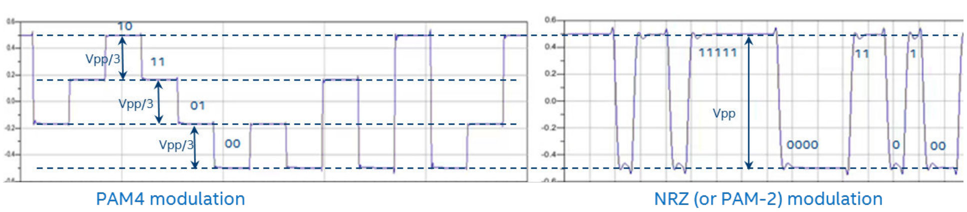
2.2. Intel Stratix 10 E-Tile Signaling - PAM4 vs. NRZ (PAM2)

The Intel Stratix 10 E-Tile enables both PAM4 and NRZ signaling.

PAM4 signaling uses four distinct voltage levels to encode two bits of data in every symbol, thereby doubling the bandwidth of the link without increasing the fundamental frequency.

The following figure shows illustrations of PAM4 signaling and NRZ signaling.

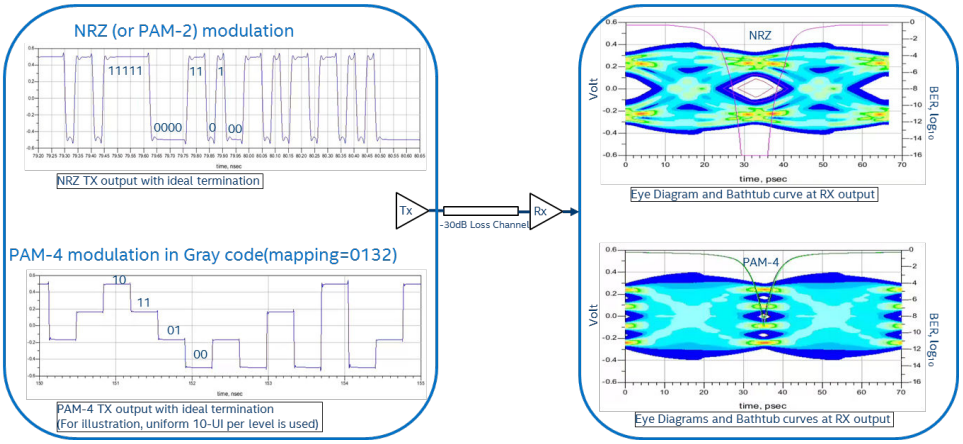
Figure 3. PAM4 vs NRZ Signaling



In PAM4 mode, the noise margin is reduced compared to NRZ mode since in PAM4, the amplitude between adjacent signal levels is only one-third that of NRZ. This intrinsic loss compared to NRZ reduces the noise margin by approximately -9.5 dB. Therefore, noise margin is a critical consideration for the design of high-speed links using PAM4 signaling.

The following figure shows signal modulation examples in an Intel Stratix 10 E-Tile channel design for both NRZ and PAM4 signaling modes.

Figure 4. Intel Stratix 10 E-Tile NRZ and PAM4 Modulation Examples

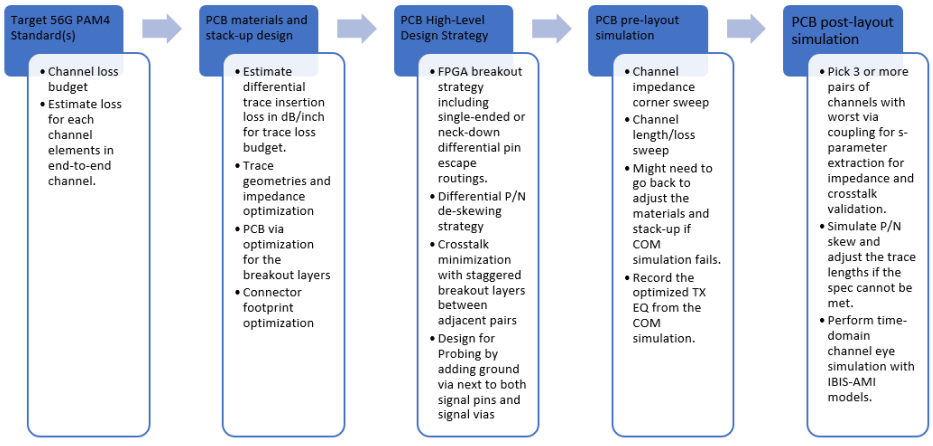


Due to the reduced noise margin in PAM4, the peak-to-peak eye opening is smaller than that in NRZ mode.

2.3. PCB Design Flow

The following figure shows the Signal Integrity work flow in a platform design. Some adjustments may be necessary if PCB simulations fail or do not reach the desired targets.

Figure 5. Signal Integrity Work Flow in Platform Design



2.3.1. Design Target at 56 Gbps PAM4 Standard

Understanding the PAM4 standards is the key in the PAM4 PCB design flow. You must evaluate your channel loss budgets by using a loss estimate for each channel element in an end-to-end channel.

Below are the recommended channel losses for different standards:

50/56G PAM4 - Refer to each standard for the loss requirement:

- IEEE802.3bs
- IEEE802.3cd
- OIF CEI-56G-VSR
- OIF CEI-56G-MR
- OIF CEI-56G-LR

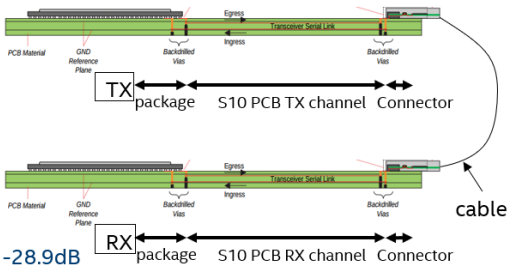
25/28G NRZ - Refer to each standard for the loss requirement:

- IEEE802.3bj
- IEEE802.3by
- OIF CEI-28G-VSR
- OIF CEI-28G-MR
- OIF CEI-28G-LR

The following figure shows the channel insertion loss (IL) budget calculation for an end-to-end (TP0 to TP5) 200GBASE-CR4 channel, with the IL estimate at the Nyquist frequency for each channel element provided. Intel recommends that you estimate the minimum and maximum insertion loss allocations for each element of the channel (transmitter to receiver) carefully to meet the link standard (e.g. IEEE802.3cd).

Figure 6. Example of an end-to-end 200GBASE-CR4 Channel Loss Estimation

- Nyquist frequency 13.28GHz
- IL_{Max}(TX S10 TX Pin PCB Via)= -1dB
- IL_{Max}(TX PCB Trace)= -6dB
- IL_{Max}(TX Connector+footprint)= -1.45dB
- IL_{Max}(Cable only) = -12dB
- IL_{Max}(RX Connector+footprint) = -1.45dB
- IL_{Max}(RX PCB Trace) = -6dB
- IL_{Max}(RX S10 RX Pin PCB Via) = -1dB
- Total IL_{Max} = Sum of each element loss = -28.9dB



The boundaries of each element (i.e. connectors and cables) in the above example must be carefully defined.

2.3.2. PCB Materials and Stackup Design

The proper selection of PCB materials and stackup is an essential key in the design flow. There are four key PCB channel design parameters/elements for E-Tile:

- Insertion Loss (IL)
  - The higher the channel loss, the more difficult it is for devices to send high-speed data over the channel reliably.
  - Different standards have different recommended channel losses.
- Return Loss (RL)
  - Return Loss (RL) measures how much energy a given channel reflects back. A channel with a high impedance discontinuity will have a bad RL performance (i.e. it will reflect back a lot of energy).
- Far-End and Near-End Crosstalk (FEXT and NEXT)
  - Crosstalk can be considered a form of noise from neighboring channels. It reduces the noise margin.
- Mode Conversion (MC)
  - Mode conversion can reduce the common noise cancellation. Common mode noise can leak into the differential mode and reduce the noise margin.

2.3.2.1. Insertion Loss

You must estimate the differential trace insertion loss in dB/inch for the trace loss budget based on the selected PCB materials and stackup. To optimize the PCB trace impedance and stackup, you must follow the key notes below:

If thin dielectric layers with high dielectric constant (Dk) cannot be avoided, lowering the trace impedance will avoid narrow trace widths, leading to:

- Better impedance control
- Better loss performance

Avoid tightly coupled differential traces for a given routing density. Doing this will:

- Reduce the trace impedance fluctuation when having deskew trombone.
- Achieve larger trace widths for a given impedance target.

Implementing the key notes above will improve the trace geometry and impedance optimization in your PCB design.

2.3.2.2. Return Loss

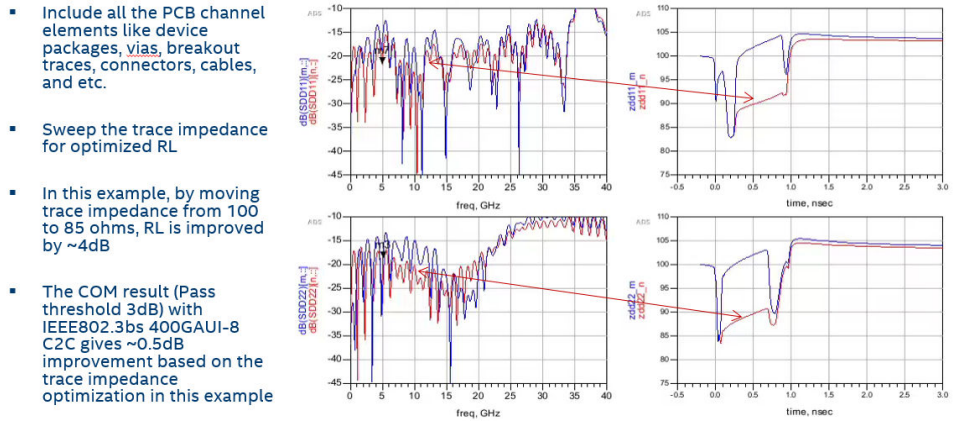
You must optimize the PCB trace impedance to achieve a better return loss or less signal reflection. Factors that determine the PCB impedance Z0 value for a better RL performance are:

- Elements in the end-to-end channels:
  - Device packages
  - PCB vias
  - Connectors
  - Cables
  - DC block caps (if they exist)
- PCB stackup and the dielectric and copper materials

Picking the PCB impedance Z0 that gives the minimum impedance fluctuation (discontinuity) with all other elements of the channel is the key for transferring the signal from one end of the channel to the other while minimizing the signal reflection.

The following figure shows an example of PCB trace impedance optimization. From the blue to red performance curves (insertion loss, return loss and time domain reflectometry (TDR) at both ends), it appears that a reduction in the impedance fluctuation eventually leads to a return loss improvement.

Figure 7. Example of PCB Trace Impedance Optimization



2.3.2.3. Package Loss and Crosstalk

The package loss for the Intel Stratix 10 E-Tile is summarized below for designers' end-to-end channel loss estimation/evaluation:

- Impedance specification: 90 ohm +/- 10%
- Maximum differential insertion loss: -3 dB (Tx or Rx) at the Nyquist frequency
- Differential return loss: better than -15 dB up to the Nyquist frequency
- Crosstalk (up to the Nyquist frequency)
  - NEXT < -60 dB
  - FEXT < -50 dB

2.3.2.4. PCB Via Design

PCB via structures are usually capacitive (fringe coupling from via pads/drill to surrounding reference planes). PCB vias also have via stubs (after back/top drilling to the through-hole vias), which can lower the via impedance even further.

Tuning the via anti-pad size to bring the via impedance to the required impedance tolerance range is essential in via optimization.

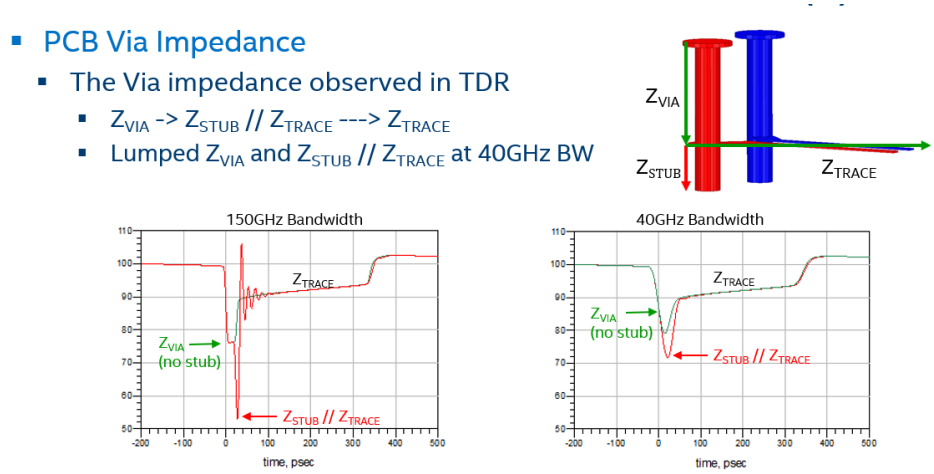
However, sometimes there are limitations to increasing the anti-pad size. Due to the ground reference needed for breakout traces, a small anti-pad can make the via impedance go very low.

Here are the techniques that you can take advantage of to control/optimize the PCB via impedance:

- A smaller PCB via anti-pad size results in a lower impedance.
- A longer PCB via stub also results in a lower impedance.
- Smaller PCB via drill sizes result in a higher impedance.
- Smaller PCB via top, bottom, and functional pads result in a higher impedance.
- Thin dielectric layers, i.e. denser planes, result in a lower impedance.
- A higher dielectric constant (Dk) results in a lower impedance.

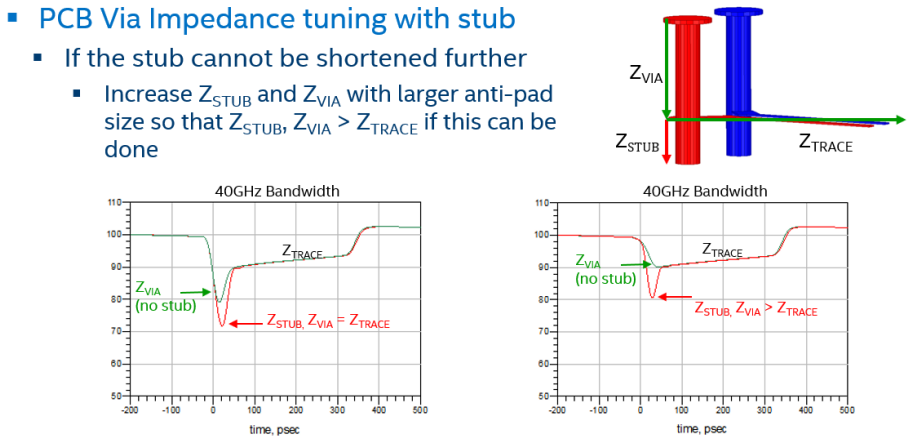
The figure below shows the impedance of PCB vias as measured by TDR. The higher the TDR bandwidth, the more details of the impedance change will be observed. The TDR plot in this figure is from the top via pad to the inner layer trace. The via stub has capacitive characteristics and it reduces the path impedance.

Figure 8. PCB Via Impedance Observation by TDR



The following figure shows the techniques used for PCB via impedance optimization/ tuning. Top/back drilling is essential in high speed data links. However, it may not be possible to shorten the via stub further due to fabrication house limitations. Therefore, achieving a larger anti-pad area would help tune the via impedance to reach a trace impedance with less reflection.

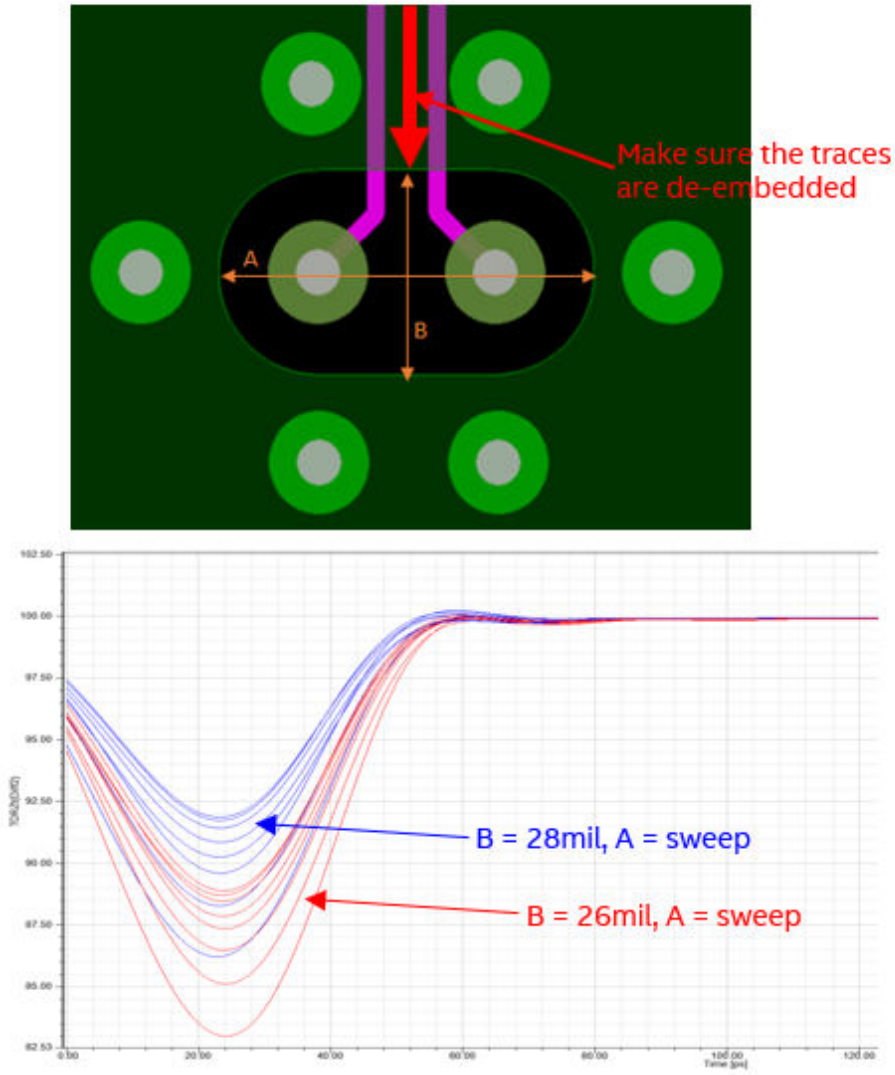
Figure 9. PCB Via Impedance Tuning with Stub



To further tune the PCB via impedance, you must follow the recommendations below:

- Use the smallest via drill/pad allowed in manufacturing to reduce the capacitive coupling that dominates the via impedance discontinuity. Reduce the anti-pad size for better breakout trace ground reference.
- Sweep the dimensions A and B (refer to the following figure) for the via impedance using any proven commercial 3D E/M tool that works for you.
- The B dimension can impact the breakout trace ground reference, so you should tune A first until you reach the maximum allowable A, then tune B.

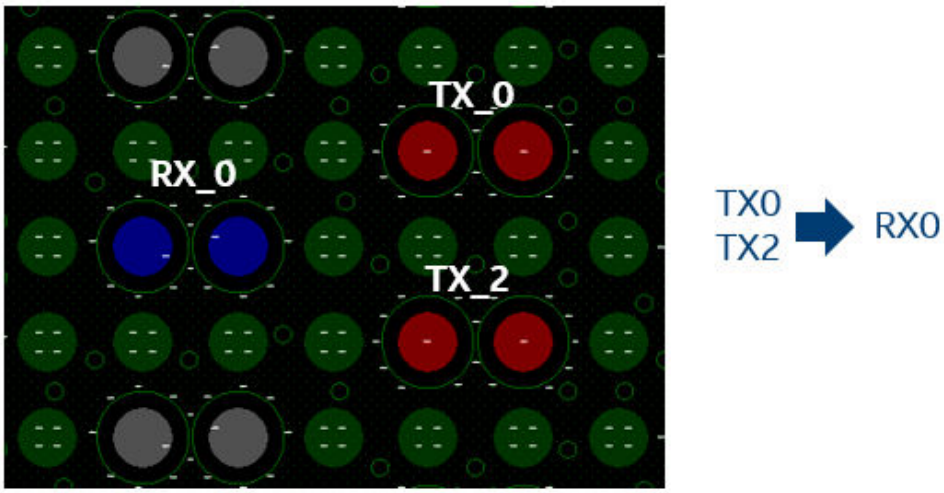
Figure 10. PCB Differential Via and TDR Performance with Respect to Various Sweeping Parameters in Via Impedance Control



PCB Via Crosstalk

The PCB via pattern follows the package BGA pattern. The via pattern and coupling length directly impact the PCB via coupling . Therefore, it is important to control the via coupling length for different via patterns in order to meet the crosstalk requirements. The 56G PAM4 mode puts a very strict crosstalk limitation (60 dB) on the TX/RX. Referring to the PAM4 usage mode, when channels 2n (n=0, 1, .. 11) run 56G, all other channels are quiet. Therefore, the same channel's TX-to-RX crosstalk, and the next second channel's TX-to-RX crosstalk are among the worst-case crosstalk scenarios in the PCB design. See below worst-case via pattern for TX/RX. For these via transitions, Intel recommends that you control the via coupling length to be smaller than 40 mil.

Figure 11. Worst-Case Via Pattern, 2-TX to 1-RX Crosstalk



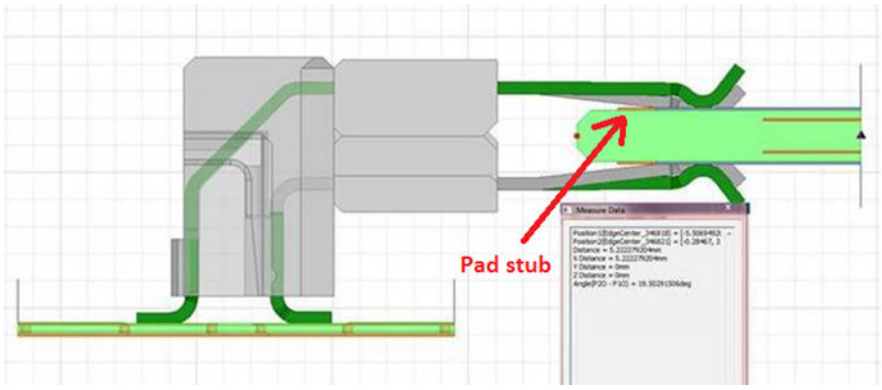
2.3.2.5. PCB Connector

Connectors are unavoidable in PCB board design. Hence, the PCB connector footprint must be optimized and tuned to reach the trace target impedance and have less discontinuity or reflection. Here are some tips that you can follow to optimize the PCB connector footprint:

- Optimize the PCB connector footprint while following the connector vendor's guideline.
- Provide the PCB stackup and material information for the connector vendor to optimize the PCB footprint based on the channel impedance requirement.
- Make sure the connector model boundary is defined clearly.
- The connector model from the vendor usually includes the vendor's reference PCB footprint.
- Check if the connector model from the vendor includes the worst-case geometry, i.e. the pad stub of the mated edge card.

The following figure shows a QSFP connector as an example in the PCB connector footprint optimization.

Figure 12. QSFP Connector and PCB Footprint Optimization



Co-simulation must be done with the connector in an E/M tool solver. In the pre-layout phase, provide the PCB stackup and materials to the connector vendor for preliminary footprint optimization. In the post-layout phase, provide the routed PCB footprint to the connector vendor along with the final co-simulation with connector. Make sure to define a clear boundary for the final post-layout model for the end-to-end channel simulation.

2.3.2.6. Cable Usage in PCB Design

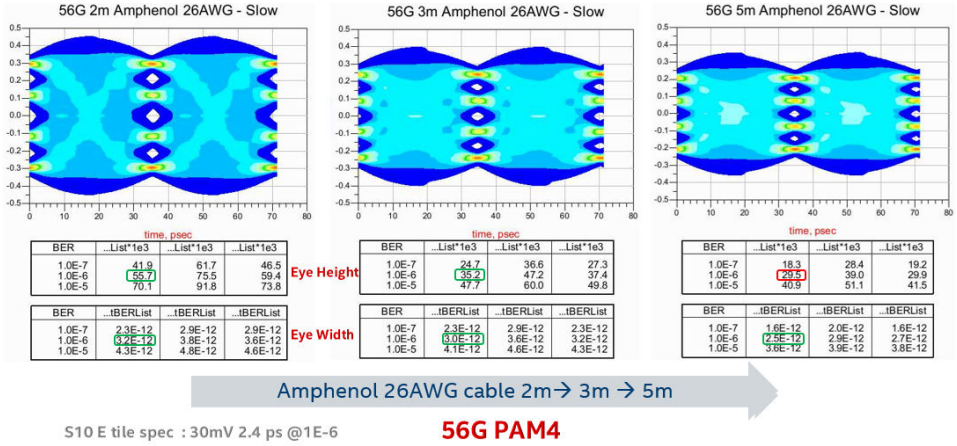
The direct attached copper cable (DAC) is the most common cable usage in high-speed PCB link design. DAC is available in various cable lengths/sizes for different applications.

You must make sure the cable model boundary is clearly defined at both ends. In addition, you should check with the cable vendor if the cable model includes the cable wire termination and edge card (elements to consider in simulation).

A ~5 dB (at 14 GHz) host board, with most AWG-26 2 m, 3 m cables and 5 m cables and with careful transmit and receive equalization tuning, can support 56G PAM4. The E-tile PAM4 mode can support ~30 dB pad-to-pad loss in cable applications.

Figure 13. TX-RX Connection via Cable

Figure 14. Channel Eye Simulation of Different Cables (~5 dB RX and 5 dB TX PCB Trace Routing)



2.3.3. FPGA PCB Design

PCB design involves end-to-end high-speed paths design from the FPGA to the connectors/chips/other devices. It starts with the FPGA breakout region, and the design strategy should include single-ended or neck-down differential pin scape routings. PCB design also covers differential P/N de-skewing strategy, crosstalk minimization with staggered break-out layers between adjacent pairs as well as proper design for probing by adding ground vias next to signal pins for impedance control and via reference ground path.

2.3.3.1. FPGA PCB Breakout Design and Reference

This section focuses on the FPGA PCB breakout routing for high-density serial channel designs beyond 10 Gbps.

Refer to the AN-651-1.0 application note for preliminary breakout routing study.

Link to AN-651-1.0: PCB Breakout Routing for High-Density Serial Channel Designs Beyond 10 Gbps

The Intel Stratix 10 E-Tile differential RX/TX balls are completely shielded with ground balls, as compared to previous RX/TX balls being diagonally placed without ground ball shielding. The FPGA BGA/pin pitch is 1mm. There are some changes to breakout routing techniques in AN-651 as described below to better impedance matching.

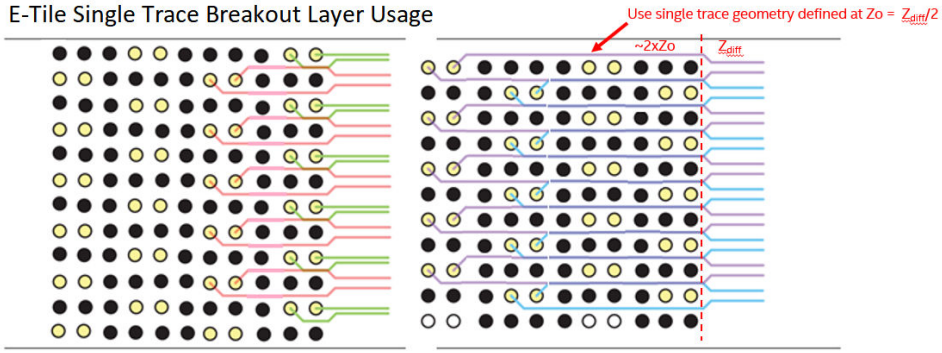
The single trace breakout study in AN-651 does not consider ~47 ohm Zo (but uses a 51.3 ohm Zo instead), so there is an impedance discontinuity at the boundary between the single trace breakout and the differential routing segments. With ~47-ohm for the single trace breakout, the differential impedance can be maintained at around ~94 ohm when crossing the boundary. The single trace breakout can still be an option with the differential impedance matching technique mentioned above when the ground reference coverage for differential breakout traces becomes an issue due to large optimized via anti-pads for a high-Dk and high-layer-count PCB.

Another benefit with the single trace breakout is that the breakout layer assignment is not constrained by the back-drill effectiveness mentioned in AN-651 due to adequate via-to-copper clearance for the back-drill.

Here are some tips to improve the single trace breakout example in AN-651 (shown in the following figure):

- Single trace Zo = 51.3 ohm, Zdiff = ~102.6 ohm with loosely coupled P/N traces.
- Use widened single trace with Zo = Zdiff / 2 to match the differential impedance.
- Via impedance also plays a major role in the loss performance in the study.

Figure 15. E-Tile Single Trace Breakout Layer Usage and Routing



2.3.3.2. P/N De-skew Strategy on Differential Pairs

High-speed data on differential links must be de-skewed to achieve the maximum eye opening and avoid mode conversion. There are various ways to de-skew a differential pair: in the via anti-pad area or in the trace.

There are some signal integrity issues with de-skewing in traces:

- Impedance fluctuation (discontinuity) issue: For tightly coupled differential traces, the de-skew trombone on one of the P/N legs creates loosely coupled sections that cause a high impedance unless the impedance of those sections is tuned in layout.
- Mode conversion issue: The de-skew trombone on one of the P/N legs may have less delay per unit length compared to the straight trace on the other leg. For more details, refer to http://www.sigcon.com/Pubs/edn/serpentine.htm

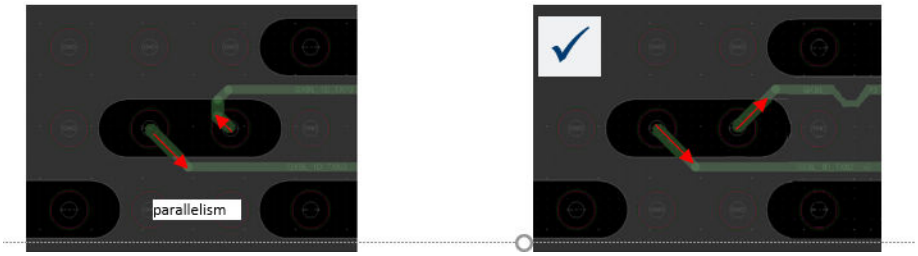
There are also some signal integrity issues with de-skewing inside the via anti-pad area:

- The trace delay is smaller in the via anti-pad area due to less coupling to the reference planes.
- The trace impedance discontinuity due to the length mismatch inside the via anti-pad can also cause signal integrity issues.

Figure 16. De-skew Inside/Outside the Via Anti-pad

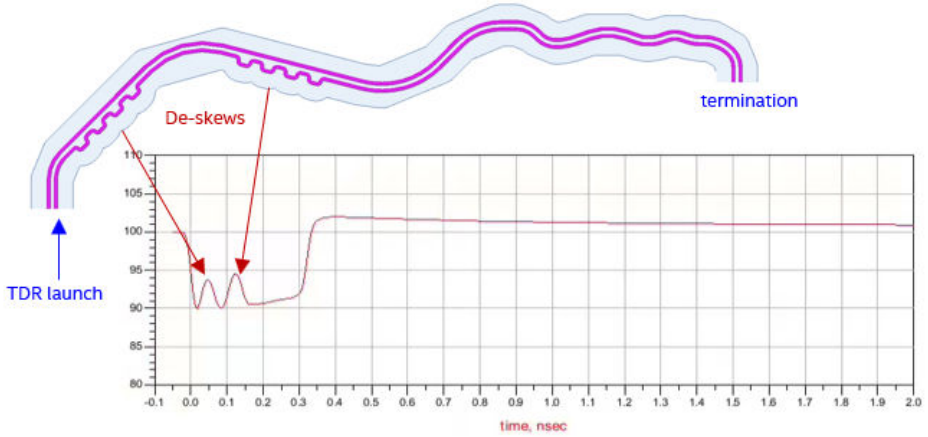
- For de-skewing with single-ended breakout routing, the trace parallelism inside the anti-pad with no ground reference causes NEXT effect (see the following figure). However, the NEXT effect is not significant with 1 mm pin-pitch vias and short coupled lengths as shown in the left image of the picture.

Figure 17. Parallelism, Crosstalk and De-skew in the Via Anti-pad Region



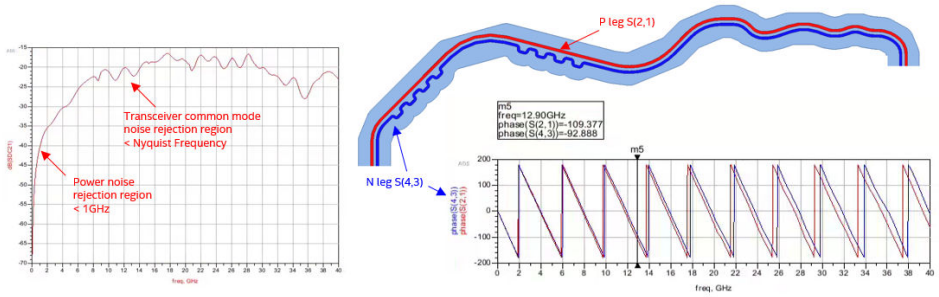
The figure below shows an impedance discontinuity example due to trace de-skew. The most common way to de-skew P/N lanes in a differential pair is to use the trace trombone configuration. As you can see in the TDR performance of the trace in the figure, the impedance of the differential pair fluctuates due to the discontinuity in that trombone region. In this example, the differential pair is routed on the top layer and has tight coupling between the P/N legs , i.e. Zodd << Zeven. It appears there are 4-ohm Zdiff bumps in the TDR performance curve that eventually cause a return loss penalty.

Figure 18. Impedance Discontinuity Example Due to Trace De-skew



The following figure also shows a mode conversion example due to trace de-skew. In this example, the delay difference between the P and N legs as well as the measured trace lengths end-to-end are the same in the layout tool. However, through simulation, the P leg delay is about 17 degrees or 3.5 ps longer than the N leg delay at the Nyquist frequency (12.9 GHz). The delay difference between the P and N legs increases at higher frequencies. The common mode to differential mode conversion is about -20 dB.

Figure 19. Mode Conversion Example Due to Trace De-skew

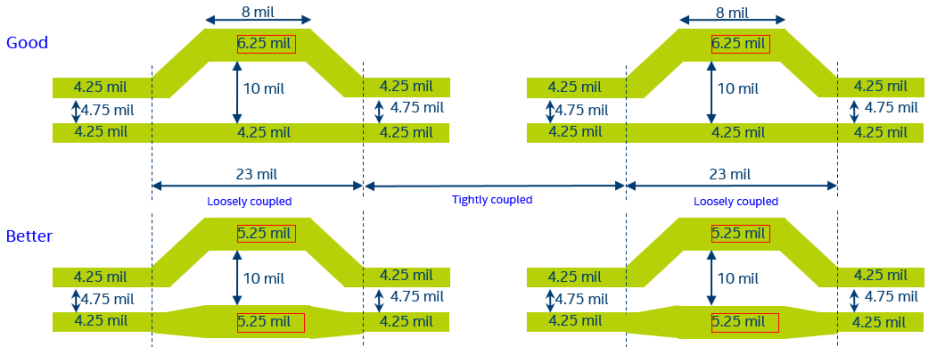


The figure below illustrates some routing recommendations for trace de-skew to avoid both an impedance mismatch and mode conversion.

Trace De-Skew Trombone Consideration for Tightly Coupled Differential Pairs

Widening the trace segments with loosely coupled P/N legs will help with impedance compensation and reduce the impedance in that region. The figure below illustrates good and better implementations of the trace de-skew trombone configuration.

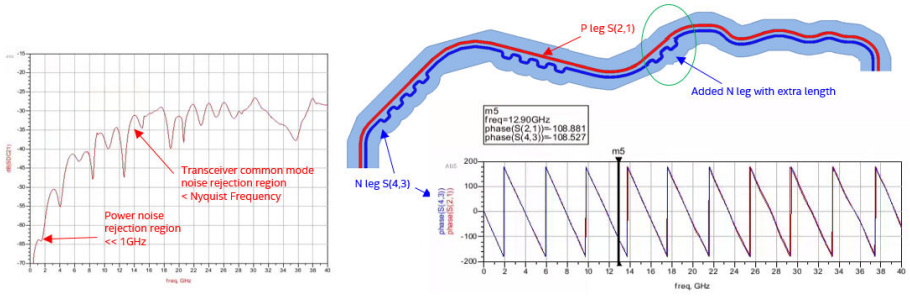
Figure 20. Improving Impedance Matching in Trace De-skew Trombone Configuration



Trace De-Skew Length Matching Consideration for Differential Pair

Adding extra length on the leg with more de-skew trombone will help compensate for the trace delay for better de-skewing. However, simulations or lab measurements are required to determine the extra lengths needed in layout. The following figure shows the N leg with added length. The common mode to differential mode conversion improves by an extra 19 dB at 12.9 Ghz and by 25 dB at 1 GHz compared to the example shown in the figure *Mode Conversion Example Due to Trace De-skew* above.

Figure 21. Improving Mode Conversion in Trace De-skew Trombone Configuration



2.3.3.3. Crosstalk - NEXT and FEXT in Differential Pairs

In PCB layout, the typical crosstalk sources are:

- PCB BGA via
  - Distance between vias, nearby ground vias, and via barrel length parallelism
- PCB via for layer transition and DC blocking capacitors
  - Distance between vias, nearby ground vias, and via barrel length parallelism
- PCB traces
  - Edge coupled micro-strip lines
    - Pair-to-pair airgap, trace to reference plane distance, and trace coupling length, based on simulation, all combine to obtain FEXT < -50 dB, NEXT < -60 dB
  - Edge coupled strip lines
    - Pair-to-pair airgap, trace to reference plane distance, and trace coupling length, based on simulation, all combine to obtain FEXT < -50 dB, NEXT < -60 dB
- Connectors
  - Vendors, types, pin assignments, footprints, etc.

The other source of crosstalk is the package as discussed in the section titled *Package Loss*. The achieved package crosstalk for the Intel Stratix 10 E-Tile is less than -60 dB for NEXT and less than -50 dB for FEXT.

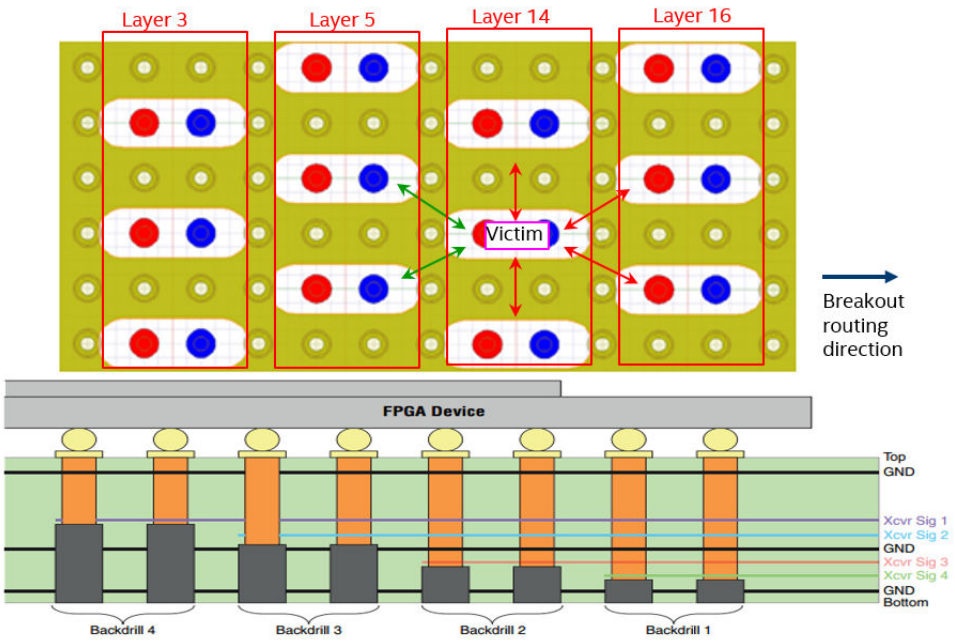
Crosstalk at BGA VIA

There are multiple factors affecting the crosstalk at a BGA via, including:

- Pin assignment
  - How close the signal pins are to one another
  - How far the signal pins are from reference (ground) pins
- Routing layer assignment
  - Using a routing layer closer to the BGA chip results in shorter via barrels and less coupling among the vertical signal vias.
- Via anti-pad size
  - Tuning the via anti-pad with larger sizes to mitigate the low via impedance issue can also increase the crosstalk due to less coupling to the reference. Include the crosstalk effect during the via impedance optimization as a design trade-off.
- PCB Stackup
  - More reference planes within the same stackup thickness (i.e. denser reference planes) provide a higher coupling to reference, resulting in less crosstalk.

The following figure shows an example of a routing layer assignment for less BGA via crosstalk. A typical breakout layer assignment for high-speed differential signals is illustrated. There are six adjacent signal via pairs acting as crosstalk sources in this example. The worst coupling pair depends on the number of grounds between the columns/rows (vertical ground vias). Coupling between breakout vias in the bottom layers gives significant crosstalk due to long via barrel parallelism. The crosstalk due to this parallelism from the six neighbors has also been illustrated in the figure.

Figure 22. BGA Via Barrel Parallelism and Crosstalk in Routing Layers Assignment

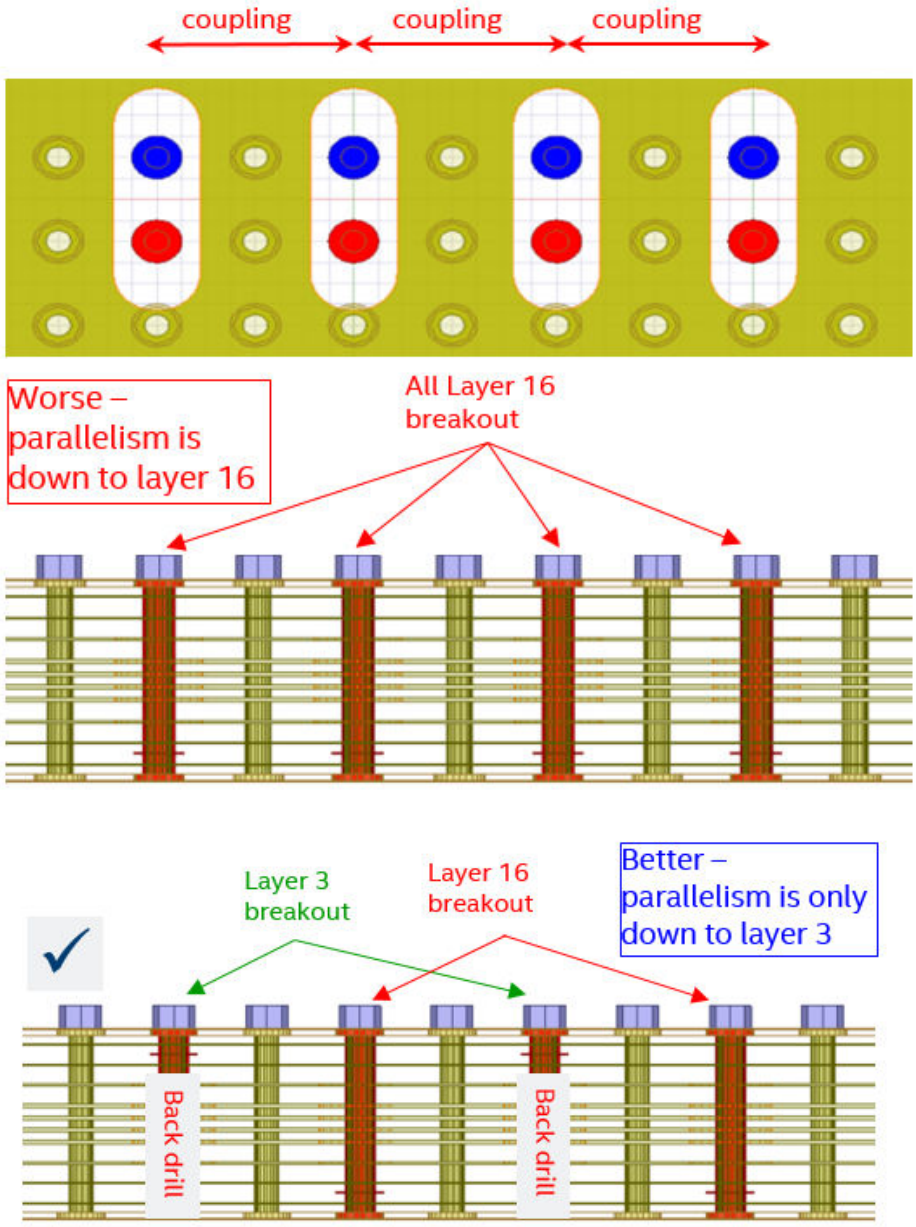


Strategy to Reduce Crosstalk among BGA Vias

Here are some tips to reduce the crosstalk among BGA vias (illustrated in the figure below):

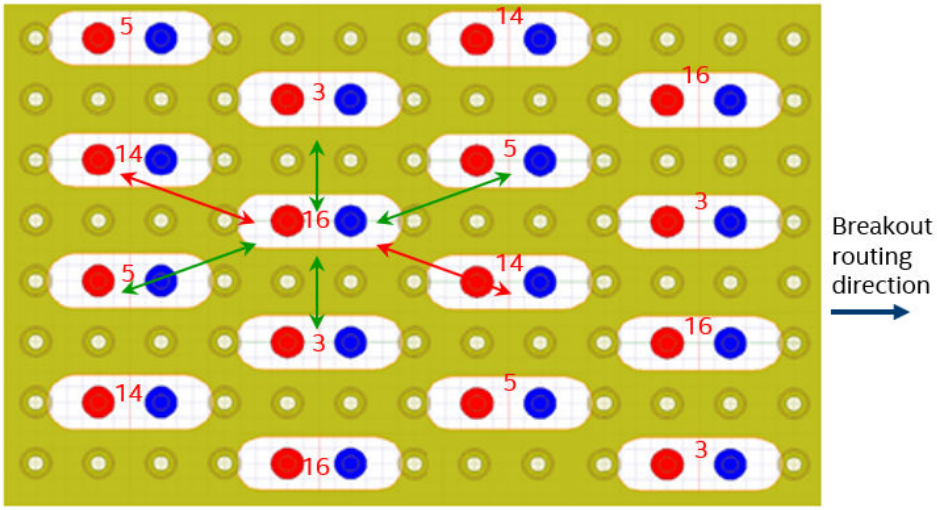
- Stagger breakout layers for adjacent signals and reduce the via parallelism.
- For an n-layer board:
  - Use adjacent signal vias with breakout on layers i and j where i+j <= n+1.
  - Single trace breakout may be needed for drill to trace tolerance/margin.

Figure 23. Strategy to Reduce BGA Vias Crosstalk in Routing Layer Assignment



The figure below shows the final breakout layer assignment for the example shown in the figure titled *BGA Via Barrel Parallelism and Crosstalk in Routing Layers Assignment* above. In this assignment, the crosstalk to the six adjacent high-speed differential signal via pairs has been improved. In the example, an 18-layer board has been used and via barrel parallelism from the neighbors has been reduced. Single-ended trace breakout may be needed for drill-to-trace tolerance and also back-drill-to-trace tolerance.

Figure 24. Final Breakout Layer Assignment for BGA Via Crosstalk Reduction



2.3.4. PCB Pre-Layout Simulation Phase

Pre-layout simulation is the preliminary phase of the PCB design. This link simulation models the channel on the PCB, and it must cover the items below:

- Channel impedance corner sweep
- Channel length/loss sweep
- You may need to adjust the materials and stackup if the Channel Operating Margin (COM) simulation fails.
- Record the optimized TX EQ from the COM simulation.

COM (Channel Operating Margin - IEEE802.3cd/bs)

COM is initially published in IEEE802.3cd.

- Normative channel compliance is through COM computation with specified margin.
- IEEE802.3cd/bs spec and COM are not fully finalized yet as of this document's publish date.
- IEEE802.3cd/bs compliance check for the channels is mandatory. It is a fast way to check the compliance of the channels with scattering parameters or S-parameters in touchstone format.
- The optimized TX FFE c(-2), c(-1), and c(1) may be used to assist in the IBIS-AMI simulation as a "starting point" for TX EQ settings based on the conversion table to be made available in the E-Tile IBIS-AMI model user guide (if the E-tile TX FIR starting point table or RX equalization alone cannot achieve the desired BER target).
- COM tool is available in the Intel Advanced Link Analyzer (formerly JNEye) for you to test your channels.

2.3.5. PCB Post-Layout Simulation Phase

Post-layout simulation is a mandatory design phase for the Intel Stratix 10 E-Tile high-speed data links. Follow the steps below in your post-layout simulation:

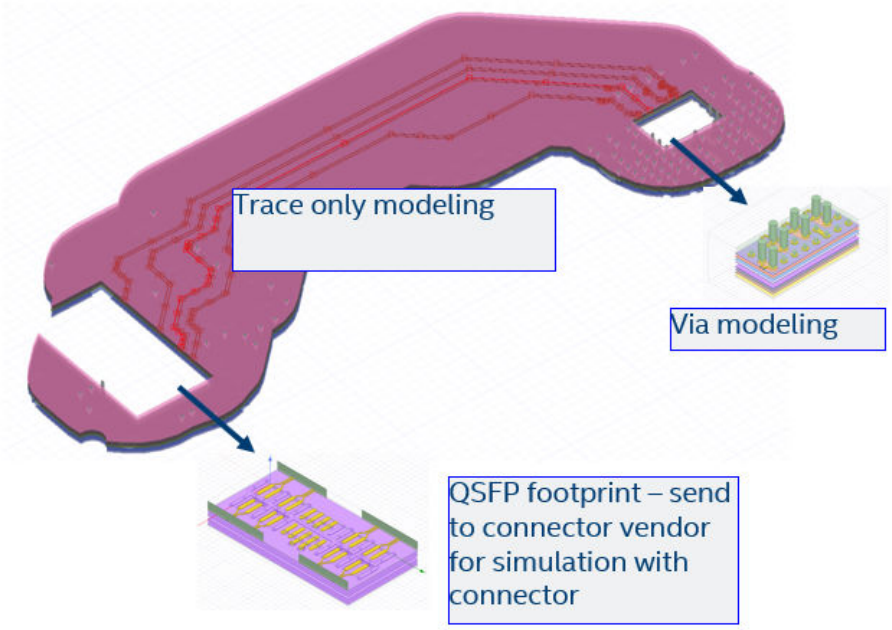
- Pick three or more pairs of channels with the worst via coupling for s-parameter extraction for the impedance and crosstalk validation.
- Perform time-domain channel eye simulation with the IBIS-AMI models while the actual channel model is being extracted.

Strategy for Post-Layout PCB Channel Modeling

- Extract the entire PCB channel in the E/M solver (not recommended)
  - The extraction takes a long time to finish and is not even possible for many complicated cases.
  - Connector pads do not have proper coupling to the connector, and may be double-counted when cascading with the connector model.
- Use the divide-and-conquer method (recommended)
  - Cut the channel at the trace near the FPGA/connector pad/via boundary.
  - Solve the trace-only portion.
  - Solve the FPGA via with the package ball and ground reference.
  - Solve the connector pad/via with the connector together. This step may require SI support from the connector vendor.
  - Cascade all pieces solved individually to build the whole channel eye simulation with the IBIS-AMI model.

The following figure shows a channel model extraction example using the recommended procedure, i.e. the divide-and-conquer methodology.

Figure 25. Divide and Conquer Methodology in Channel Model Extraction



This figure shows a group of four RX channels selected from the actual layout of a PCB. The benefits of the divide-and-conquer methodology to this example are:

- No double counting of the QSFP pin pads when combining with the QSFP connector model.
- The different portions of the channel can be simulated faster individually, and these simulations can be run in parallel.
- A 2.5D E/M solver may be good enough for trace-only geometries.
- Trace setup is easier and includes the etching effect.

The only disadvantage of the divide-and-conquer method is that it takes a longer time to prepare the cutouts and settings. However, the time cost can be improved with clearly specified steps.

3. Document Revision History for AN 875: Intel Stratix 10 E-Tile PCB Design Guidelines

Document Version	Changes
2019.03.12	Updated maximum transceiver data rates. NRZ was 30 Gbps, is 28.9 Gbps, PAM4 was 56 Gbps, is 57.8 Gbps.
2018.09.21	Initial release.