Application note

PCB layout tips to maximize ESD protection efficiency

Introduction

Electronic equipment's are smarter and more complex, embedding fragile and susceptible IC’s.

Environment is often harsh for these devices, generating high level electrostatic charges and fast transient surges. These ESD events may disturb equipment, from malfunction up to destruction of IC.

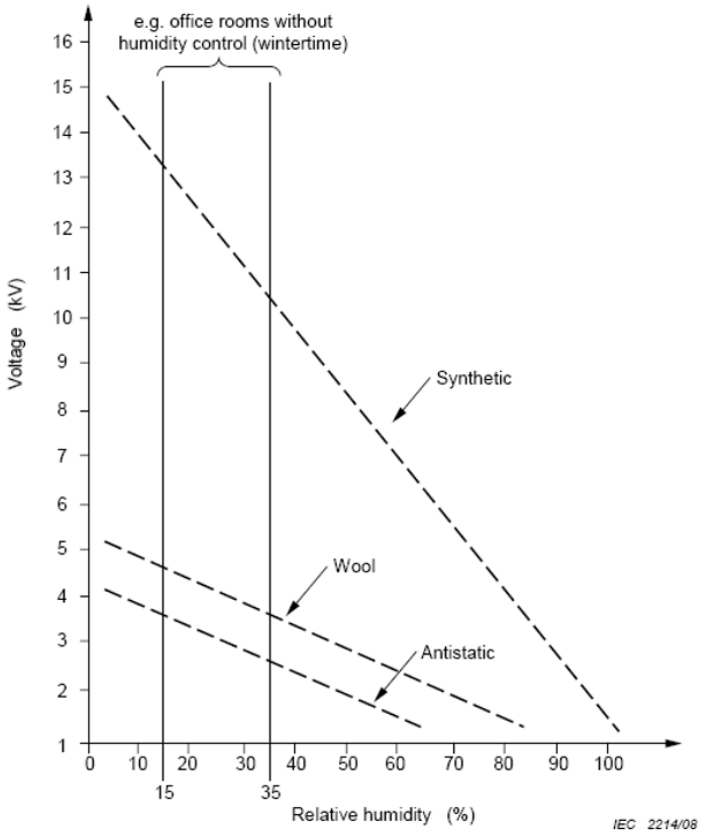
The best way to minimize these issues is to place transient voltage suppressors (TVS) from ST, where the surges can appear; but some care must be taken for routing these components to ensure the best possible protection.

This note gives some tips to achieve this result.

1 Electrostatic discharge

Electrostatic charges are mainly generated by our body in contact with various insulating materials. The amount of charges depends on the materials themselves and on the ambient relative humidity around. The discharge waveform is linked to the resistive way used by the charges to return to the earth. The IEC61000-4-2 standard models these kinds of discharge. The Figure 1 extracted from this standard shows the voltage levels reached versus different materials and relative humidity.

Figure 1. Maximum values of electrostatic voltages to which operators may be charged while in contact with three kinds of material



It is clear that dangerous level can occur for sensitive components. The standard defines four severity classes, corresponding to four voltage levels, with two types of discharge, contact and air. The Table 1. Classes versus voltage levels and current waveform definition for contact discharge shows the definition of these classes for a contact discharge and the definition of the waveform versus the different voltage levels.

Table 1. Classes versus voltage levels and current waveform definition for contact discharge

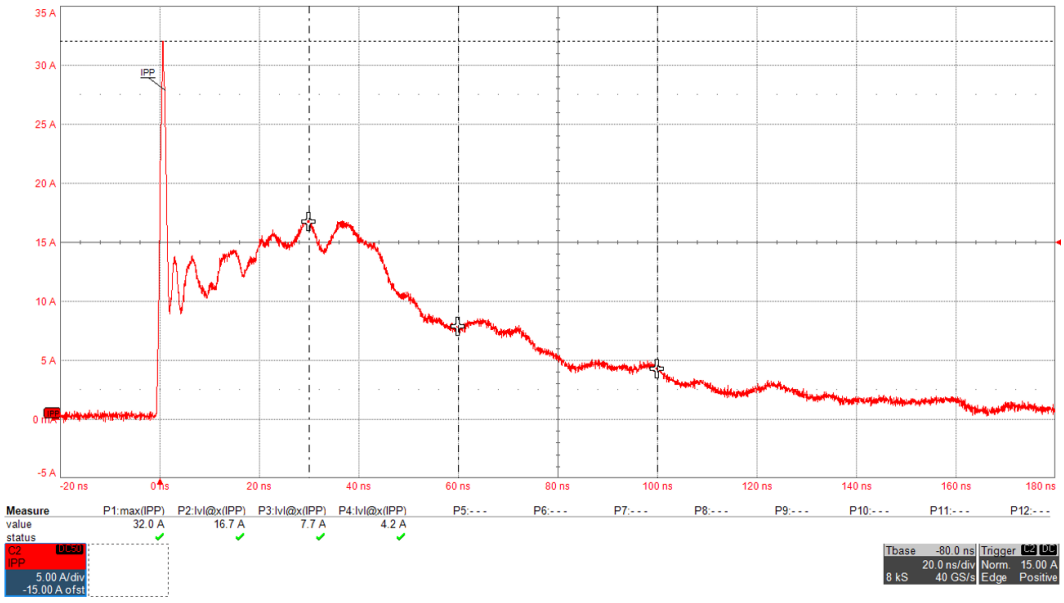
Level	Indicated voltage	First peak current of discharge ±15%	Rise time t_r (±25%)	Current (±30%) at 30 ns	Current (±30%) at 60 ns
	kV	A	ns	A	A
1	2	7.5	0.8	4	2
2	4	15	0.8	8	4
3	6	22.5	0.8	12	6
4	8	30	0.8	16	8

Note: The reference point for measuring the time for the current at 30 ns and 60 ns is the instant when the current first reaches 10% of the first peak of the discharge current.

The rise time, t_r, is the time interval between 10% and 90% value of the first peak current.

We can see that the waveform is composed by a first peak current with a very fast rise time, typically 0.8 ns, followed by a current starting from half the peak and decreasing to zero during around 200ns. The Figure 2 shows this waveform measured through a shunt resistor.

Figure 2. Typical current waveform for an 8kV contact discharge IEC61000-4-2 level 4



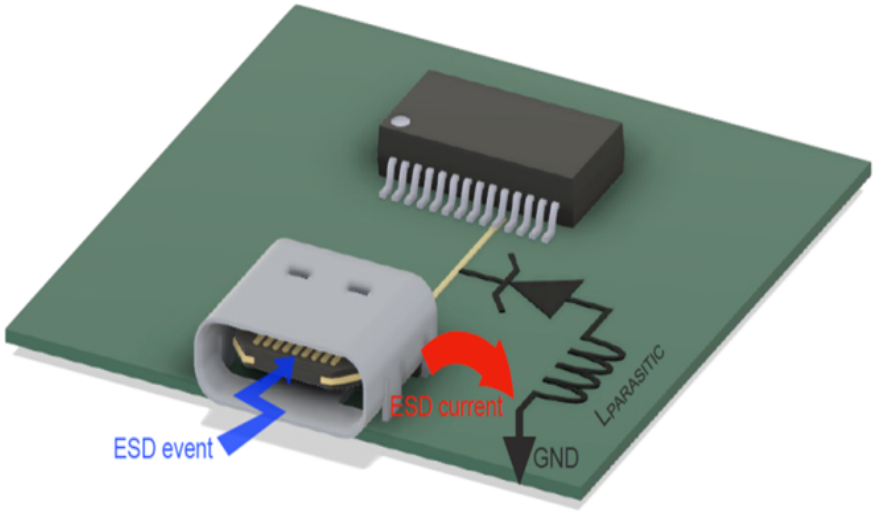
If we choose the example of the most severe level (level 4), the fast rise time of this waveform will induce a theoretically $\frac{dI}{dt}$ from 24 A/ns up to 40 A/ns and typically 30 A/ns.

This high $\frac{dI}{dt}$ of ESD current flowing from the ESD protection to the ground will induce on parasitic series inductance a proportional overvoltage $V_{PARASISTIC}$ equal to:

$$V_{PARASITIC} = L_{PARASITIC}\frac{dI}{dt} \quad (1)$$

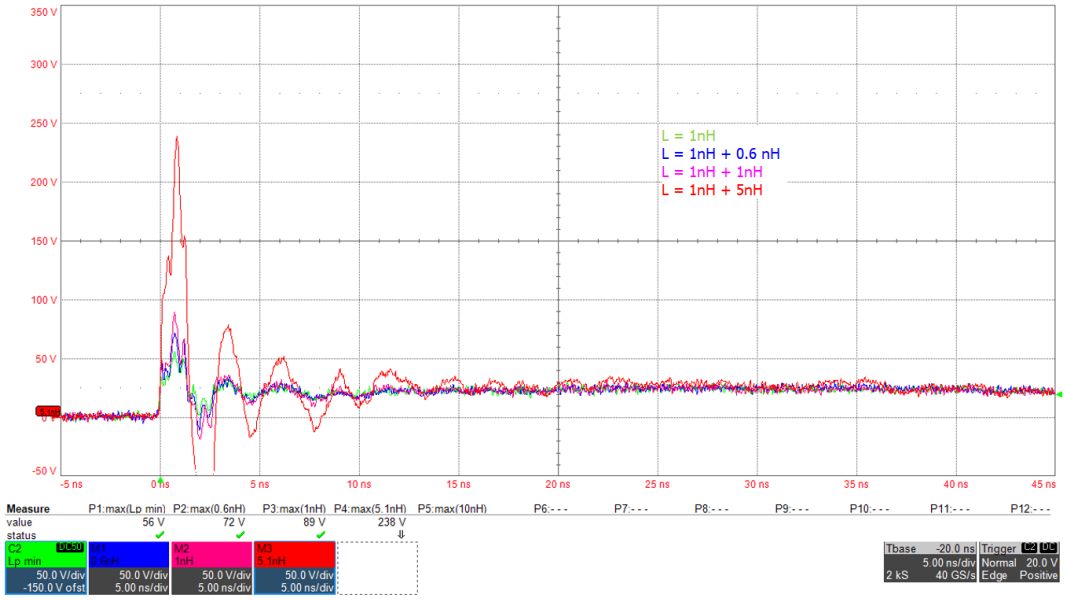
The picture on Figure 3 shows a typical configuration of a TVS placed just after a connector in order to protect the ASIC just behind. The parasitic inductance $L_{PARASITIC}$ due to the layout is always present between the protection diode and the ground.

Figure 3. **TVS and parasitic inductance**



To show the influence of this parasitic impedance in the protection circuit, we can insert a known inductance to evaluate the result on the protection response. In Figure 4, we can see the behavior of the clamping characteristic just after the protection when three inductances are added: 600 pH, 1 nH and 5 nH.

Figure 4. **Clamping voltage V_{CL} versus ground parasitic inductance**



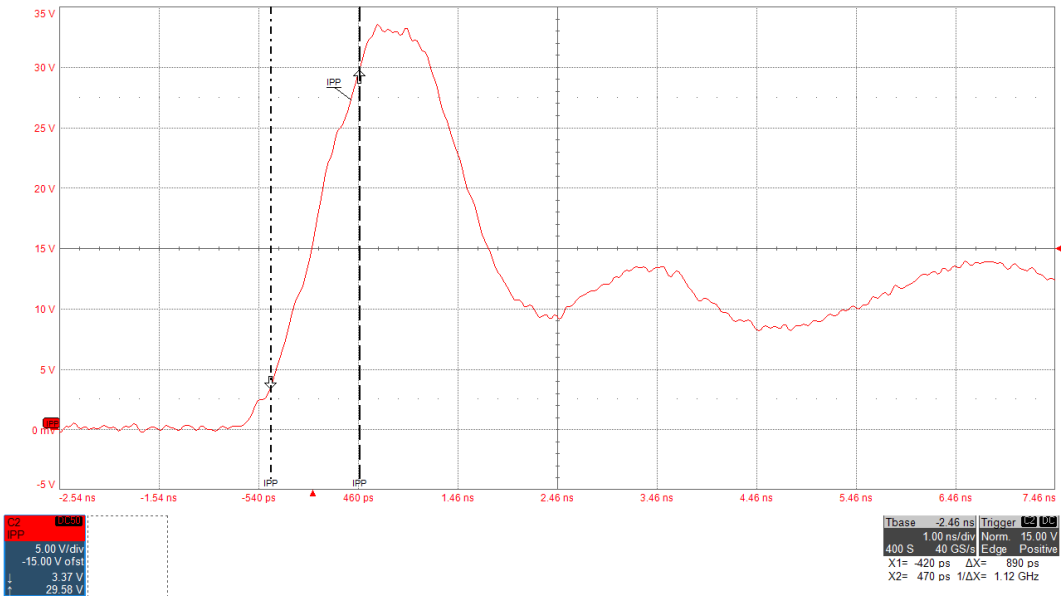
The green curve is the clamping voltage measured with the “best in class” parasitic inductance of the PCB evaluated at 1nH.

The peak clamping voltage is then equal to 56 V.

The blue, orange and red curves represent the clamping voltage with parasitic inductances added of 0.6 nH, 1 nH and 5 nH.

We can see than the peak voltage is then equal to 72 V, 89 V and 238 V. This increase is due to the $\frac{dI}{dt}$ during the surge (see Figure 5).

Figure 5. $\frac{dI}{dt}$ during ESD, here equal to 30 A/ns for 8 kV contact discharge



Note: The clamping voltage after the peak, at 30 ns for example which is generally the reference, is not affected by the ground inductance.

Moreover, transient magnetic field is generated during this ESD event and may induced voltage ringing by coupling in any loops of PCB tracks or wires, causing ground bounce and risk of loss of function of the equipment due to latch-up of IC's structures or reset.

The next figures extracted from IEC61000-4-2 standard illustrate these phenomena. Figure 6 gives an order of the magnetic field generated by a 5 kV ESD event and Figure 7 an order of the voltage that can be generated in a semi loop.

Figure 6. Magnetic field of a real human holding metal charged at 5 kV and measured at 10 cm

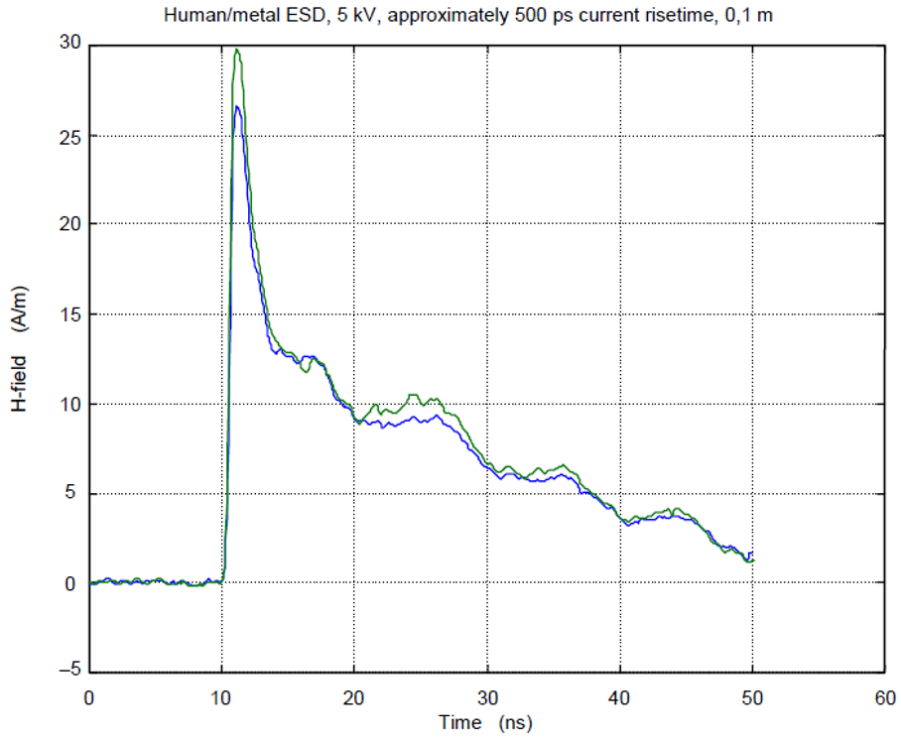
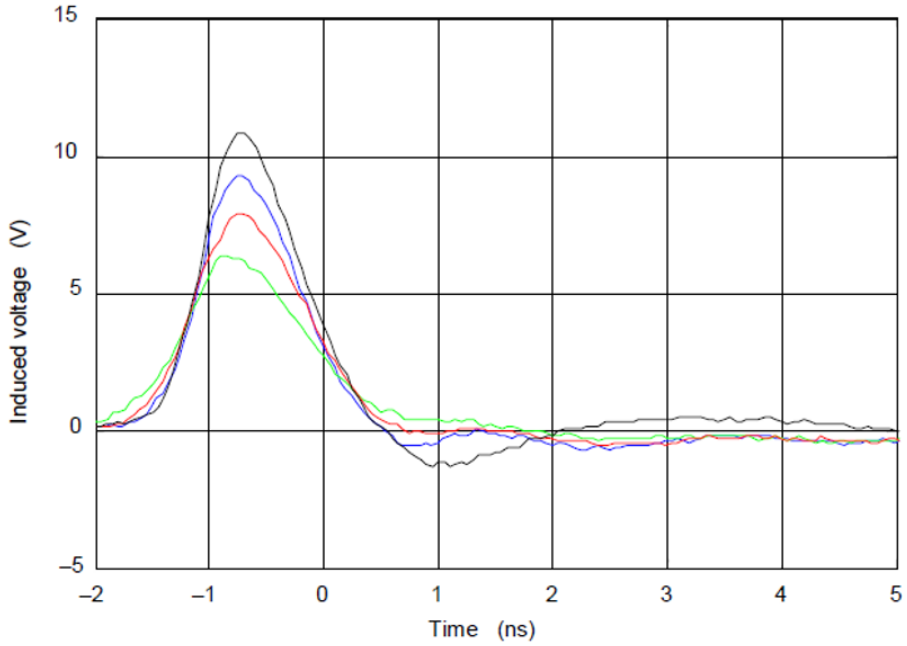


Figure 7. **Voltage induced in a semi-loop by a 5 kV ESD discharge**



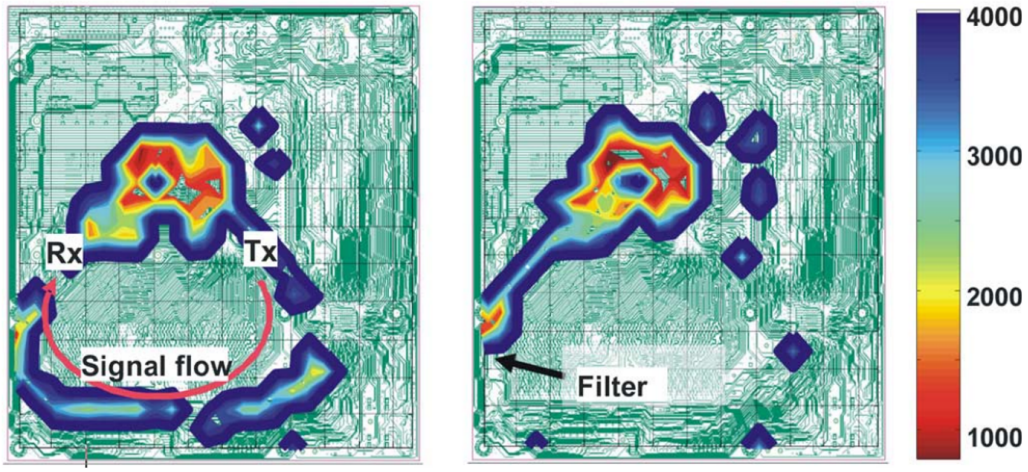
A way to reduce coupling is to use straight paths, as short as possible and also to avoid 90 ° trace angles when change of direction is necessary; 45 ° is preferred, the best way is round corner. Acute angle radiates more than an obtuse one.

Furthermore, the electric field generated can be coupled by capacitive effect, so it is better to route exposed and protected lines far from sensitive unprotected ones.

To illustrate these phenomena, Figure 8 shows a mother board PCB submitted to various levels of TLP (transmission line pulse, like ESD event) up to 4 kV and the corresponding H field levels, spreads on the board thru the tracks, far from the source.

On the right picture, a filter has been introduced at the surge source to suppress the unwanted noise. We can show that the noise generated disappeared.

Figure 8. **ESD susceptibility map (courtesy of amber precision Instruments)**



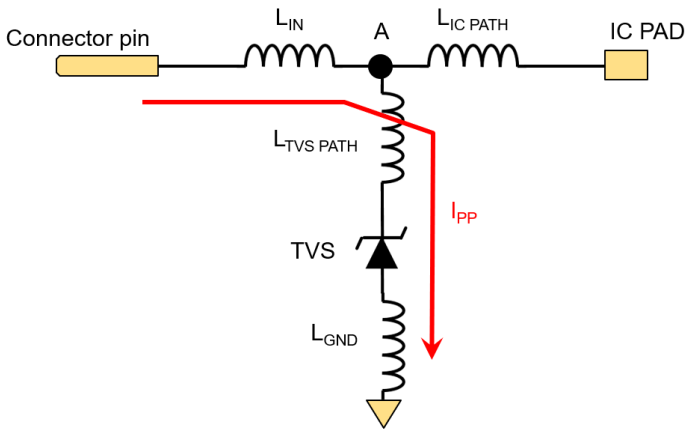
2 Layout rules of thumb

To summarize that we see above, the best way to provide an efficient ESD protection is to follow below rules:

- Minimizing the impedances around the TVS in order to control the ESD current paths
- Using vias to drain the current to the ground as close as possible from its input
- Designing a ground with a very low impedance to dissipate ESD energy
- Limiting the effects of EMI for the sensitive circuit

2.1 Minimizing the impedances

Figure 9. Inductances around protection device and IC



Most of the impedances between the surge source and the protected IC pin are made by the parasitic inductances shown in Figure 9.

L_{IN} and $L_{IC\ PATH}$ are often driven by the controlled impedance of the line (50 Ω or 100 Ω differential for example). To force the surge current to flow through the protection circuit, we must ensure L_{GND} and $L_{TVS\ PATH}$ as low as possible. Also, to minimize radiations on PCB, the best way is to place the protection circuit as closer as possible to the connector pin.

At A point, the peak overvoltage during the ESD surge current I_{PP} is equal to:

$$V_A = V_{CL} + \frac{dI_{PP}}{dt} \times (L_{TVS\ PATH} + L_{GND}) \quad (2)$$

Where V_{CL} is equal to:

$$V_{CL} = V_{BR} + R_D \times I_{PP} \quad (3)$$

V_{BR} is the breakdown voltage of TVS and R_D its dynamic resistance, measured in TLP test conditions in its clamping characteristic.

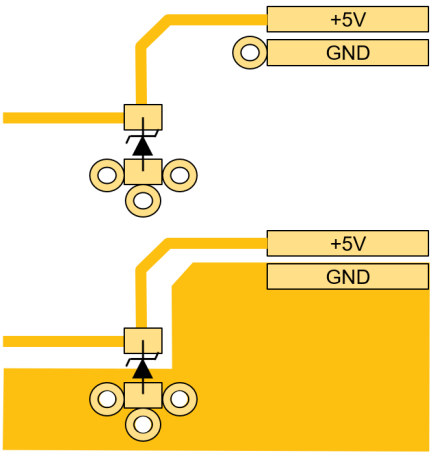
Minimizing $L_{TVS\ PATH}$ is achieved by driving as directly as possible the input track to the TVS pad and minimizing L_{GND} by using vias.

2.2 TVS layout

2.2.1 Connection to ground

Figure 10 shows examples of a way to reduce L_{GND} by multiplying the vias from the TVS to the ground. In the first one, the vias drive the current to the ground layer and in the second, the TVS ground is also connected on the first layer ground plane.

Figure 10. TVS ground connection



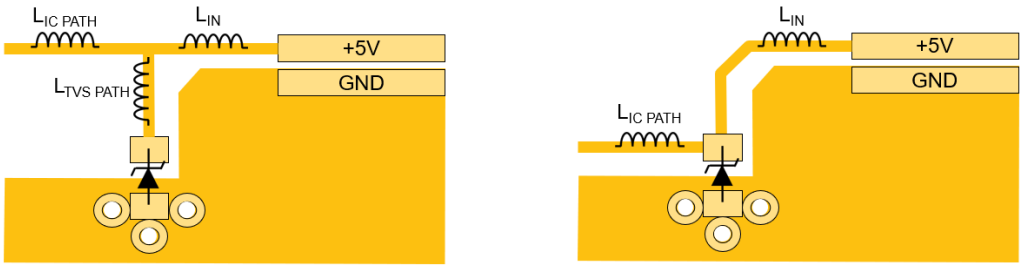
2.2.2 Line connection

When TVS is on the same PCB side than the line to protect, connection between line and TVS must be as close as possible, to minimize $L_{TVS\ PATH}$.

Figure 11 shows two ways to connect TVS to the line to protect:

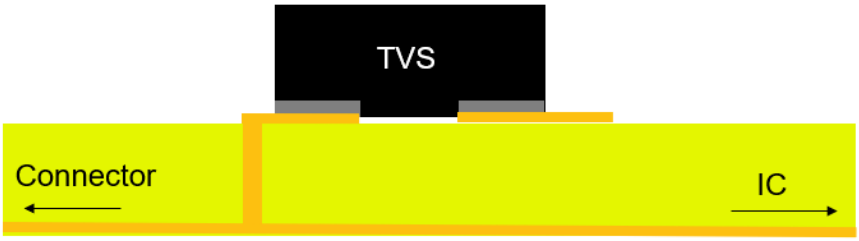
- The left layout implies the presence of $L_{TVS\ PATH}$, so not recommended
- With the layout on the right, $L_{TVS\ PATH}$ is canceled, so it is the right way. On other word, track must from connector to TVS, and then from TVS to IC to protect.

Figure 11. TVS routing, on the left, not recommended, on the right, recommended layout



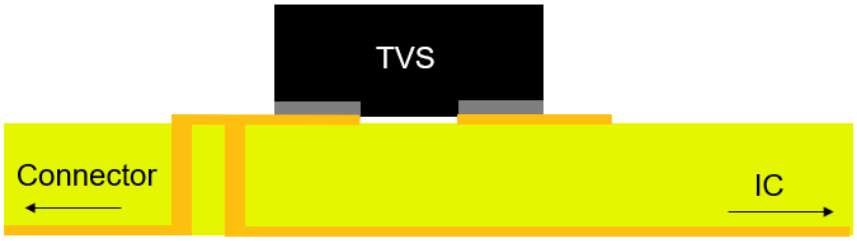
When line to protect is not on the same PCB side (or internal layer) than TVS, vias must be used carefully because they can act like inductance such as in the Figure 12. In this case the via correspond to $L_{TVS\ PATH}$ in Figure 9.

Figure 12. **Via acts like inductance, not recommended**



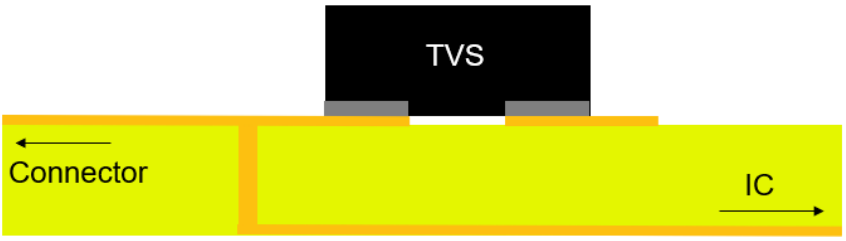
If the path to be protected is on the same layer that the ESD source the best way is to route as in Figure 13. The parasitic inductance $L_{TVS\ PATH}$ is then reducing to its minimum.

Figure 13. **Double via, better way**



But the best configuration is to route directly the ESD source to the TVS, and then changing layer by the via as in Figure 14.

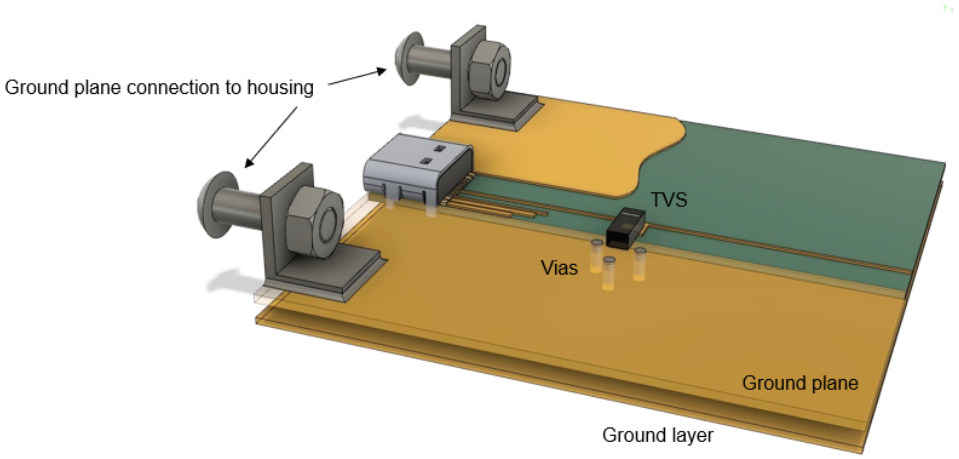
Figure 14. **Optimum routing configuration with vias**



2.2.3 Low ground impedance

In Figure 4 we have seen the influence of the ground inductance which is the main contributor to peak ESD overvoltage. The best way to reduce it is to maximize the vias number around the TVS ground as we saw in Section 2.2.2 Line connection and to connect them to the closer ground plane layer to minimize also the resistance of the ground path. Connecting this ground plane to the metallic housing of the equipment is also recommended (see Figure 15), when possible.

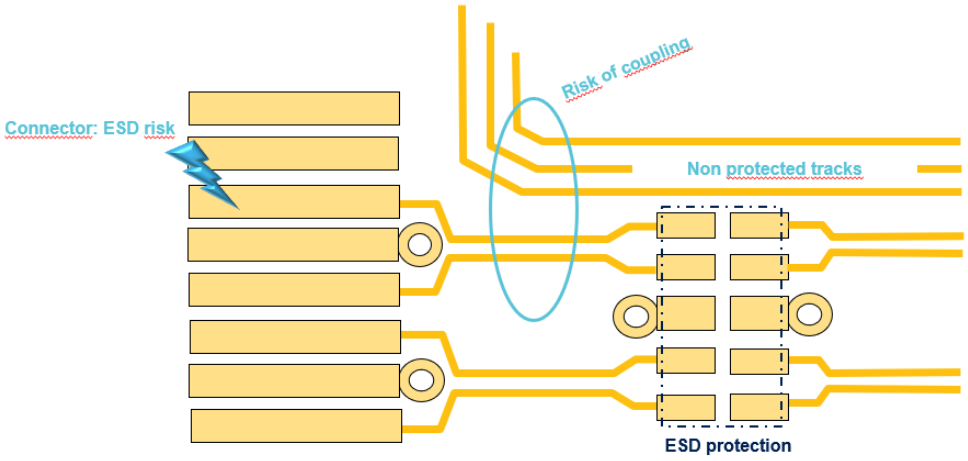
Figure 15. Ground vias and ground plane



2.2.4 Limiting EMI effects

As we have seen in Figure 6, Figure 7 and Figure 8, ESD event generates important magnetic field. If unprotected tracks are routed near tracks which can receive an ESD strike, there is a risk that, by coupling, transient voltages would be generated and malfunction occurred (see Figure 16).

Figure 16. Risk of EMI coupling on non-protected tracks



It is mandatory to separate the protected tracks exposed to ESD and all other “clean tracks”. For the same reason, the “risky” vias must be routed far from other ones.

3 Layout examples

Following the previous recommendations, here are some typical layouts for various packages and applications.
Figure 17 shows the layouts to be done in case of HDMI TMDS lanes with a type A connector. Notice that in any case, to ensure robust signal integrity, the differential impedance as to be respected for each lane.

Figure 17. Layout for HDMI TMDS type A connector with 2 x HSP051-4M10

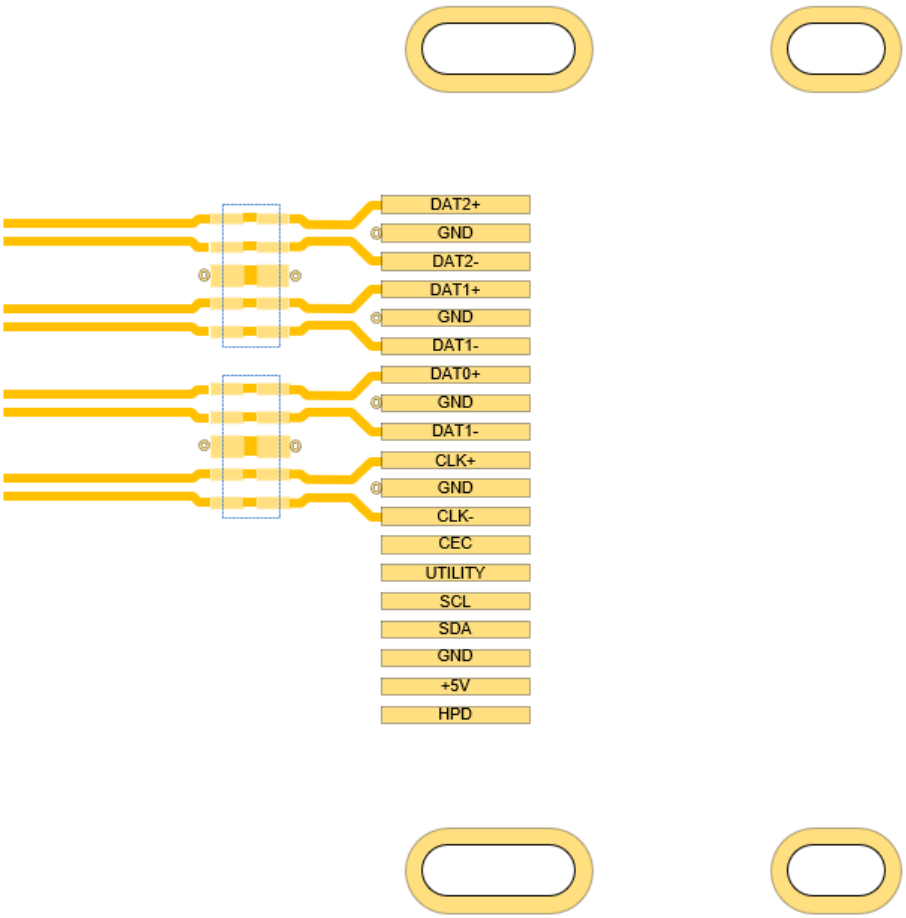


Figure 18 shows a schematic for USB 3.2 type C connector protection and Figure 19 associated layout example.

Figure 18. **Schematic example for USB 3.2 Type C connector protection**

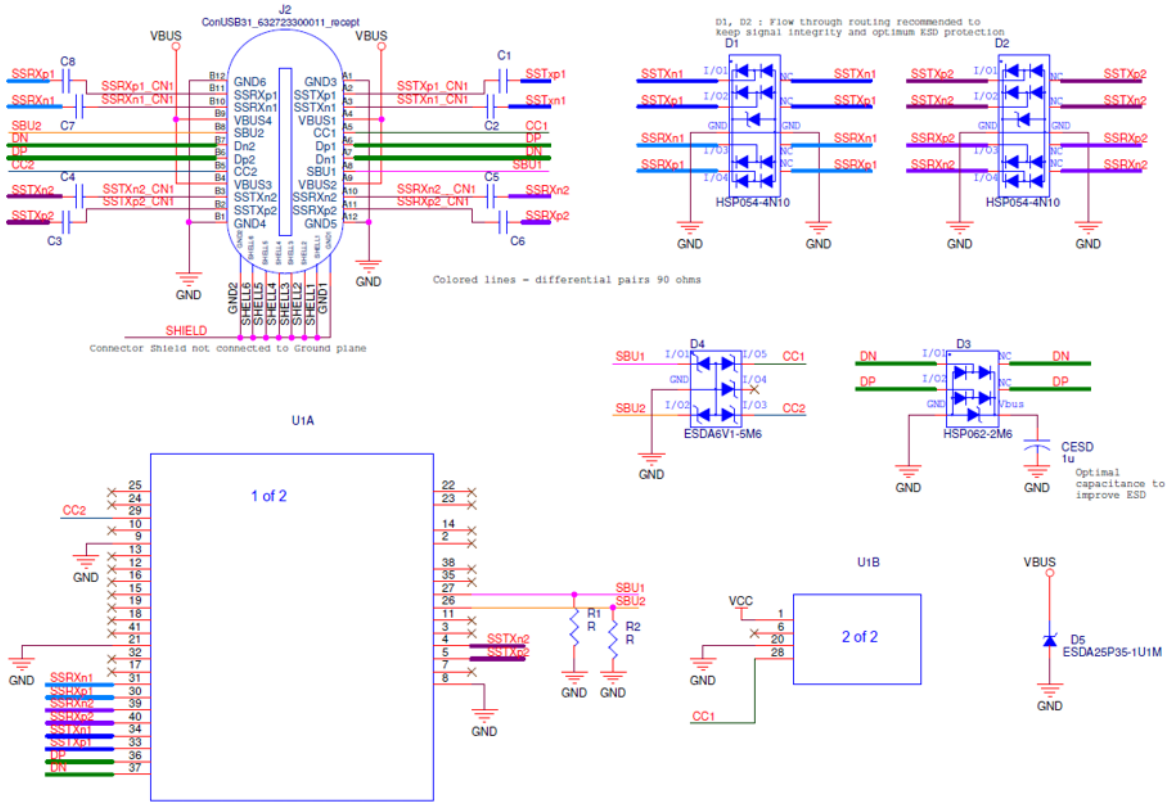
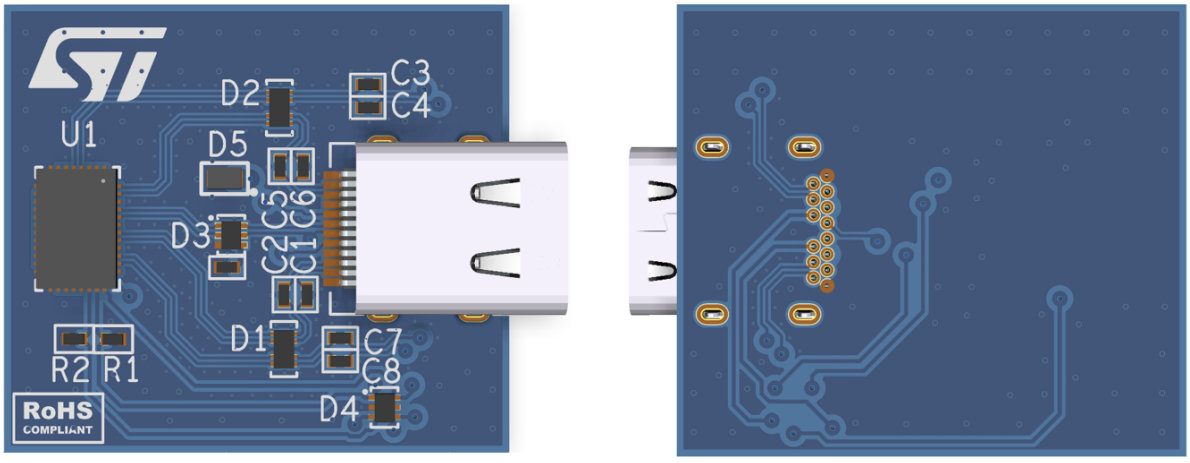


Figure 19. **Layout example for USB 3.2 Type C connector protection**



4 Conclusion

Choosing an effective protection device to ensure robust and reliable operation of an equipment is not enough. We saw in this note that it is mandatory to take care of the PCB layout in order to limit the various parasitic generating overvoltage and electromagnetic interference.

Taking care on ground connection and placing the TVS on the right way is the key for a successful circuit insuring a high reliability level of the equipment.

To summarize, below essential points:

- Ensure the protection device connection to ground as short as possible, with multiple vias to minimize parasitic inductance
- Routing is from ESD source to protection component, and then from protection component to chip to protect (and not from ESD source to chip to protect, and then the protection is connected to this track). This is also a avoid parasitic inductance
- Place the protection component as close as possible to ESD source: this minimizes the EMI on the PCB, couplings with other tracks

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- On protection devices, please visit https://www.st.com/protection
- On filter and ESD protection, please visit https://www.st.com/filter

Revision history

Table 2. **Document revision history**

Date	Revision	Changes
07-Jul-2021	1	Initial release.

Contents

List of figures