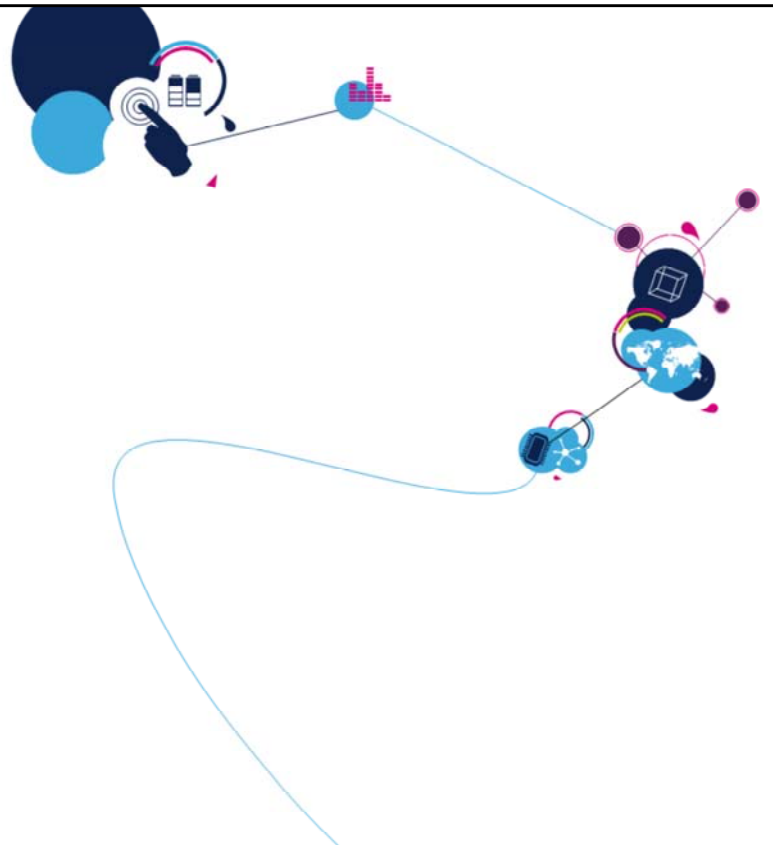# STM32F7 - FMC

Flexible Memory Controller
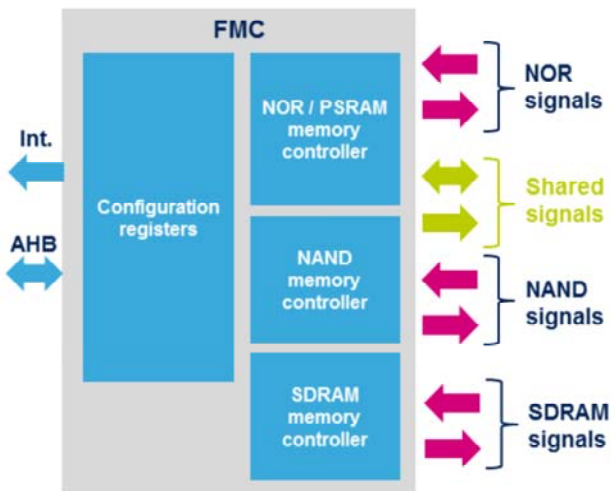
Revision 1

life.augmented

Hello, and welcome to this presentation of the STM32F7 Flexible Memory Controller. It covers all the features of this interface which is used to connect external memories such as NOR Flash, NAND Flash, SRAM, PSRAM and SDRAM.

The FMC controller integrated in STM32F7 products provides external memory support through three memory controllers: the NOR Flash/PSRAM controller, the SDRAM controller and the NAND memory controller. This enables the CPU to communicate with external memories including NOR and NAND Flash memories, PSRAM, SRAM, and SDRAM. This interface is fully configurable, allowing easy connection with external memories or other parallel interfaces.

The benefits of the FMC controller include not only RAM and Flash memory space extension, but also the ability to interface seamlessly with most LCD controllers which support Intel 8080 and Motorola 6800 modes. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules containing embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

- **Fully independent banks**
  - Four banks to support separate external memories
  - Independent Chip Select for each memory bank
  - Independent configuration for each memory bank

- **Flexible configuration**
  - FMC external access frequency is up to HCLK/2
  - Programmable timings to support a wide range of devices
  - 8- ,16- or 32-bit data bus
  - External asynchronous wait control
  - Extended mode (read timings and protocol different to write timings)
  - Supports burst mode access to synchronous devices (NOR Flash and PSRAM)
  - Write FIFO with 16 x 32-bit depth

The FMC controller offers four independent banks to support separate external memories. Each bank has an independent Chip Select and an independent configuration.
Each bank features programmable timings, a configurable 8- 16- or 32-bit data bus, and can access memory in asynchronous or burst mode for synchronous memory such as NOR Flash and PSRAM.
Synchronous memory can be accessed at a maximum frequency of HCLK divided by 2.

Supported devices

Compatible with a wide variety of interfaces and memories

- Static memory-mapped devices including
  - Static random access memory (SRAM)
  - Read-only memory (ROM)
  - NOR / OneNAND Flash memory
  - PSRAM

- NAND Flash memory
  - Includes ECC hardware to check up to 8 Kbytes of data read/written
  - 3 possible interrupt sources (level, rising edge and falling edge)

- SDRAM memory
  - Interfaces with Synchronous DRAM (SDRAM) memory-mapped

The FMC controller supports a wide variety of devices and memories.

It interfaces with static memory-mapped including static random access memory (SRAM), read-only memory (ROM), NOR / OneNAND Flash memory and PSRAM.

The FMC also interfaces with NAND Flash memories and supports error code correction (ECC) for up to 8 Kbytes of data read or written. Three interrupt sources can be configured to generate an interrupt when a rising edge, falling edge, or high level is detected on the NAND Flash Ready/Busy signal.

It also interfaces with Synchronous DRAM (SDRAM) memories

Supported devices

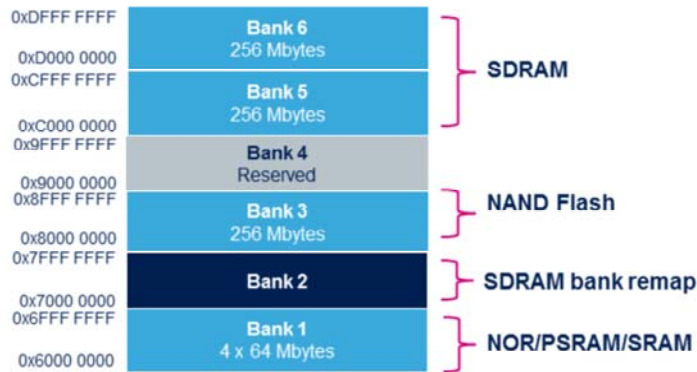## Compatible with a wide variety of interfaces and memories

- Parallel LCD modules
  - Intel 8080 and Motorola 6800

Furthermore, the FMC interfaces with parallel LCD modules, supporting the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to various LCD interfaces.
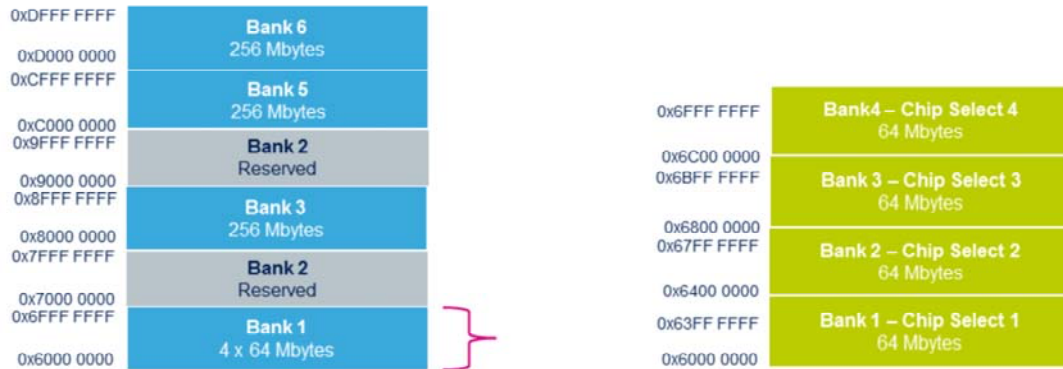
FMC Bank memory mapping

- External memories are divided into 4 fixed-size banks
  - Bank 1 (4 x 64 Mbytes) for NOR Flash, SRAM or PSRAM
  - Bank 3 (256 Mbytes) for NAND Flash
  - Bank 2 is used for SDRAM bank remap and Bank 4 is reserved.
  - Banks 5 & 6 for SDRAM

Address	Bank	Memory
0xDFFF FFFF	Bank 6 – 256 Mbytes	SDRAM
0xD000 0000		
0xCFFF FFFF	Bank 5 – 256 Mbytes	SDRAM
0xC000 0000		
0x9FFF FFFF	Bank 4 – Reserved	
0x9000 0000		
0x8FFF FFFF	Bank 3 – 256 Mbytes	NAND Flash
0x8000 0000		
0x7FFF FFFF	Bank 2	SDRAM bank remap
0x7000 0000		
0x6FFF FFFF	Bank 1 – 4 x 64 Mbytes	NOR/PSRAM/SRAM
0x6000 0000		

The external memory space is divided into fixed-size banks of 256 Mbytes each. Four external memory banks are dedicated to the FSMC. Bank 1 is connected to the NOR/PSRAM controller, Bank 3 is connected to the NAND controller and Banks 5 and 6 are connected to SDRAM. Bank 2 is used for SDRAM bank remap and Bank 4 is reserved.

NOR / PSRAM address mapping

- Bank 1 is divided into 4 banks of 64 Mbytes each to interface with 4 external NOR / PSRAM memories (4 Chip Selects) which support
    - NOR Flash: 8/16/32-bit synchronous/asynchronous, multiplexed or non-multiplexed
    - SRAM/ROM: 8/16/32-bit
    - CRAM/PSRAM: 8/16/32-bit synchronous/asynchronous

Address	Bank
0xDFFF FFFF	Bank 6 — 256 Mbytes
0xD000 0000 / 0xCFFF FFFF	Bank 5 — 256 Mbytes
0xC000 0000 / 0x9FFF FFFF	Bank 2 — Reserved
0x9000 0000 / 0x8FFF FFFF	Bank 3 — 256 Mbytes
0x8000 0000 / 0x7FFF FFFF	Bank 2 — Reserved
0x7000 0000 / 0x6FFF FFFF	Bank 1 — 4 x 64 Mbytes
0x6000 0000	

Address	Bank
0x6FFF FFFF	Bank4 – Chip Select 4 — 64 Mbytes
0x6C00 0000 / 0x6BFF FFFF	Bank 3 – Chip Select 3 — 64 Mbytes
0x6800 0000 / 0x67FF FFFF	Bank 2 – Chip Select 2 — 64 Mbytes
0x6400 0000 / 0x63FF FFFF	Bank 1 – Chip Select 1 — 64 Mbytes
0x6000 0000	

Bank 1 is used to address up to 4 NOR Flash memories or PSRAM devices. This bank is split into 4 NOR or PSRAM sub-banks of 64 Mbytes each with 4 dedicated Chip Selects to interface with:
8- or 16-bit synchronous or asynchronous NOR Flash in multiplexed or non-multiplexed mode.
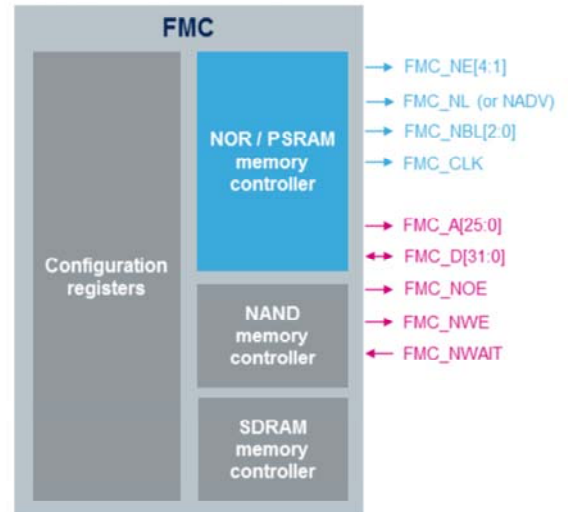8- or 16-bit asynchronous SRAM and ROM.
8- or 16-bit synchronous or asynchronous PSRAM memories.

NOR / PSRAM interface signals

- **The FMC generates the appropriate signals to drive**
  - Asynchronous SRAM and ROM
    - 8-bit
    - 16-bit
    - 32-bit
  - PSRAM (CellularRAM and CosmoRAM)
    - Asynchronous mode
    - Burst mode
    - Multiplexed or non-multiplexed
  - NOR Flash
    - Asynchronous mode
    - Burst mode
    - Multiplexed or non-multiplexed

FMC

Configuration registers

NOR / PSRAM memory controller

NAND memory controller

SDRAM memory controller

→ FMC_NE[4:1]
→ FMC_NL (or NADV)
→ FMC_NBL[2:0]
→ FMC_CLK

→ FMC_A[25:0]
↔ FMC_D[31:0]
→ FMC_NOE
→ FMC_NWE
← FMC_NWAIT

The FMC outputs a unique Chip Select signal to each bank and performs only one access at a time to an external device. The external memories are connected either to the NOR PSRAM controller or the NAND controller, and share address, data, and control signals.

NOR / PSRAM timing configuration

Flexible timing configuration

- The FMC NOR / PSRAM controller is used to set the timings of the memory connected to the bank
  - Address setup phase duration
  - Address hold phase duration
  - Data setup phase duration
  - Bus turnaround phase duration
  - Clock divide ratio
  - Data latency (for synchronous burst NOR Flash)
  - Access mode

The NOR PSRAM controller allows the configuration of various timing parameters for the supported memories:
Address setup phase: Duration of the first access phase
Address hold phase: Duration of the middle phase of the access cycle
Data setup phase: Duration of the second access phase
Bus turnaround phase: Duration of the bus turnaround phase
Clock divide ratio: Number of AHB clock cycles (HCLK) within one memory clock cycle (CLK)
Data latency: Number of clock cycles to be issued to the memory before the first data transfer
Access mode.

NAND address mapping

- Bank 3 is used to support NAND Flash memory through two memory spaces
  - Common memory space
  - Attribute memory space

- Each memory space is divided into 3 subsections
  - Data section (64 Kbytes): Used to read or write data
  - Command section (64 Kbytes): Used to send a command to NAND Flash memory
  - Address section (128 Kbytes): Used to specify the NAND Flash memory address
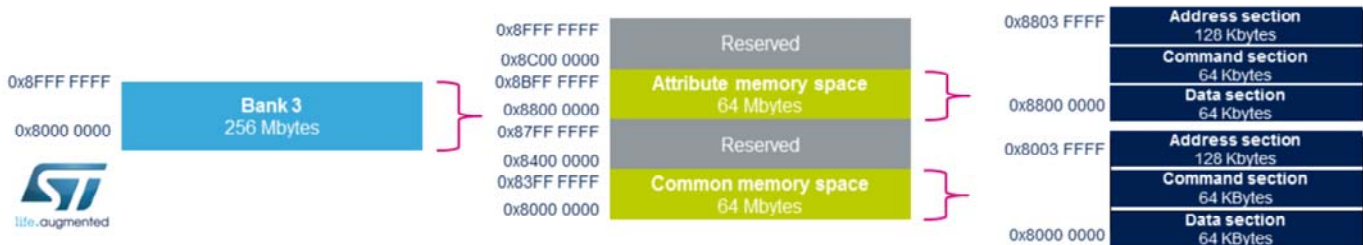
Bank 3 is used to interface with the NAND Flash memory. It is divided into two memory spaces: Common memory space and Attribute memory space. Both spaces are similar. The common memory space is for all NAND Flash read and write accesses, except when writing the last address byte to the NAND Flash device, where the CPU must write to the attribute memory space. This allows to implement the pre-wait functionality needed by certain NAND Flash memories by writing the last address byte with different timings.

Each memory space is subdivided into three sections:

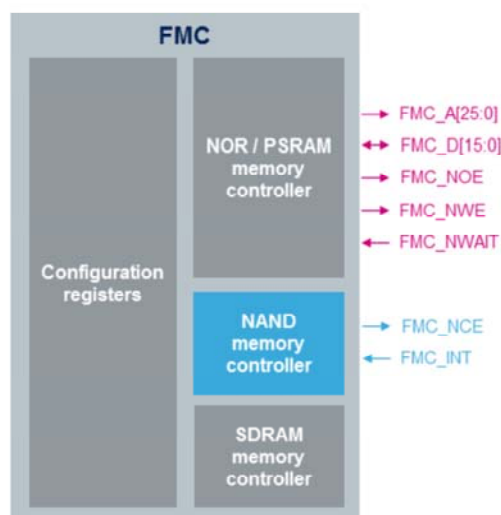Data section (64 Kbytes): Used to read or write data from NAND Flash memory.

Command section (64 Kbytes): Used to send a command to NAND Flash memory.

Address section (128 Kbytes): Used to specify the NAND Flash memory address.

NAND interface signals

- The FMC generates the appropriate signals to drive the NAND memories
  - NAND Flash
    - 8-bit
    - 16-bit

The FMC generates the appropriate signals to drive NAND Flash memory. The address, data, and control signals are shared with the NOR / PSRAM controller.

The command latch enable (CLE) and address latch enable (ALE) signals of the NAND Flash memory device are driven by address signals from the FMC controller connected to Address line 16 and Address line 17 respectively.

The ALE is active when writing to the address section and the CLE is active when writing to the command section.

NAND configuration

- The FMC NAND memory controller supports the following features
  - ECC hardware acceleration for read and write operations ranging from 256 to 8192 bytes
  - 3 interrupt sources for NAND bank
    - Rising edge
    - Falling edge
    - Level of the external memory Ready/nBusy output pin
  - Wait feature management
    - The controller waits for the NAND Flash memory to be ready (Ready/nBusy signal high), before starting a new access.

- The MPU memory attribute of the FMC NAND bank must be configured as "Device".

The FMC NAND memory controller includes support for the following features:
Error code correction: The ECC algorithm can perform 1-bit error correction and 2-bit error detection per 256 to 8192 bytes read or written from/to the NAND Flash memory. It is based on the Hamming coding algorithm.
3 interrupt sources can be enabled to detect a rising edge, falling edge or level on Ready/Busy signal output from NAND Flash memory.
Wait feature management: The controller waits for the NAND Flash memory to be ready before starting a new access.
The MPU memory attribute of the FMC NAND bank must be configured as a Device

NAND timing configuration

- For each memory space a set of parameters can be configured
    - Setup time: Time to set up the address before the command assertion
    - Wait time: Time to assert the command
    - Hold time: Time to hold address after the command de-assertion
    - Data bus HiZ time: Time from address valid to data bus drive

Each common and attribute memory space can be configured with different timings for the NAND Flash's command, address write, and data read/write accesses. The attribute memory space is used for the last address write access if the timing must differ from that of previous accesses in case of
Ready/Busy management. Otherwise, only common space is needed.
Four parameters are used to define the number of HCLK cycles for the different phases of any NAND Flash access:
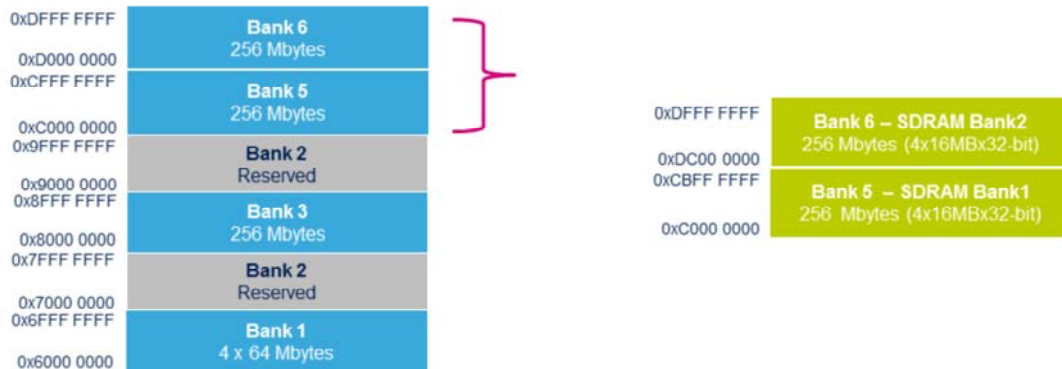Setup time
Wait time
Hold time
Data bus HiZ time

Interrupt event	Description
Rising edge	Rising edge has been detected on FMC_INT pin
Falling edge	Falling edge has been detected on FMC_INT pin
High level	High level has been detected on FMC_INT pin

The NAND controller offers 3 interrupt sources: rising edge, falling edge, and high level detection on the FSMC INT pin when it is connected to the Ready/nBusy signal from the NAND Flash memory.

SDRAM address mapping

- Up to **512 Mbytes of continuous memory** split into two banks, can be seen as a single device.

- Each bank can address up to 256 Mbytes of memory

Address	Bank
0xDFFF FFFF	**Bank 6** 256 Mbytes
0xD000 0000	
0xCFFF FFFF	**Bank 5** 256 Mbytes
0xC000 0000	
0x9FFF FFFF	**Bank 2** Reserved
0x9000 0000	
0x8FFF FFFF	**Bank 3** 256 Mbytes
0x8000 0000	
0x7FFF FFFF	**Bank 2** Reserved
0x7000 0000	
0x6FFF FFFF	**Bank 1** 4 x 64 Mbytes
0x6000 0000	

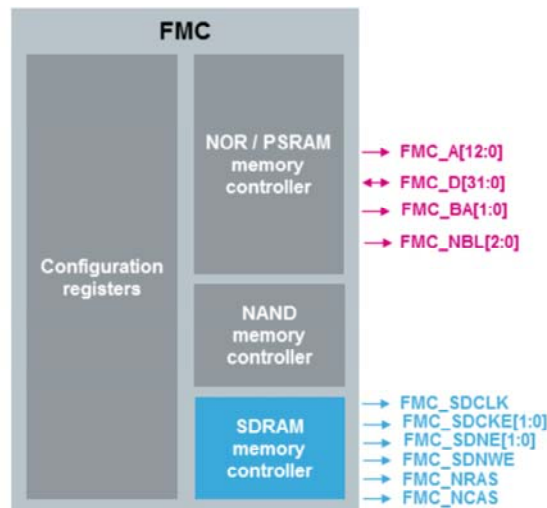| Address	Bank
0xDFFF FFFF	**Bank 6 – SDRAM Bank2** 256 Mbytes (4x16MBx32-bit)
0xDC00 0000	
0xCBFF FFFF	**Bank 5 – SDRAM Bank1** 256 Mbytes (4x16MBx32-bit)
0xC000 0000	

Banks 5 and 6 are used to interface with SDRAM memory.
Each bank can address up to 256 Mbytes of memory.
The two banks can be used to interface with two SDRAM devices.

SDRAM interface signals

- The FMC generates the appropriate signals to drive the SDRAM memories
  - SDRAM
    - 8-bit
    - 16-bit
    - 32-bit

FMC

Configuration registers

NOR / PSRAM memory controller
→ FMC_A[12:0]
↔ FMC_D[31:0]
→ FMC_BA[1:0]
→ FMC_NBL[2:0]

NAND memory controller

SDRAM memory controller
→ FMC_SDCLK
→ FMC_SDCKE[1:0]
→ FMC_SDNE[1:0]
→ FMC_SDNWE
→ FMC_NRAS
→ FMC_NCAS

The FMC generates the appropriate signals to drive SDRAM memory. The address and data are shared with the NOR / PSRAM controller.

The Bank address signals FMC BA0 and FMC BA1 are shared with FMC A14 and FMC A15 respectively.

The SDRAM controller has dedicated signals:
- SDCLK: SDRAM clock
- SDCKE0: SDRAM Bank 1 Clock Enable
- SDCKE1: SDRAM Bank 2 Clock Enable
- SDNE0: SDRAM Bank 1 Chip Enable
- SDNE1: SDRAM Bank 2 Chip Enable
- NRAS: Row Address Strobe
- NCAS: Column Address Strobe
- SDNWEN: Write Enable

SDRAM configuration

- Up to 4 internal banks with configurable Row and Column sizes:
  - up to 13-bit Address Row,
  - up to 11-bit Address Column.

- Programmable timing parameters for different SDRAM device requirements
  - Automatic Refresh operation with programmable Refresh rate

- Automatic row and bank boundary management

- Configurable SDRAM clock speed
  - One-half AHB speed (HCLK /2)
  - One-third AHB speed (HCLK/3)

The FMC controller offers two independent SDRAM banks to support separate external memories. Each bank has an independent Chip Select and an independent configuration. Each SDRAM bank can support memory devices with up to 4 internal banks. The device size is programmable with up to 13 bits for Address Row and up to 11 bits for Address Column.
SDRAM can be accessed at maximum frequency of HCLK divided by 2.
Each bank features programmable timings and a configurable 8-, 16- or 32-bit data bus.

SDRAM Multibank access

Multi Bank Ping-Pong access

- Multibank ping-pong access allows to perform consecutive write accesses to different banks

- SDRAM controller keeps track of the active row for each bank,

- Avoids bank precharge and row activation if the row is already activated.

Multibank ping-pong access allows to perform consecutive write accesses to different banks.
Consequently, it avoids bank precharge and row activation when the row is already activated in the accessed bank.

SDRAM optimized access

Optimized Read access

- Cacheable Read FIFO with depth of six 32-bit lines

- Configurable Read Burst allows to anticipate the next read accesses during CAS latencies

The SDRAM controller adds a cacheable read FIFO with a depth of 6 32-bit lines. The Read FIFO is used when the Read Burst is enabled and allows to anticipate the next read accesses during CAS latencies.

SDRAM low-power modes

Energy-saving capabilities

- Two low-power modes are supported:
  - Self-refresh mode
    - When in Self-refresh mode, the SDRAM retains data without external clocking
    - The device can remain in Self-refresh mode as long as requested by the application.
    - Self-refresh mode is exited when:

      SDRAM device is selected (read/write operation requested) or MODE bits are set to '000' (Normal mode)

  - Power-down mode
    - The device cannot remain in Power-down mode longer than the refresh period. The SDRAM controller carries out the refresh operation.
    - Power-Down mode is exited when:

      MODE bits are set to '000' (Normal mode)

For energy saving, the SDRAM controller cane be configured in one of two low-power modes: Self-refresh or Power-down mode.
When in self-refresh mode, the SDRAM retains data without external clocking.
The device can remain in self-refresh mode as long as requested by the application.
The device exits Self-refresh mode when a SDRAM device is selected (read/write operation requested) or when MODE bits are set to '000' (Normal mode).

The device cannot remain in the Power-down state longer than the refresh period because no REFRESH operations are performed in this mode. Consequently, the SDRAM controller carries out the refresh operation.
The device exits Power-down mode when MODE bits are set to '000' (Normal mode).

SDRAM commands

Supported Commands

- Commands can be delivered to the two banks simultaneously using Configure Target Bank bits (CTB1 and CTB2) in the FMC_SDCMR register

Command	MODE bits
Normal mode	'000'
Clock Configuration Enable	'001'
PALL ("All Bank Precharge") command	'010'
Auto-refresh command	'011'
Load Mode Register	'100'
Self-refresh command	'101'
Power-down command	'110'

SDRAM controller can issue different commands to the SDRAM devices:
The commands are issued by software to initialize the SDRAM device, or to switch the device mode.
The commands can be delivered to the two banks simultaneously using Configure Target Bank bits CTB1 and CTB2 in FMC_SDCMR register.
The table shows the supported commands.

SDRAM initialization procedure

- SDRAM memory power-up initialization procedure:
  1. Configure memory device features in the FMC_SDCRx register
  2. Configure memory device timings in the FMC_SDTRx register
  3. Set MODE bits to '001' in the FMC_SDCMR register to start delivering the clock signal to the memory.
  4. Wait for the prescribed delay period (typical delay is around 100 µs)
  5. Set MODE bits to '010' in the FMC_SDCMR register to issue a "Precharge All" command.
  6. Set MODE bits to '011' in the FMC_SDCMR register as well as the NRFS field number of consecutive Auto-refresh commands.
  7. Set MODE bits to '100', in the FMC_SDCMR register to issue a "Load Mode Register" command and MRD field to program the SDRAM device·
      - Burst Length (BL) has to be set to '1' and the CAS latency has to be selected
  8. Configure the refresh rate in the FMC_SDRTR register

This slide presents the SDRAM initialization procedure to implement in firmware.

Mode	Description
Run	Active.
Sleep	Active. Peripheral interrupts cause the device to exit Sleep mode.
Stop	Frozen. Peripheral registers content is kept.
Standby	Powered-down. The peripheral must be reinitialized after exiting domain and system Standby mode.

The FMC is active in Run and Sleep modes. A FMC interrupt can cause the device to exit Sleep mode. The device is not able to perform any communication in Stop and Standby modes. It is important to ensure that all transmissions are completed before the FMC controller is disabled or the domain or system is switched down to Stop or Standby modes.

To retain external SDRAM memory data while in Stop or Standby modes, it can be put in the self-refresh mode prior to entering Stop or Standby modes.
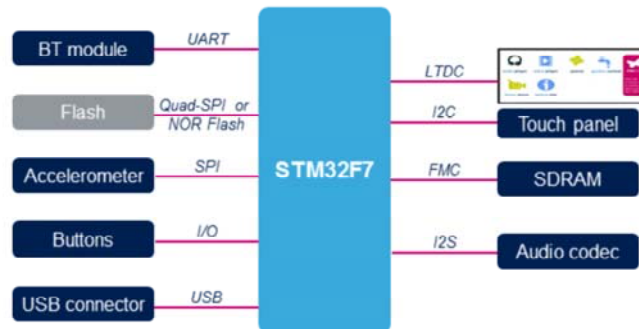
Graphic applications require low-power management together with a high-quality user interface. This can be achieved using the STM32F7 to connect the display thanks to the LCD-TFT controller. In addition, the FMC or Quad-SPI interface may be used to access an external Flash memory containing all of the graphical content needed such as background images, high-resolution icons, or fonts to support multiple languages. The internal RAM can be extended thanks to the FMC by connecting a SDRAM memory used as a frame buffer for the LTDC controller. Additional audio data for ringtones can also benefit from the large space offered by the external Flash memory.

Related peripherals

- This is a list of peripherals related to the FMC controller. Please refer to these peripheral trainings for more information if needed.
    - Reset and clock control (RCC)
    - Interrupts (NVIC)
    - General-purpose inputs/outputs (GPIO)

Here is a list of peripherals related to the FMC interface.
Users should be familiar with all the relationships
between these peripherals to correctly configure and use
the FMC controller.